

VLSI IMPLEMENTATION OF CHARGE PUMP PLL WITH LOW PHASE NOISE VCO

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Abstract

The paper explains the design of a second order power optimized Phase Locked Loop operating at higher frequency ranges with low noise. It is seen that the demand for frequency synthesizers is increasing, and a good design of the phase locked loop is necessary. The designed circuit operates from 20 to 170 MHz frequency range and can be used in data recovery, generation of clock signals, FM demodulation and in many other applications. The noise generated in the components of the PLL is minimized in order to get maximum efficiency. The PLL has a faster locking range and wide capture range enabling it to operate with lesser noise. The PLL blocks are implemented in Cadence schematic tool using 180nm NMOS and PMOS transistors.

Keywords: - PLL, CP-PLL, VCO, MOSFET, FD, PFD

1. INTRODUCTION

The emergence of electronics in the present day world has paved way in creating handy electronics goods and products in the market. The high quality and demand for products like mobile phone, television is ever-increasing. In order to meet the high demands of the market, the handy products need to be equipped with circuits capable of operating in different frequency ranges. A frequency synthesizer is an electronic circuit which produces multiple frequencies from a single frequency. A good design procedure of the frequency synthesizer is the Phase Locked Loop. A Phase Locked Loop is a feedback control system which generates an output signal proportional to the phase of the input signal. The most common on chip clock generators are based on PLL. Charge pump is one interesting configuration of the PLL. It is a PLL based frequency multiplier which consists of a Phase frequency detector, a charge pump, a loop filter, a VCO and a programmable frequency divider.

2. CP- PLL

The Charge Pump PLL consists of 5 blocks as shown in Figure 1.

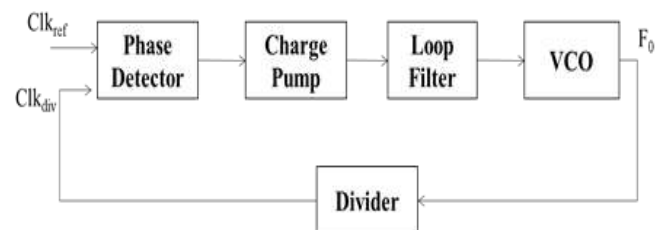


Fig 1: Block diagram of CP-PLL

The first block is the phase frequency detector, it detects the phase difference between the input signal and the feedback signal and generates the up and down pulses, which is then given to the charge pump. The charge pump produces a current signal which is stored in the loop filter. The loop filter consists of resistor and capacitor. The capacitor gets charged when the UP signal is produced and discharges when the DOWN signal is produced. This signal is then passed on to the voltage controlled oscillator, which produces the frequency of oscillations and these are converted to square wave and serve as input to the divider. The divider circuit divides the frequency and is matched with the input reference signal given to the phase frequency detector.

3. DESIGN AND IMPLEMENTATION OF CP- PLL

All the Blocks of CP-PLL are designed and implemented at transistor level in cadence schematic tool.

3.1 Phase Frequency Detector

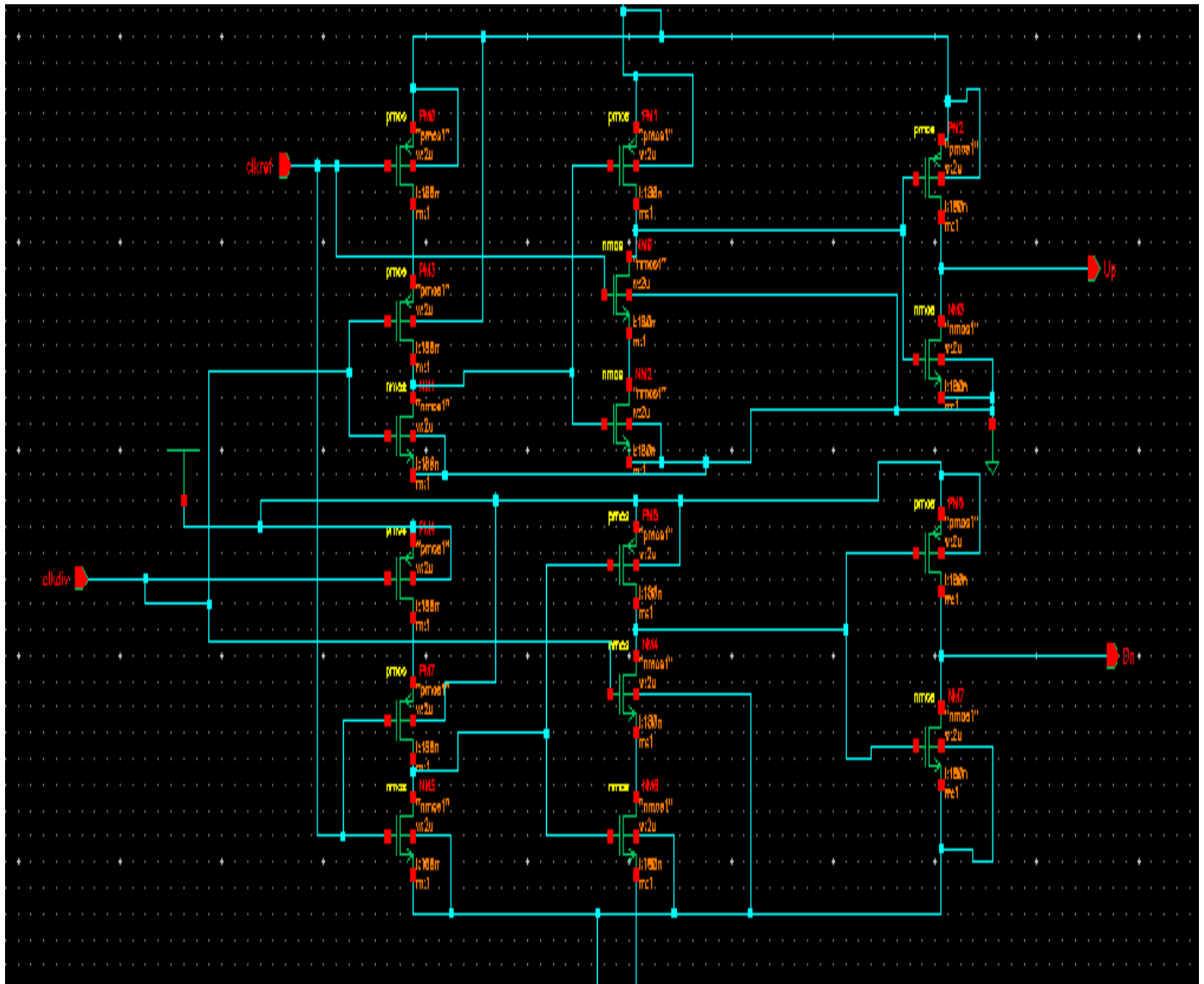


Fig 2: Schematic of PFD

The phase frequency detector is one of the main components of the PLL. It detects the phase and frequency difference between the input signal and the feedback signal. If the input signal leads the feedback signal then an UP signal is produced and the DOWN signal is zero. Similarly, if the input signal lags the feedback signal then a DOWN signal is produced and the UP signal is zero. The W/L ratio of each MOSFET is designed such that it operates in the saturation region. The K_{pd} is the gain of the phase frequency detector and is calculated using equation 1.

$$K_{pd} = V_{dd}/2\pi \dots \dots \dots (1)$$

Where $V_{dd}=1.8$ V and $\pi= 3.14$. Thus, $K_{pd} 0.2866$ v/rad.

3.2 Charge Pump and Loop Filter Design

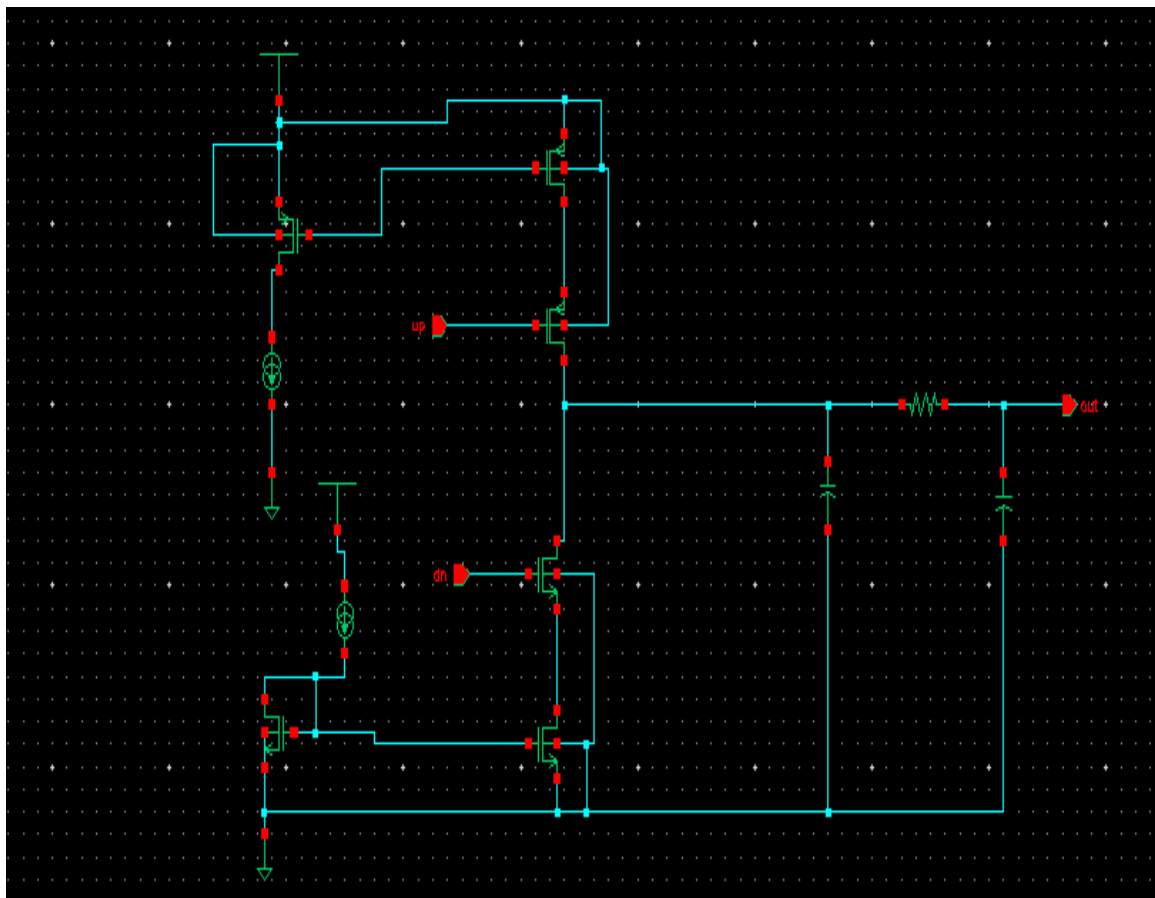


Fig 3: Schematic of Charge Pump and Loop filter

The charge pump is another important block which is used to convert the phase information in the form of UP or DOWN signals coming from the phase frequency detector into current signal. It's a kind of a DC-DC converter. The CP combines the UP and DOWN signals into a single signal and feeds it to the loop filter. It consists of two current sources, current mirrors and a PMOS and NMOS transistor which act as switches.

Loop filter is used to convert the current pulse coming from the charge pump to voltage. The frequency of oscillation of the output signal of the VCO depends on the voltage generated by the loop filter. The loop filter voltage will increase if the input signal leads the feedback signal. The loop filter voltage will decrease if the input signal lags the feedback signal. The loop filter is used to maintain the overall stability of the closed loop system. Since the PLL is a three pole system with two poles at the origin, the stability of the system decreases. Therefore, a resistor is added in series with the capacitor. Since the charge pump drives the series combination of resistor and capacitor there is a large surge in the voltage levels and hence a capacitor is added in parallel. The loop filter thus consists of two capacitors and one resistor. The values of the same is designed and calculations are done using equation 2.

$$(W_{ref}) = 2\pi F_{ref} \dots\dots\dots(2)$$

With $F_{ref} = 20.15 \text{ MHz}$, $W_{ref} = 126.542 \text{ M rad/s}$.

In order to maintain stability of the circuit W_{ugb} is chosen as $W_{ref}/50$ and $\phi M = 60 \text{ degree}$.

$$W_{ugb} = 2.53 \text{ M rad/s} \dots\dots\dots(3)$$

Constant K_c is calculated to get values of R, C_1 , C_2 .

$$K_c = C_1/C_2 = 2 (\tan^2 \phi M + \tan \phi M \sqrt{\tan^2 \phi M + 1}) = 2.928 \dots\dots(4)$$

$$C_1 = \frac{1}{R} W_z \text{ and } C_2 = C_1 / K_c \dots\dots\dots(5)$$

Let the value of $R = 10K\Omega$. From the above values and equations $C_1 = 40pF$. Thus $C_2 = 3.094pF$

Hence the designed values of resistor R, capacitor C_1 and capacitor C_2 are $10K\Omega$, $40pF$ and $3.094pF$ respectively.

3.3 Voltage Controlled Oscillator

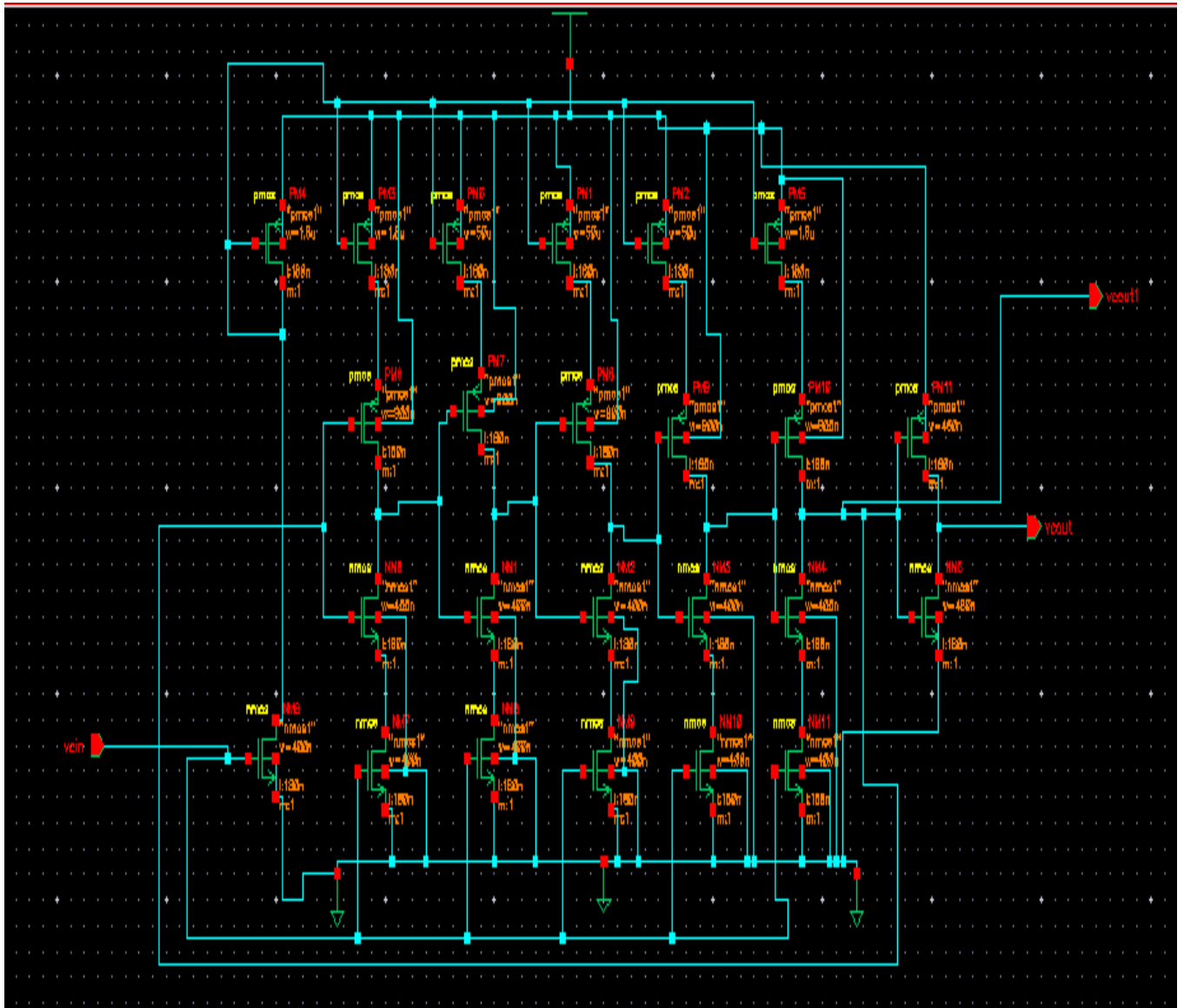


Fig 4: Schematic of VCO

The input from the loop filter is given to the voltage controlled oscillator. It generates an output whose frequency of oscillation is directly proportional to the input voltage that is provided. The inverter used here is a ring oscillator with five inverter stages. An LC oscillator can also be used as it has less noise and is error-free, but a ring oscillator occupies much lesser area compared to an LC oscillator. The designed ring oscillator has 24 transistors. In Figure 4, the top PMOS transistors and the bottom NMOS transistors act as current sources and they mirror the current into the inverter stages. There are 5 inverter stages to produce sine wave. Sixth inverter stage is provided to change the generated sine wave into a square wave which serves as input to the divider stage. The output of the fifth inverter stage is again fed back as input to the first inverter stage to ensure that the oscillator oscillates over a particular

frequency to generate a sine wave. There exists a linear relationship between the control input voltage provided as input to the oscillator stage and the obtained output frequency.

K_{vco} is the gain of the VCO. It's the slope of the graph that is plotted between voltage vs frequency. The gain is calculated using formula 6. Here the voltages ($v2$ and $v1$) and the frequencies ($f1$ and $f2$) are two points on the graph.

$$K_{vco} = 2 * \pi * f / (v2 - v1) \text{ where } f = f1 - f2 \dots \dots \dots (6)$$

Where, $f1 = 51 \text{ MHz}$,
 $f2 = 46.40 \text{ MHz}$, $v2 = 1.2 \text{ V}$ and $v1 = 0.7 \text{ V}$

Thus, $K_{vco} = 57.6504 \text{ MHz/V}$.

The Table 1 shows the frequency values at different voltage levels. It can be seen that as the voltage increases the frequency also increases.

Table 1: Voltage Vs frequency

Voltage (volt)	Frequency (MHz)
2.7	30.03
3	32.95
3.5	37.37
4	41.85
4.5	46.43

5	51.02
5.5	55.55
6	60.17
6.5	64.78
7	69.42
7.5	73.95
8	78.69
8.5	83.93
9	87.97
9.5	92.61
10	97.35

3.4 Frequency Divider

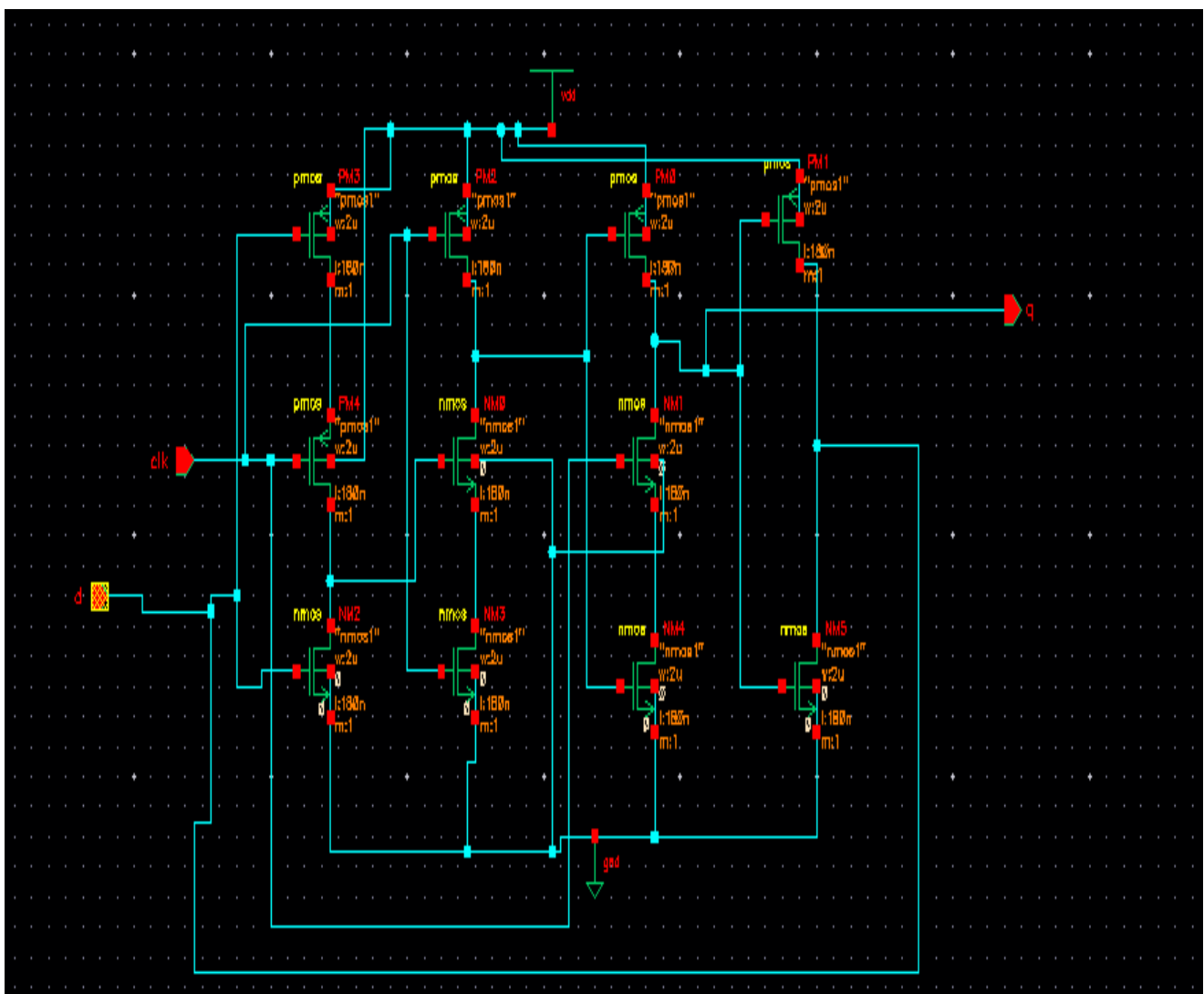


Fig 5: Schematic of Frequency Divider

The Figure 5 is a True single phase D flip flop which consists of D and clkas inputs and Q as the output. The circuit consists of PMOS and NMOS transistors which are placed alternatively, and each stage is driven by the same

clock signal. The output is not affected by the input when the clk signal is low. When the clk signal makes a low to high transition the output is Dbar and this is given as feedback to the next stage.

A divide by N frequency divider circuit is required and it can be implemented by using the D flip-flop giving the Qbar output of D flip-flop as input to the D input for the next stage. N factor is decided by calculating the output frequency of the voltage controlled oscillator divided by the reference signal given to the phase detector as input. This N factor decides the number of stages of divide by two circuits needed in the PLL. The number of stages is given by $\log_2(N)$. The TSPC flip flop is used as it dissipates less power and also occupies lesser area.

Figure 6 shows the integrated circuit of the PLL. The first block is the phase frequency detector. The second block is the charge pump with loop filter. The third block is a loop filter which consists of two capacitors and a resistor. The fourth block is the VCO. The fifth block is the frequency divider. It is basically used to scale down the frequency of the VCO. This is done in order to match the frequency of the feedback signal coming from the VCO with the input frequency. The signal is then passed through the divide by N counter and is then feedback to the phase detector.

3.5 CP-PLL

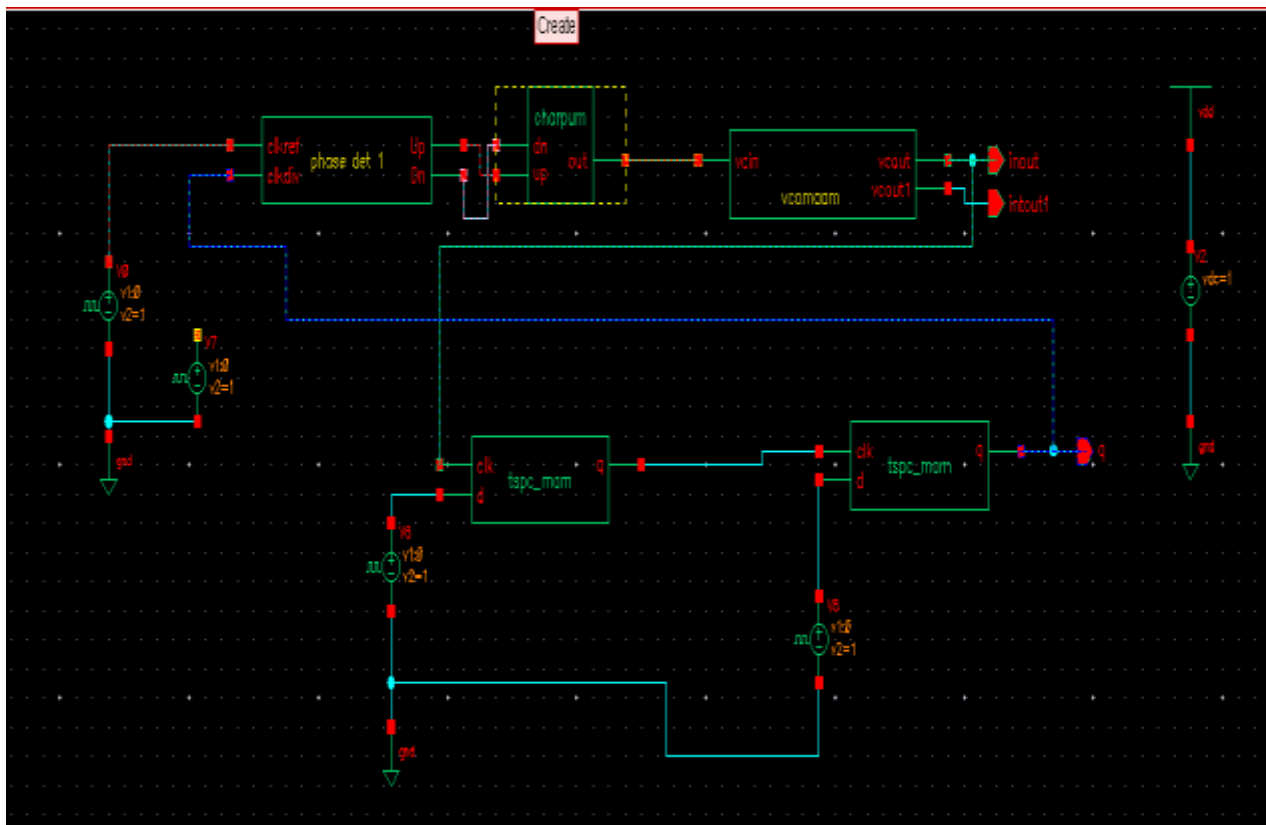


Fig 6: Schematic of PLL after integration

4. RESULTS

All the modules were designed separately and tested. The modules were then integrated to form the CP-PLL.

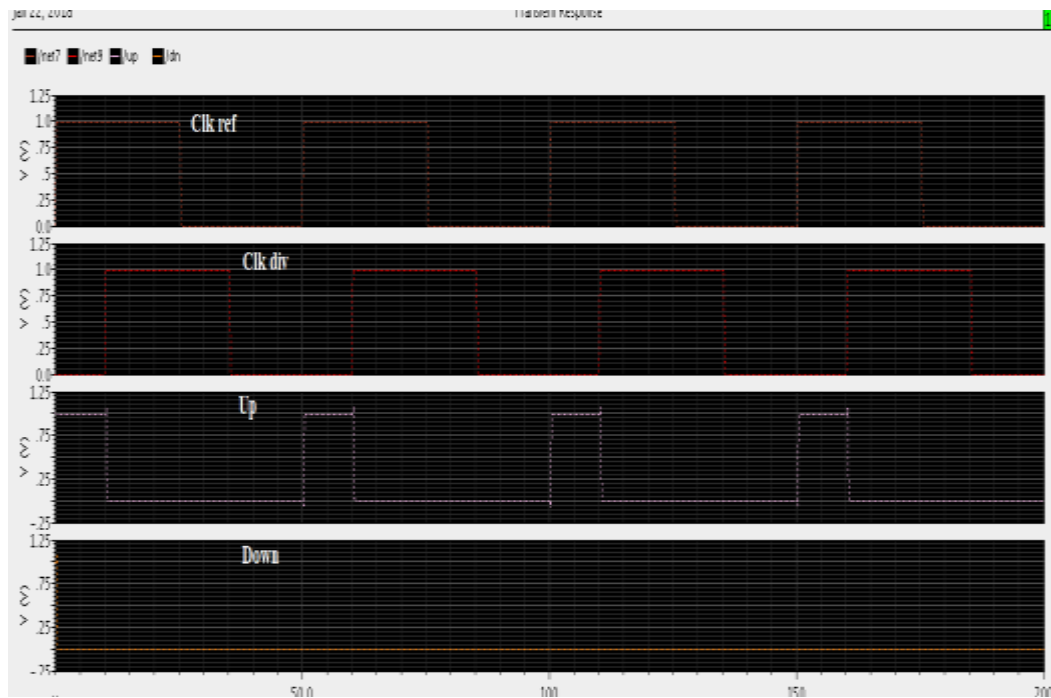


Fig 7: Output waveform of PFD(Clk_ref leading)

From Figure 7 it is clear that when the input signal leads the feedback signal the UP signal is generated and the DOWN signal is at 0V.

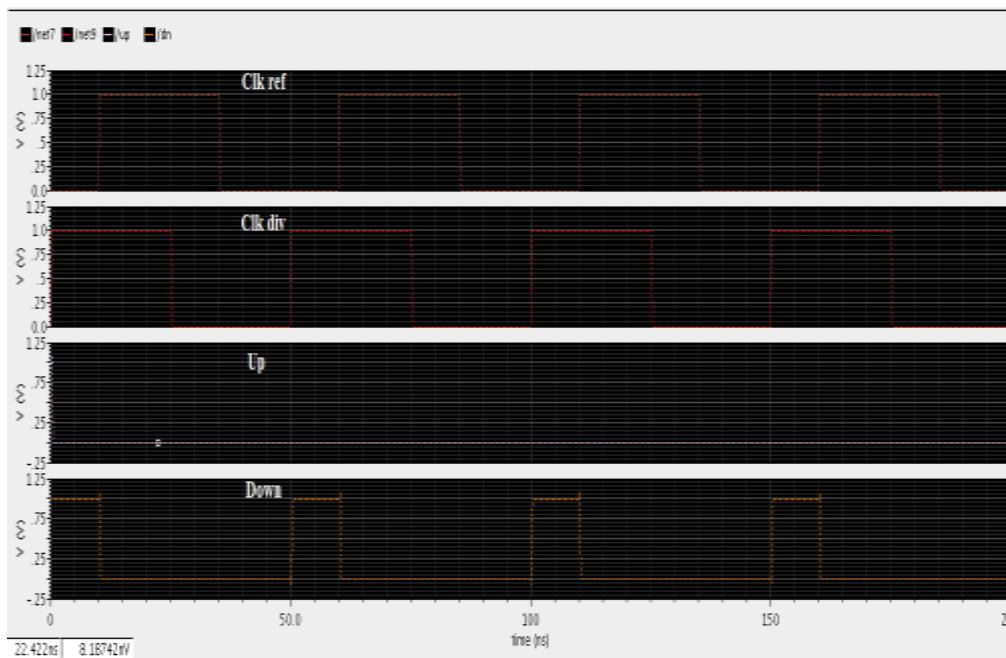


Fig 8: Output waveform of PFD(Clk_div leading)

From Figure 8 it is observed that when input signal lags the feedback signal, the DOWN signal is generated and UP signal is at 0V.

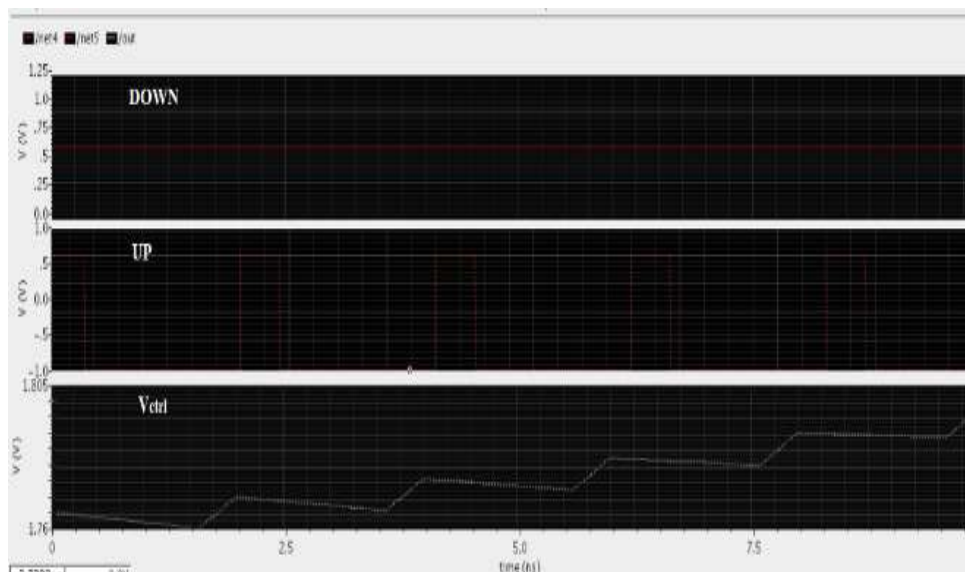


Fig 9: Output waveform of Charge Pump (UP signal)

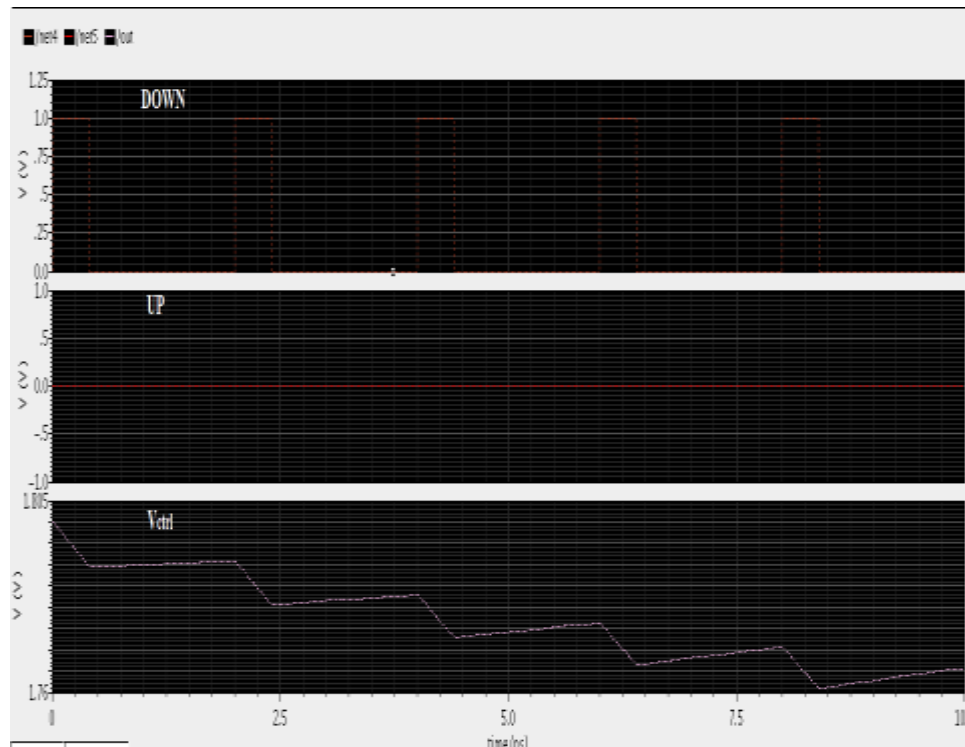


Fig 10: Output waveform of Charge Pump (DOWN signal)

When UP signal has pulse and DOWN is at zero level, charge pump produces increasing current ramp as shown in Figure 9. When DOWN signal has pulse and UP signal is at zero level, charge pump produces decreasing current ramp as shown in Figure 10. The loop filter then produces an increasing or decreasing voltage which is named as V_{ctrl} . This voltage is given as input to VCO.

The voltagecontrolled oscillator generates an output frequency as shown in Figure 11 which depends on the input provided to it.

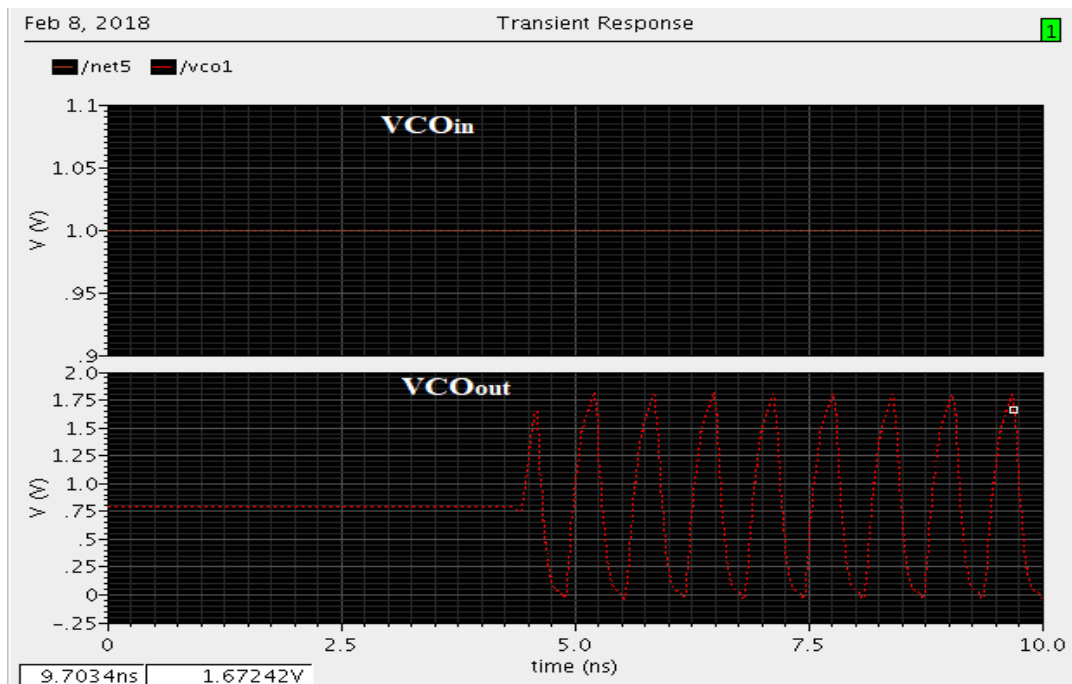


Fig 11: Output waveform of VCO

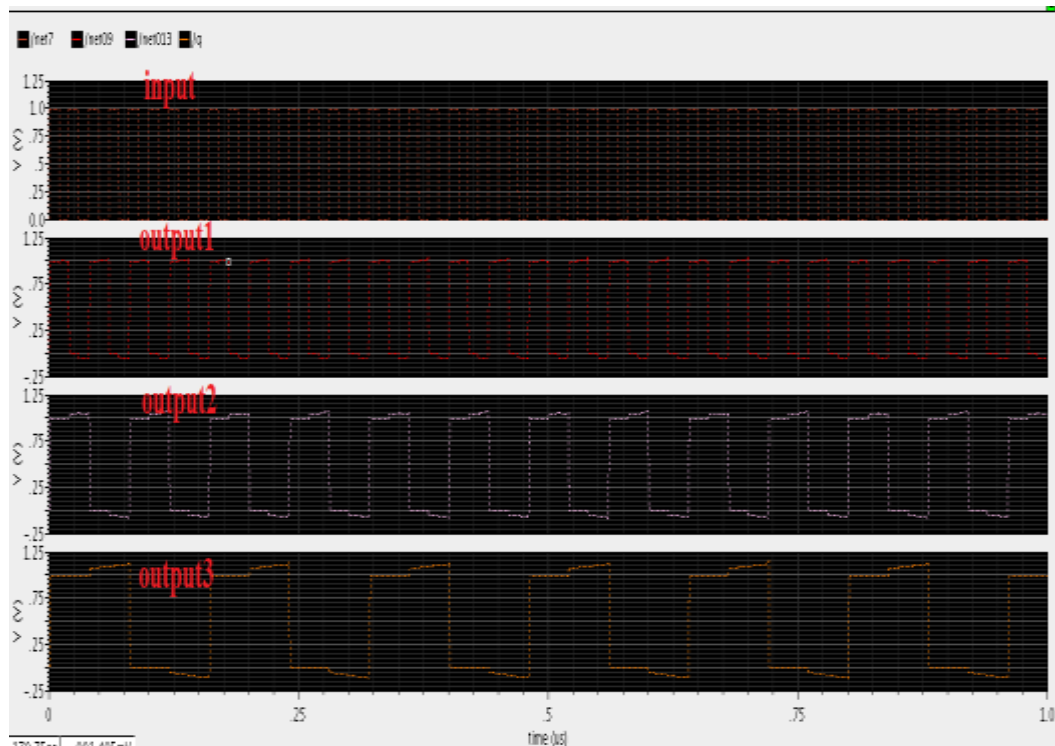


Fig 12: Output waveform of divide by 8 frequency divider.

The Figure 12 shows the output waveform of the frequency divider. The number of D flip-flops determine the divide by N value. Here three stages are used as we require divide by 8 frequency divider.

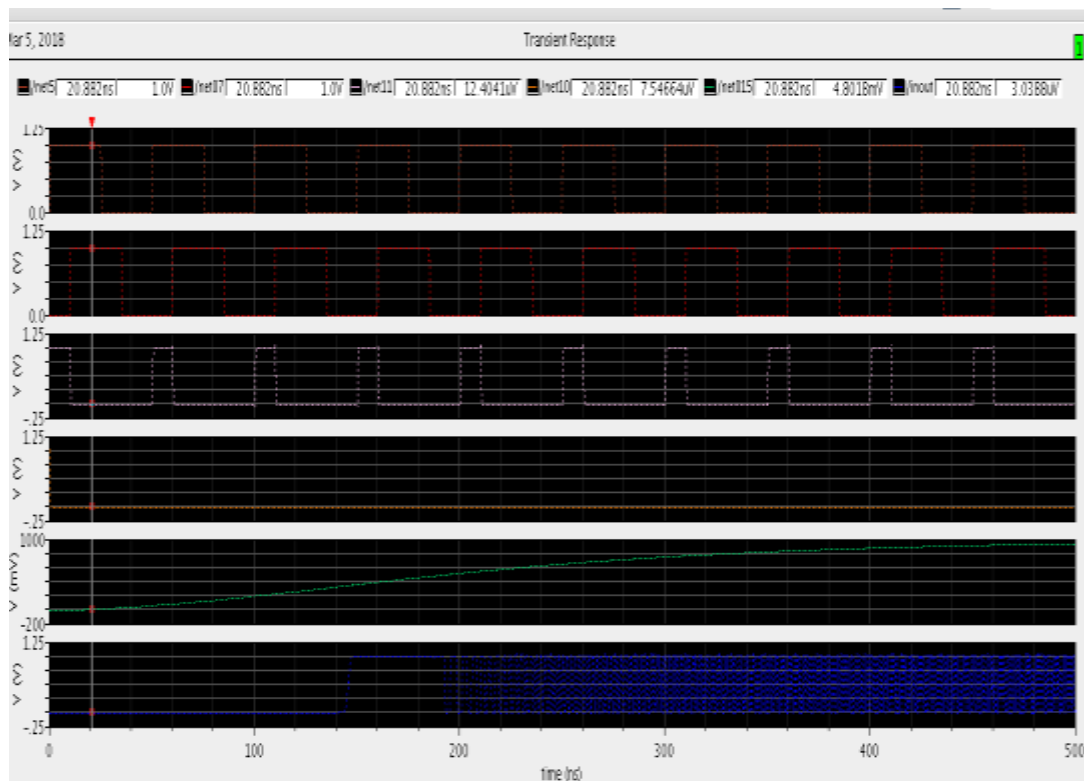


Fig 13: Output waveform of PLL

Figure 13 shows the result obtained after integration of all the blocks of the PLL. The first plot of the graph shows the input signal that was fed. The second plot shows the output signal of the VCO which is feedback to the input of the PFD. The third plot shows the UP signal which is one of the output of PFD. The fourth plot is the DOWN signal which is the other output of PFD. This signal is always zero since the

input signal leads the feedback signal. The fifth plot shows the output of the charge pump. As the input signal leads the feedback signal the output of the charge pump increases linearly and after some time it becomes constant. The sixth plot is the output of the VCO which is a sine wave, whose frequency is N times higher than that of the input signal.

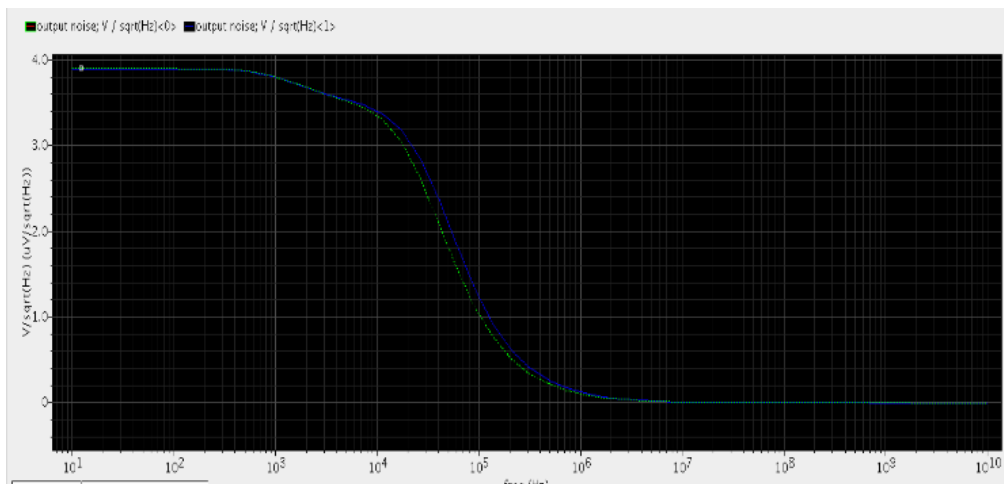


Fig 14 :Noise analysis of VCO

The Figure 14 shows that the noise curve of the VCO is constant for a certain frequency and shows a linear relationship for a range of frequencies. The noise voltage is constant 3.8V till 10000 Hz and shows a gradual decrease in

the curve from 10000 to 1 Mhz. The standard noise at 1Mhz is determined and is seen to be 0.2 V. After 1.2Mhz the voltage reduces to zero as seen in Figure 14.

5. CONCLUSION

The paper explains the simulation of CP-PLL with low phase noise voltage controlled oscillator. The paper presents the design of each block in transistor level with the specified W/L ratios. These W/L ratios are calculated using the design equations to ensure that each transistor works in saturation region. The CP-PLL presented in the paper is an ideal PLL which can be used to operate in Megahertz frequency region. Since most of the present day circuits operate in Megahertz frequency range, this PLL can be of great use in the present day technology. The charge pump is designed to store the voltage in the capacitor and serve as input to the voltage controlled oscillator. This voltage controlled oscillator is designed to operate at low noise levels. The output noise of the voltage controlled oscillator is gradually reduced when compared with the input noise of the voltage controlled oscillator. The frequency divider is simulated for divide by two initially and then cascaded to get divide by four and divide by eight dividers. All the blocks are integrated and the output is noted. The lock range is designed to be less than 10 μ s and capture range is around 10-50 μ s.

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BIOGRAPHIES



Prathima SR is currently pursuing her B.E in Electronics and Communication Engineering in R.V College of Engineering. Her area of interest is in VLSI and networking.



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