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A STUDY ON 6T SRAM AND 7T SRAM CELLS

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Abstract

Nowadays data storage is gaining more importance in human life. All electronic and digital devices need memory for reducing the power consumption. The concept of "more data in less space" is useful for increasing the system performance and overall system efficiency. Generally we used semiconductor memory as "SRAM". SRAM can be abbreviated "Static Random Access Memory". Many VLSI chip can have SRAM memory because of their large storage capacity and fast accessing time. Where, the word static indicates that it does not need to be habitually refreshed but the DRAM need habitually refreshed. DRAM can be abbreviated as "Dynamic Random Access Memory" which is another type of memory. Both the memories can be classified from "Random Access Memory: (RAM). In this paper the power analysis of 6 transistor SRAM is compared with 7 transistor SRAM. As a result the power dissipation of 7 transistors is high when compared with 6 transistors. The power dissipation of 6T SRAM is about 2.991mW and the power dissipation of 7T SRAM is about 3.183Mw.SRAM are mostly used for mobile applications, because of their ease of use and low leakage of power. In this paper the schematic of 6T SRAM and 7T SRAM are drawn using DSCH software and the layouts are drawn using MICROWIND software.

Keywords: *6T SRAM, 7T SRAM, Power Dissipation.*

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1. INTRODUCTION

In recent days, Static Random Access Memory has become the major part in digital world. Because which occupies the largest portion of SOC (system-on-chip). The device need SRAM memory mainly for device dissipate small amount of power. But the dynamic power dissipation causes problems in digital circuits because the dynamic power depends on supply voltage, switching frequency and output voltage swing. Dynamic power dissipation can be minimized by reducing the supply voltage. At the same time low supply voltage leads to performance degradation and also decreases the threshold voltage which in turn increases the sub threshold current hence the static power dissipation increases. This paper discuss about the power dissipation of 6 transistors and 7 transistors SRAM. It also includes the functional view of 6T and 7T SRAM cells.

2. 6T STATIC RANDOM ACCESS MEMORY

A conventional 6T SRAM consists 6 transistors which form two cross coupled inverters. This bit cell can be read and write single bit data. When a bit is stored in memory the 6T SRAM behave like a latch. The cross coupled inverter pattern which causes large area consumption which is a drawback of 6T SRAM when compared to resistive load. Conventional SRAM with 6 transistors is shown in figure 1 and 6T SRAM have three states they are read, write and hold states.

2.1 Hold State

When write operation (WL=0) the accessible transistor M1 and M2 disconnect the cell from bit lines. The leakage current can be drawn from $v_{dd.}$

2.2. Read State

The accessible transistor M3 and M6 should be ON when pre-charging bit and bit bar line to high.

2.3 Write state

When the WL=0, the value to be written to the bit and bit bar line. Hence we write a data value is "0", we take bit value is "0" and bit bar value is "1".and the data value is "1", we take bit value should be "1" and the bit bar value is "0".

3. 7T STATIC RANDOM ACCESS MEMORY

As like 6T SRAM, the 7T SRAM circuit also consists of two CMOS cross coupled to each other. In this circuit we additionally connect NMOS transistor to write line. And it also have two pass NMOS transistor connected to the bit and bit bar line. The access transistor N3 and N4 which are correspondingly connected to the write and read line to perform the write and read operation. Before write operation the 7T SRAM cell depends upon feedback connection. These feedback connection and disconnection can be performed by N5 transistor.

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3.1 Write Operation

The write operation can be start by turning off the N5 transistor to this cut off feedback connection. When N3 is on and N4 is off the bit line bar carries complement of input data. The N5 is turned on and WL is turned off for reconnect the feedback connection to store new data. The bit line bar is discharged to "0" for storing "1" in the cell. And there is no need to discharge bit line for storing "0" in the cell.

3.2 Read Operation

When performing the read operation both read and word lines are turned to on and also the transistor N5 is kept on.

4. RESULTS AND DISCUSSION

Here we analysis and discuss about the 6T and 7T SRAM cell during read and write operation. And the schematic view of SRAM cell is designed and implemented by using **DSCH** and **MICROWIND** software.

Table 1: Comparison of power dissipation between 6T and 7T SRAM

OPERATION	6TSRAM	7T SRAM
VDD	2.991	3.183
BL	3.084	0.292
BLB	0.329	3.925
WL	5.347	3.183
VSS	3.008	2.323
N12	0.239	12.673
N14	2.991	1.789
N15	2.991	3.323
N16	2.991	3.323

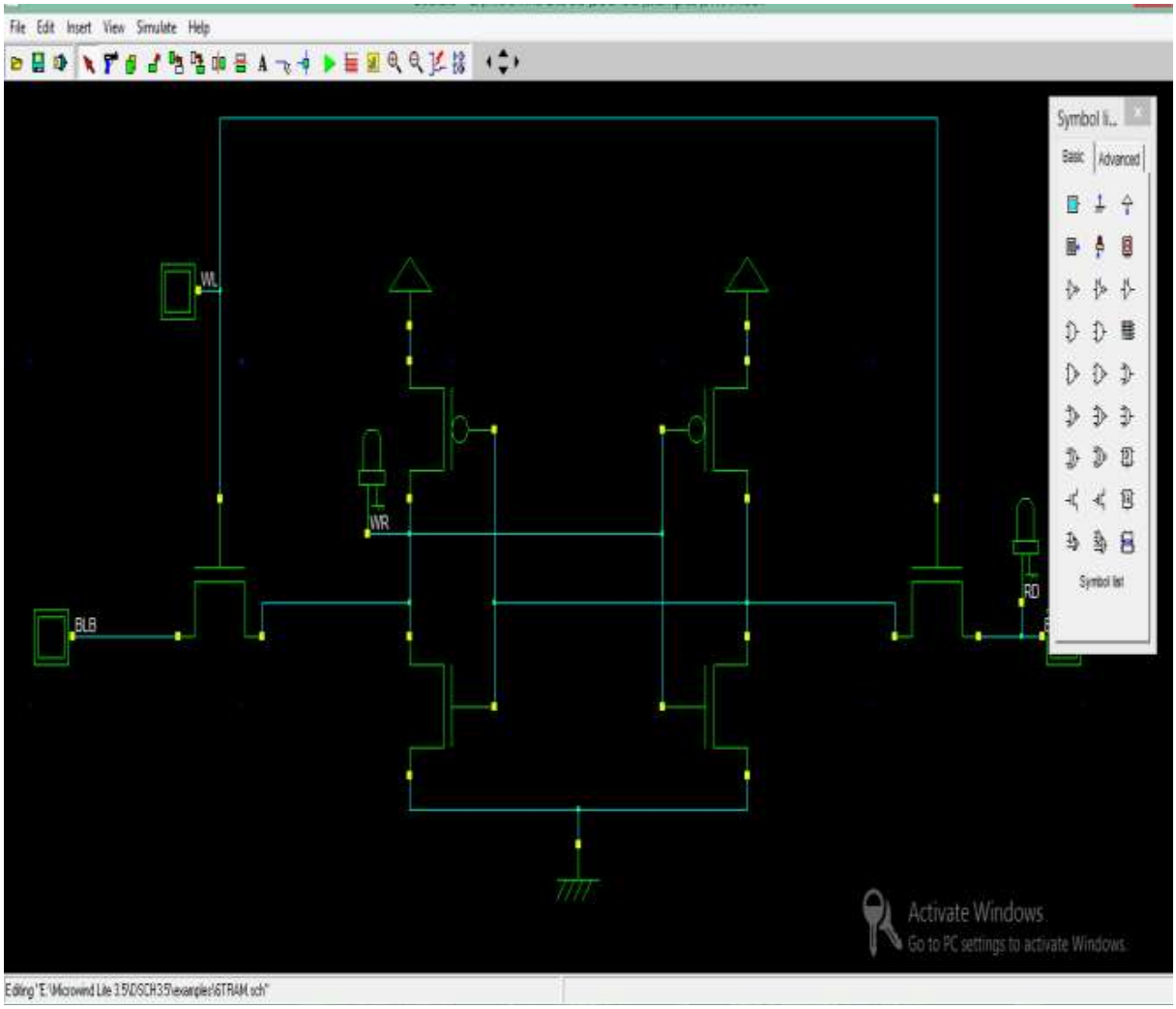

Fig 1: Schematic diagram of 6T SRAM

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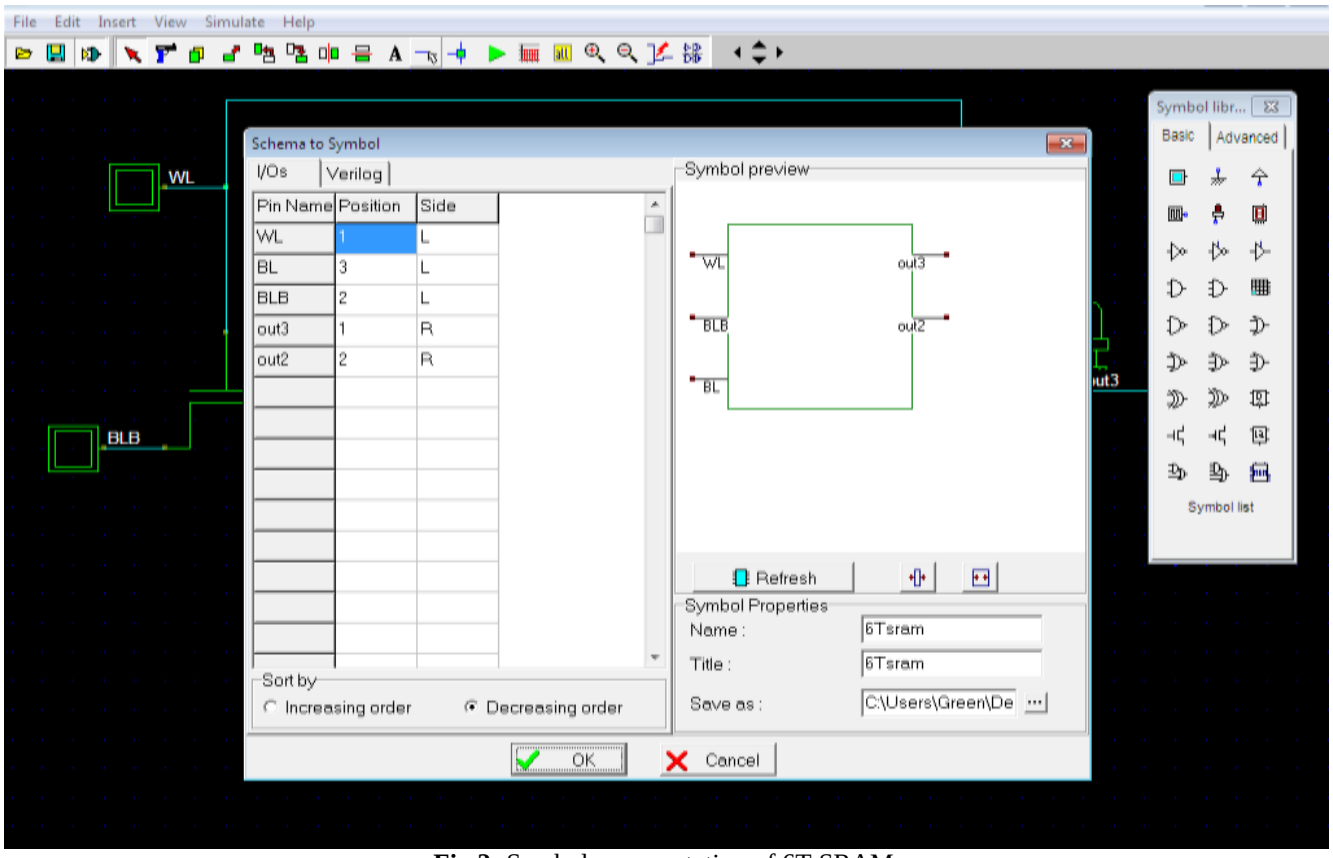

Fig 2: Symbol representation of 6T SRAM

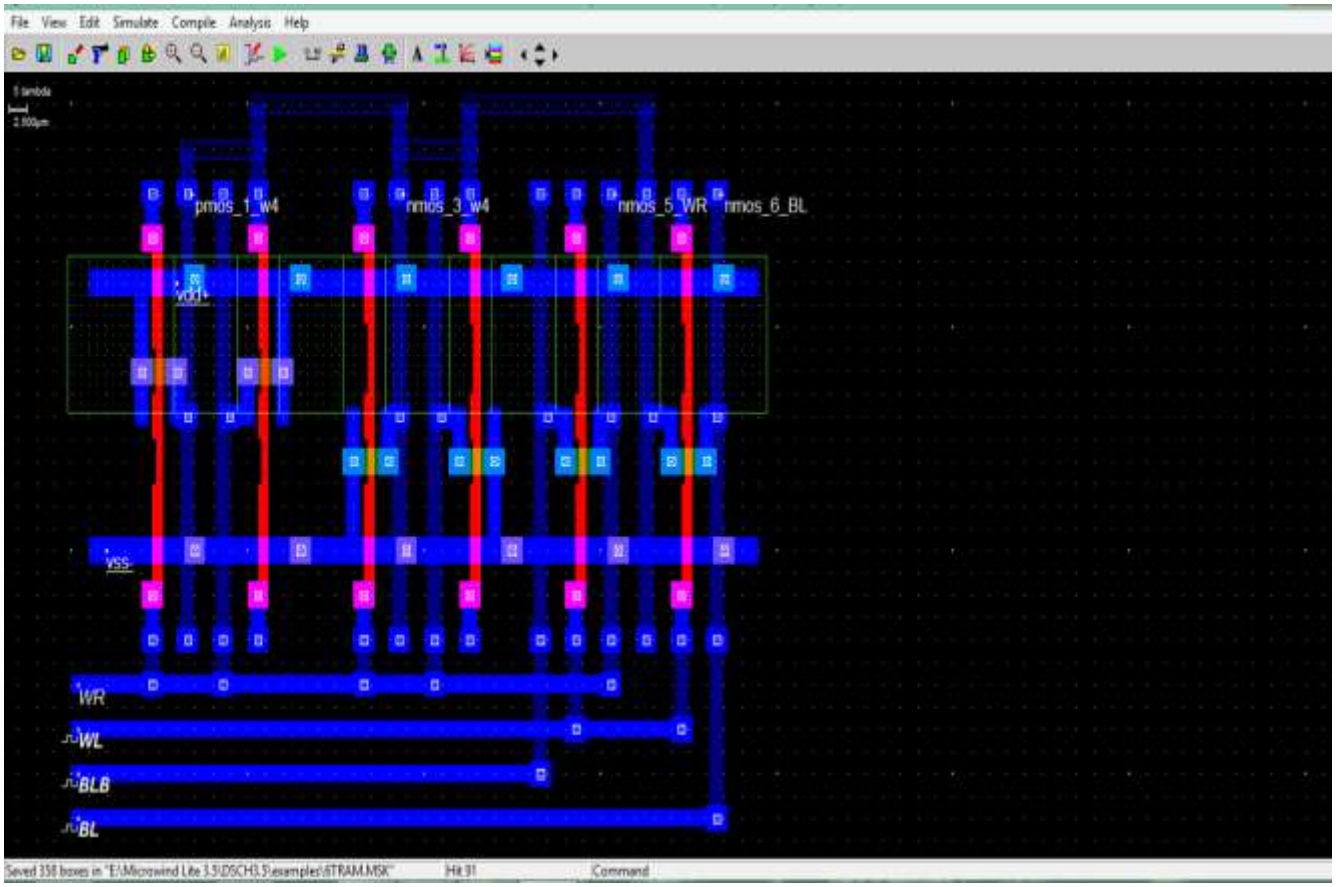

Fig 3: Layout diagram of 6T SRAM

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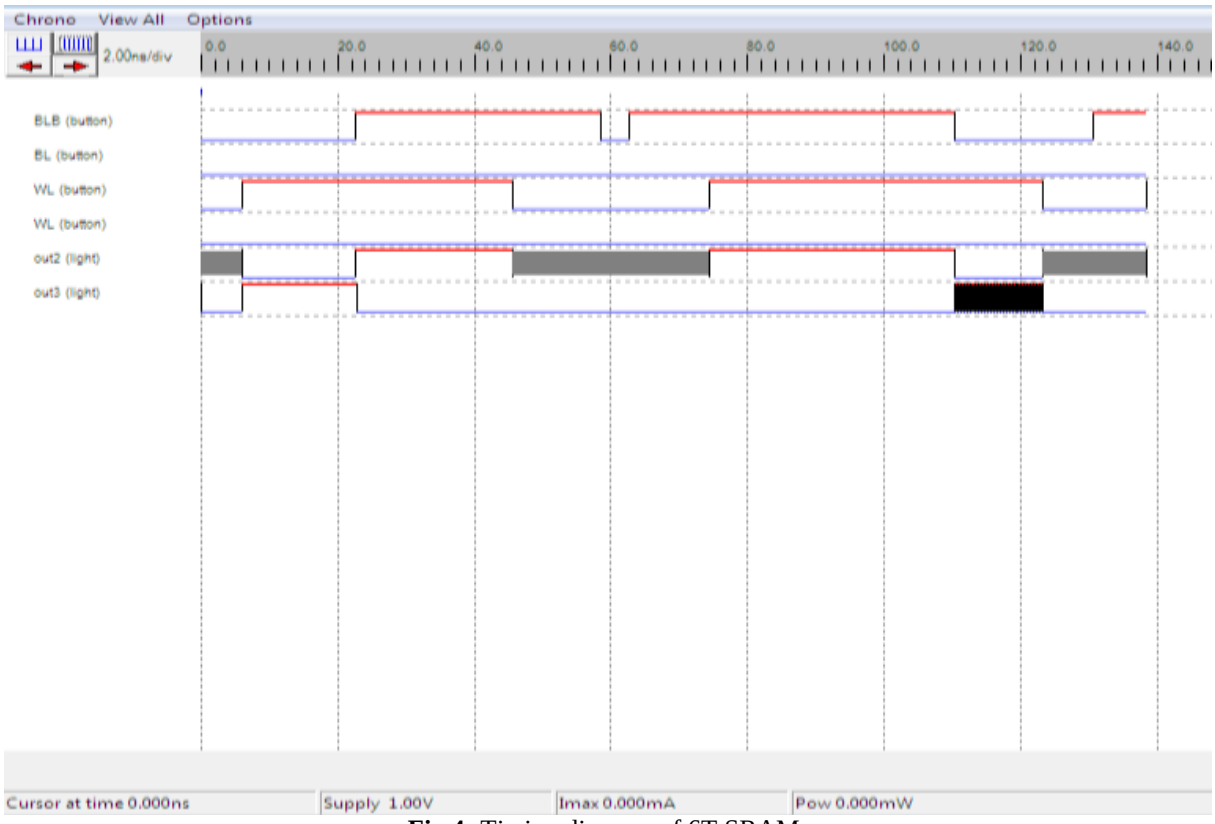

Fig 4: Timing diagram of 6T SRAM

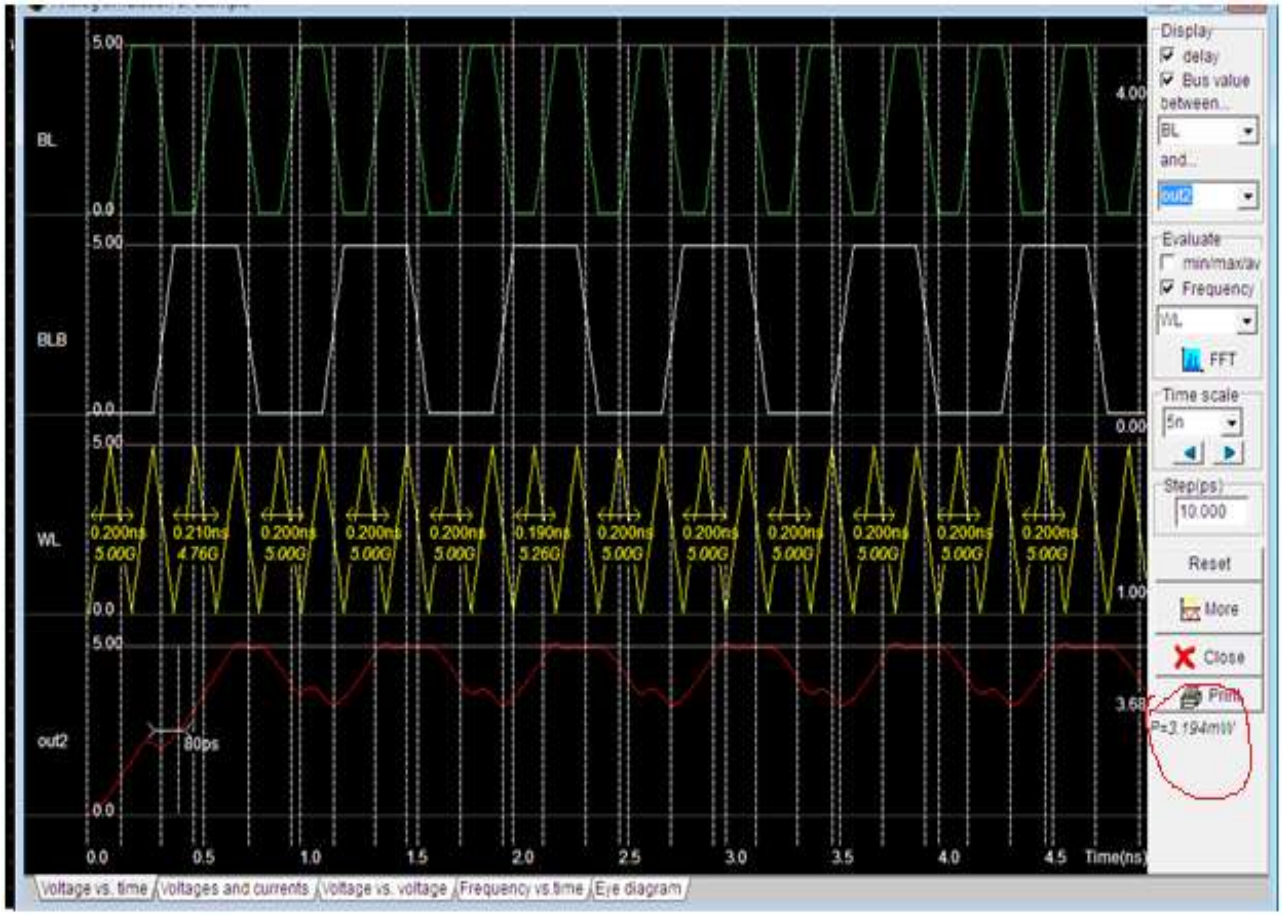

Fig 5: Analog simulation of 6T SRAM

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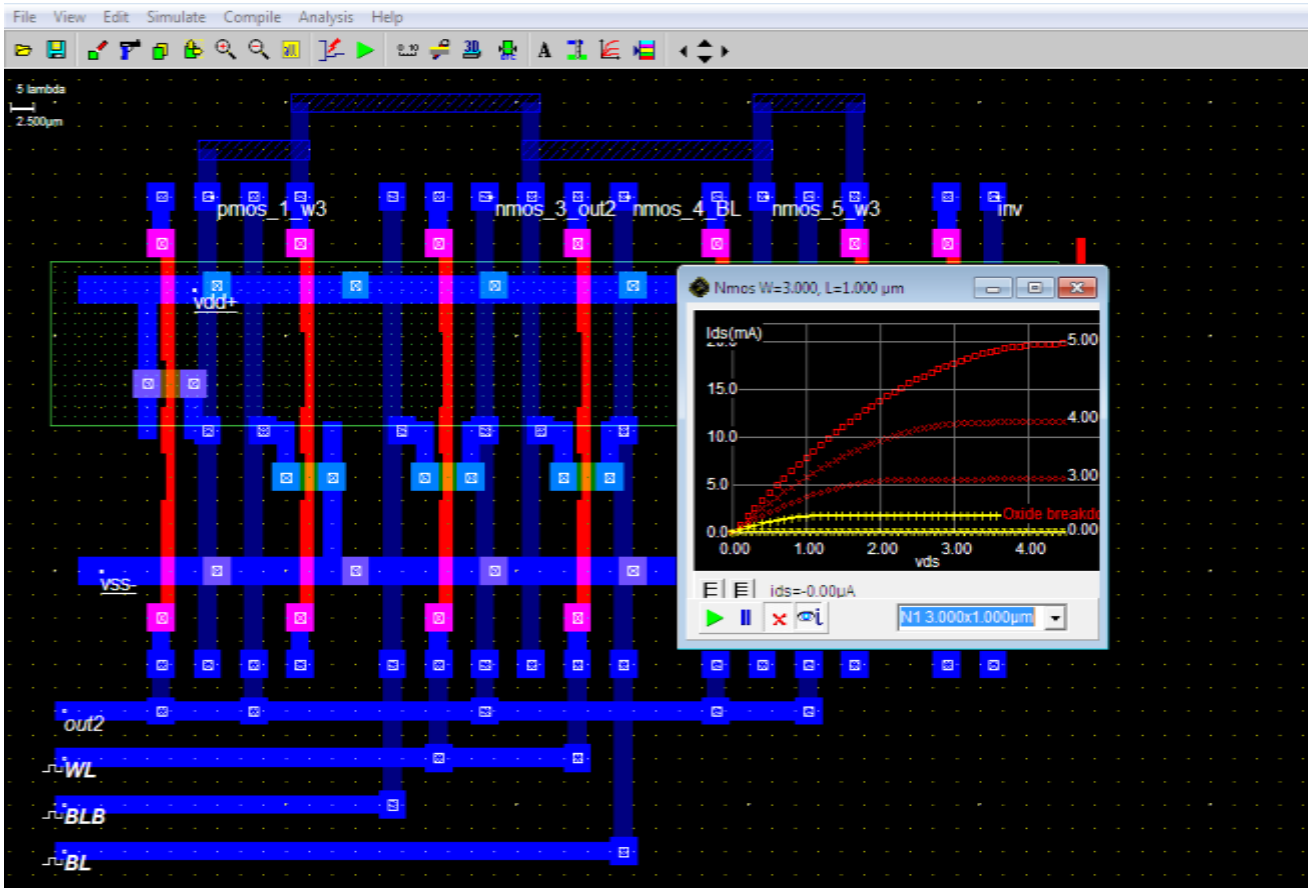

Fig 6: W/L ratio of 6T SRAM

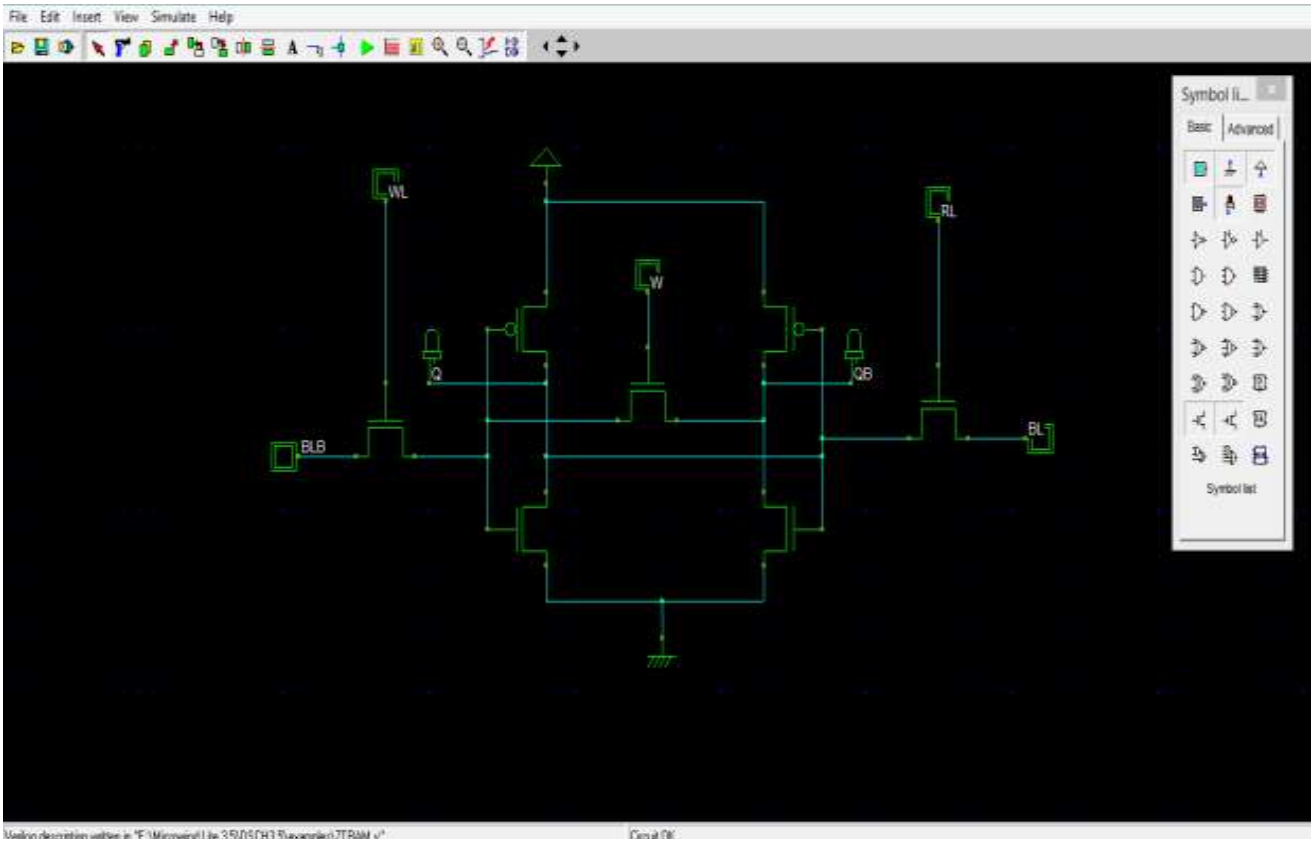

Fig 7: Schematic diagram 7T SRAM

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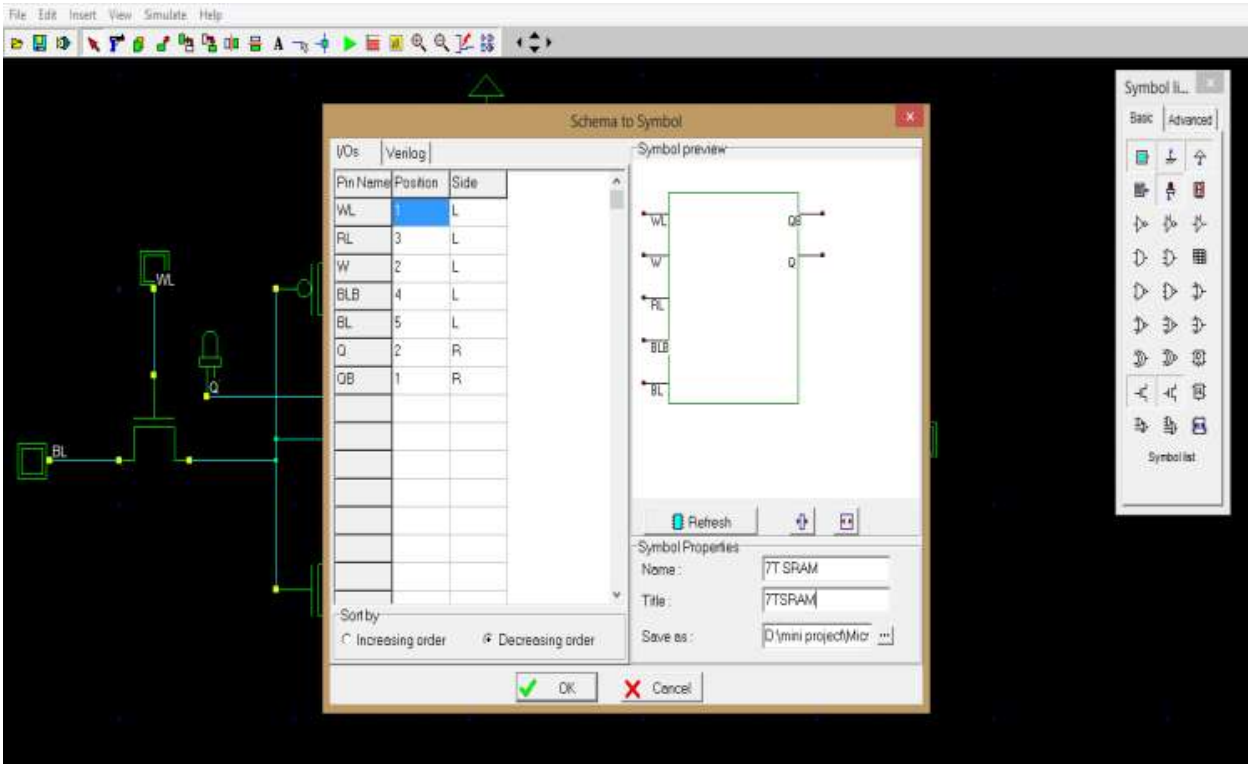

Fig 8: Symbol representation 7T SRAM

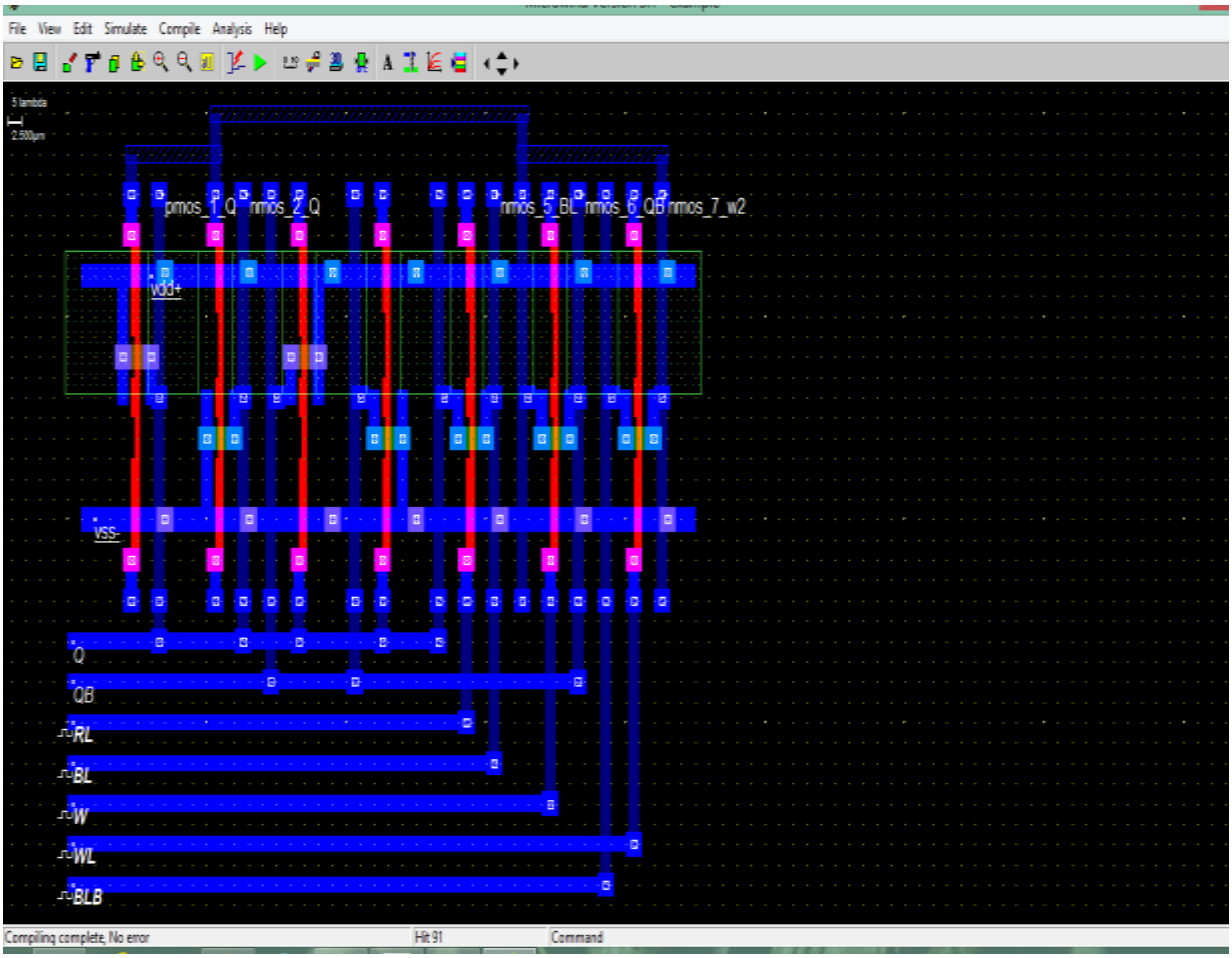

Fig 9: Layout diagram of 7T SRAM

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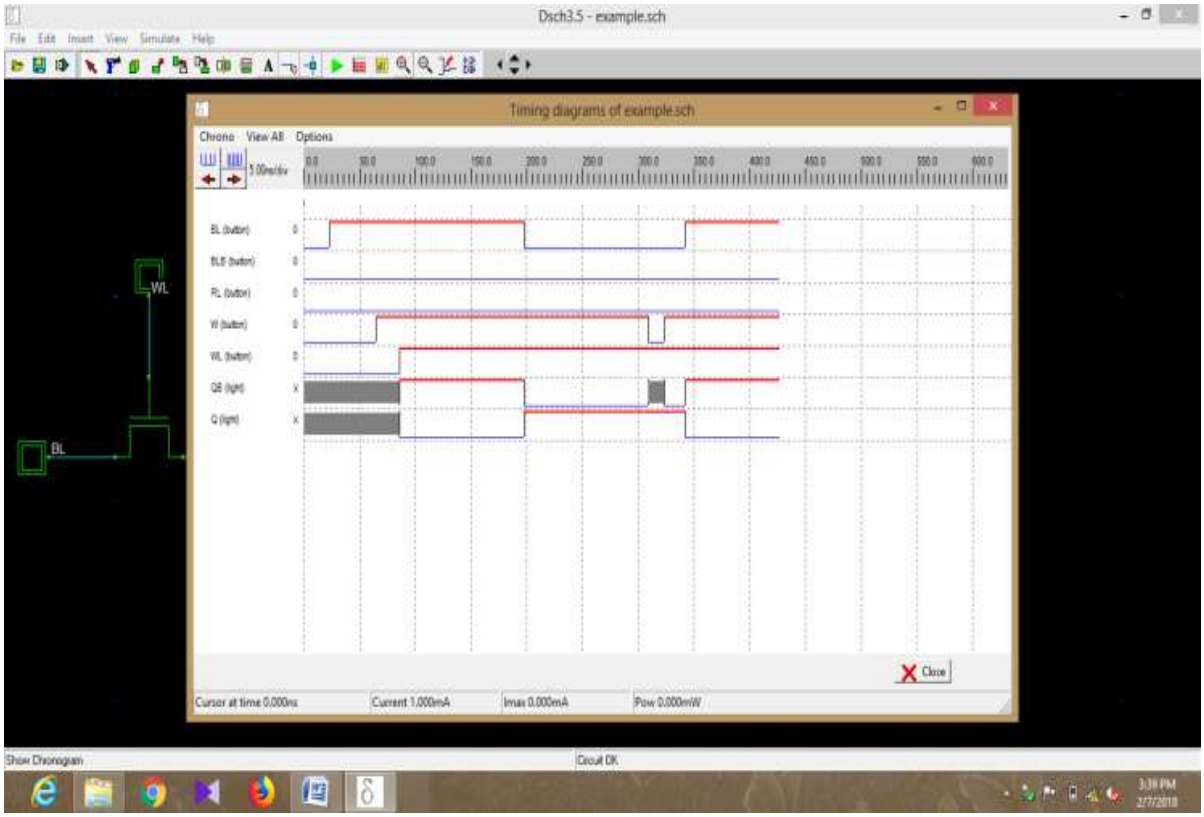

Fig 10: Timing diagram of 7T SRAM

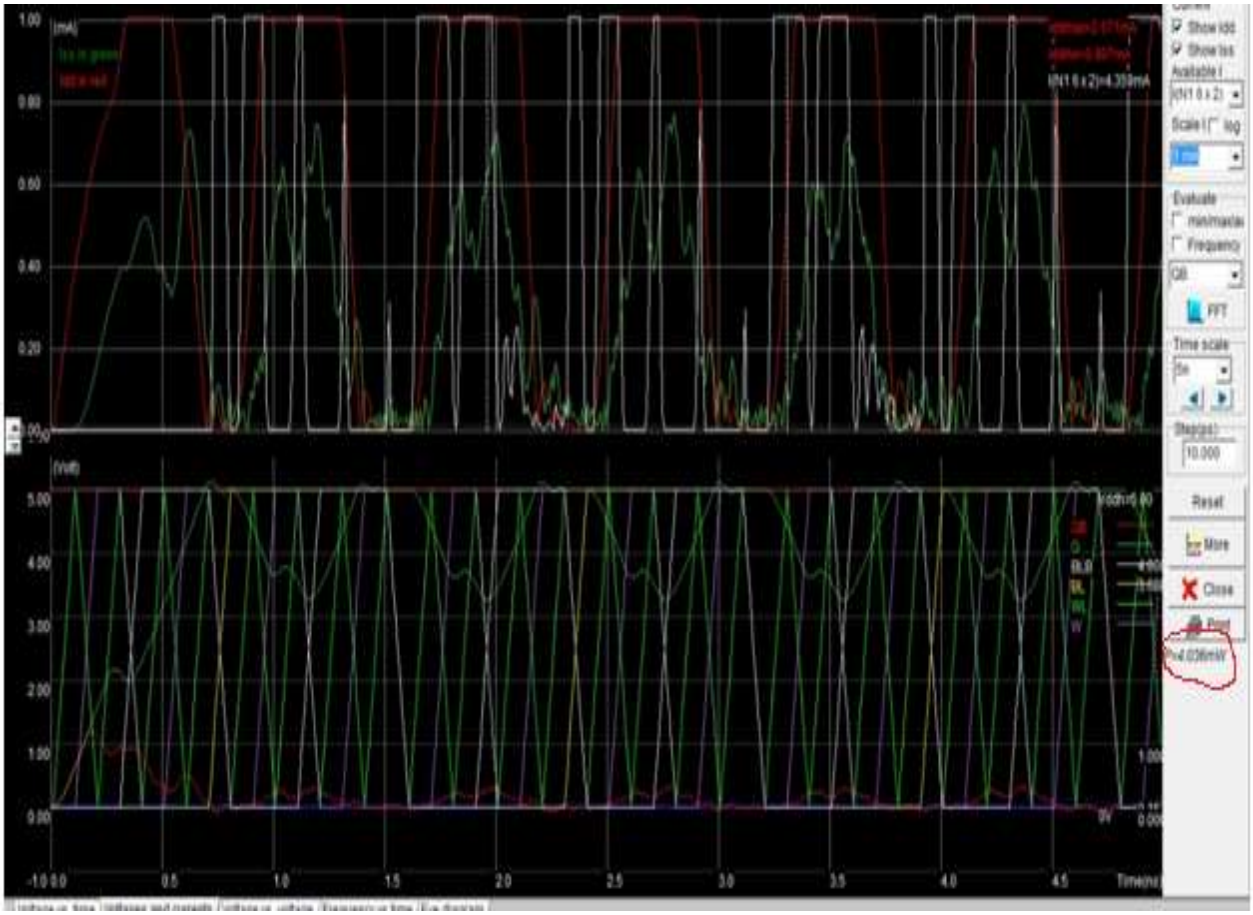

Fig 11: Analog simulation of 7T SRAM

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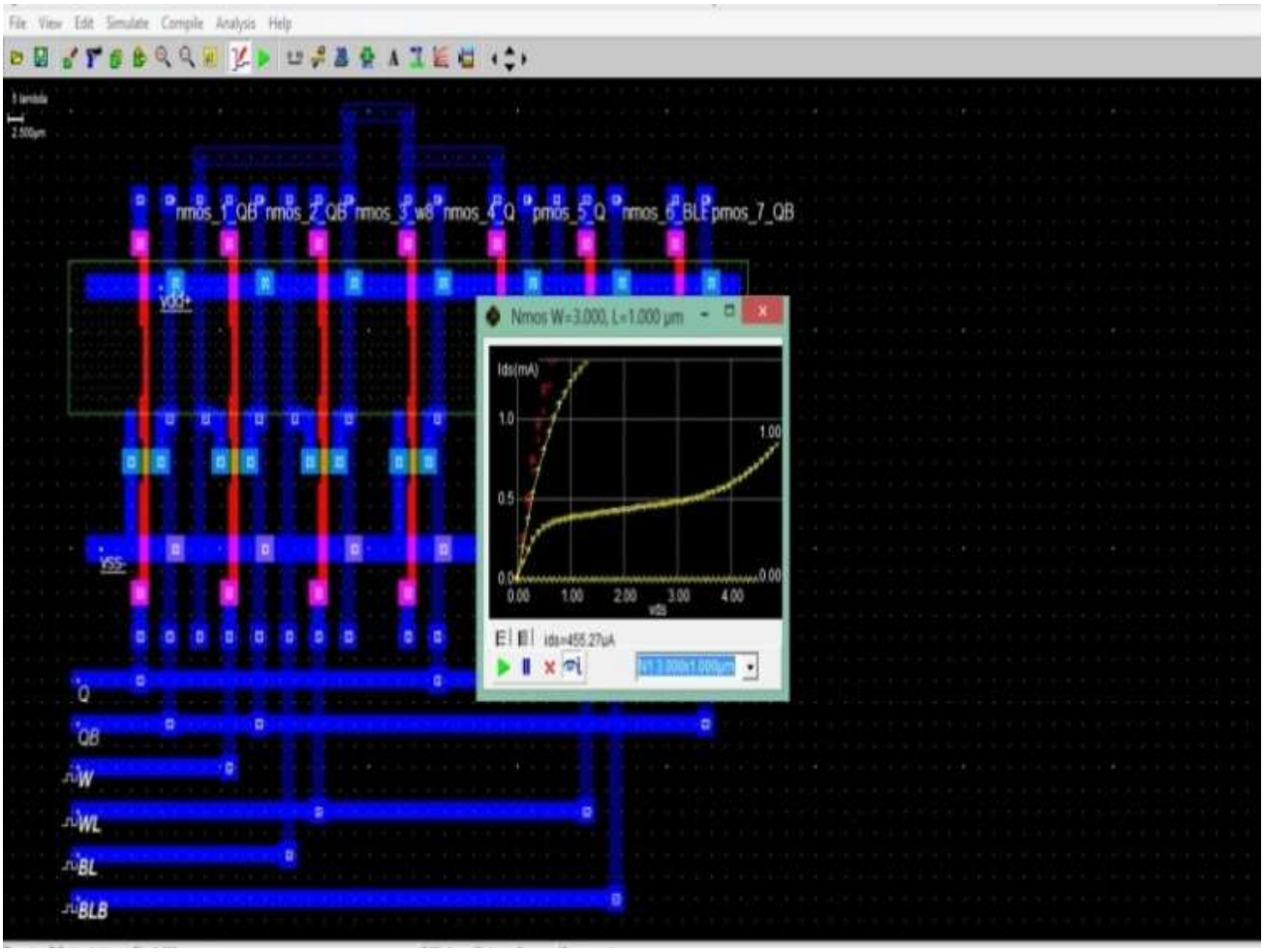

Fig 12: W/L ratio of 7T SRAM

5. CONCLUSION

In this paper power dissipation of 6T SRAM is compared with 7T SRAM. Simulation and analysis of 6T SRAM and 7T SRAM is desired. Simulation result shows clearly how read and write operation is performed. It is observed that the power dissipation is less as compared with 6T SRAM to the 7T SRAM in read as well as write mode of operation. In future, power dissipation will play a major role to reduced power consumption.

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BIOGRAPHIES

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