DIGITAL DESIGN AND SIMULATION OF CVSD CODEC ALGORITHM USING VHDL

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Abstract

Generally, digital signal transmission systems have important advantages over analog counterparts because noise dose not built up in cascading of repeaters. There is various digital transmission techniques like PCM, DM, DPCM, ADM etc. In this DM and ADM provides minimum transmission Bandwidth. DM provides slope overload error and granular noise in transmission so variation of step size is needed, which is provided by ADM. There is various algorithms in ADM technique like SONG algorithm, ABATE algorithm etc. one of the algorithm of ADM is CVSD algorithm. CVSD (continuous variable slope delta) modulation is an effective scheme for audio signal. CVSD is best coding technique for improving receiver sensitivity with low transmission rate as compare to PCM. Here in this paper, we discuss digital design of CVSD codec system using VHDL and simulation result is obtained at various data rates.

Keywords: *CVSD, DM, PCM, FPGA, ASIC, VHDL, BW, SIPO, PIPO, Verilog, RTL.*

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1. INTRODUCTION

Continuously variable slope delta modulation (CVSD or CVSDM) is an audio encoding method. It is a delta modulation with variable step size [4]. Due to variation in step size slope overload error is decreases as compare to delta modulation. The CVSD modulation is a technique of digitizing a band-limited audio signal. The CVSD modulator is many to one bit compression technique, which compresses the 8 bit into 1 bit or 16 bit into 1 bit or 12 bit data into one single bit. It is an lossy compression technique. The output of this 1-bit encoder is a serial bit stream, where each bit represents an incremental increase or decrease in signal steps amplitude. The continuously variable slope delta (CVSD) modulation is a nonlinear [1], sampled data, closed loop system which accepts a band-limited analog signal and encodes it into binary form for transmission in a digital channel. At the receiver, the binary signal is decoded into a close approximation of the original analog signal. Continuously Variable slope Delta Modulation is a simple s step adaptive DM method offering low hardware complexity, improved noise performance and minimum transmission Bandwidth [3]. It is an attractive alternative to more complex conventional analog to digital signal conversion techniques used in telecommunication and signal processing. To implement CVSD, There are few CVSD chip sets such as MC34115 from Motorola [2] but it works only at 16 kbps and it does not allow to add encryption to the algorithm, which is very important in defense systems for security purposes. Furthermore, to implement such algorithms with encryption possible, software (i.e. programming in DSP/GPP) and hardware (i.e. programming in FPGA or ASIC i.e. programming in VHDL or Verilog) approaches are available.

2. RTL SCHEMATIC OF CVSD CODEC IN QURTUS-II

The CVSD modulator consist an 8 bit comparator for comparing i/p signal with reference signal, 3 bit sipo(serial in parallel out) for detecting slope overload, 8 bit pipo(parallel in parallel out) for providing 1 clock cycle delay , overload detect and level select algorithm is used for selecting the variable step size. The present input compared with previous level selected output in 8 bit comparator. The comparator output is a digital encoded output which is 1 bit compressed output of 8 bit A to D input. Here shows the RTL view of CVSD TOP Module designed in altera quartus II.

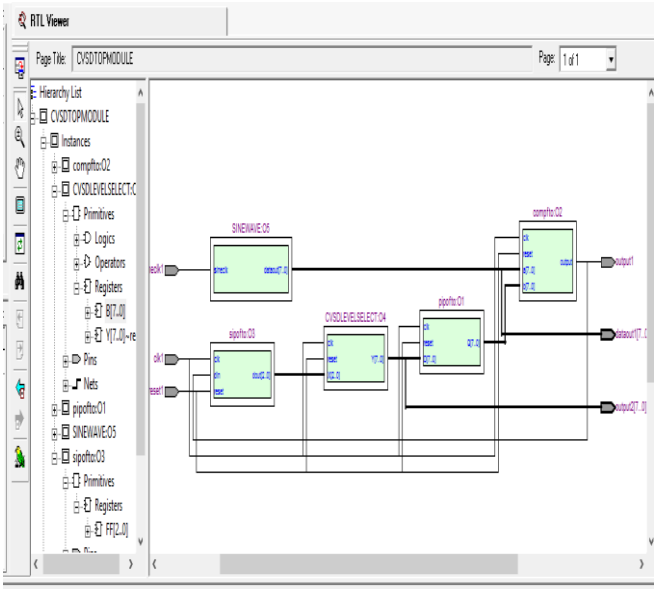

Fig-1.RTL view of CVSD top module

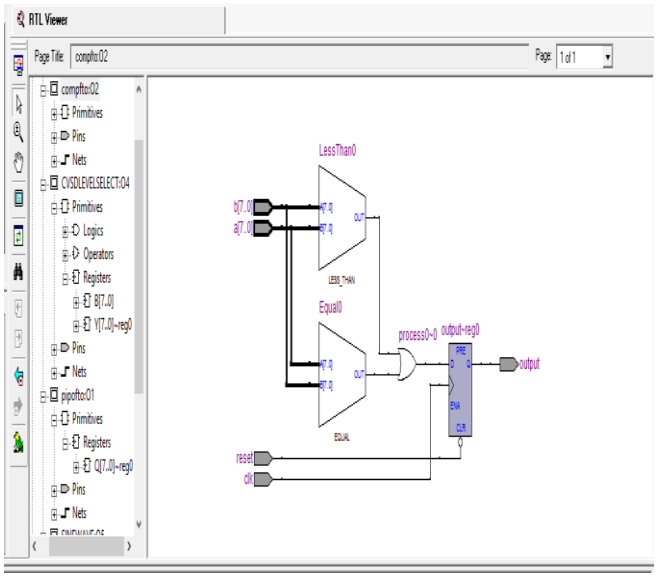

Fig-2 RTL view of 8 bit comparator

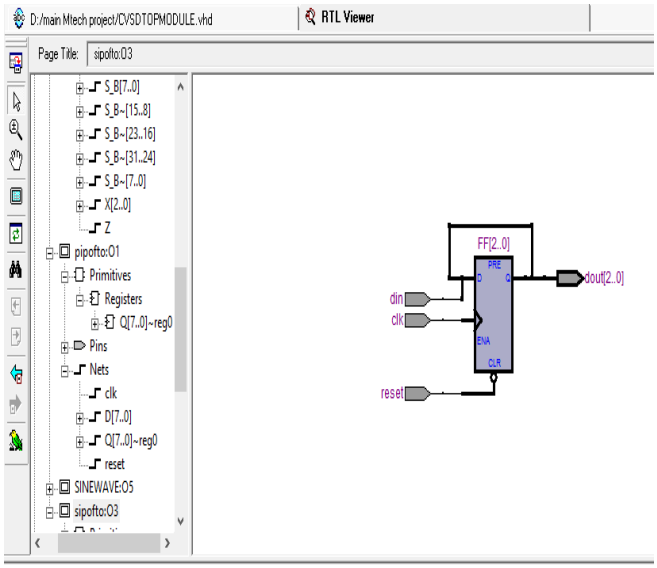

Fig-3 RTL view of 3 bit sipo register

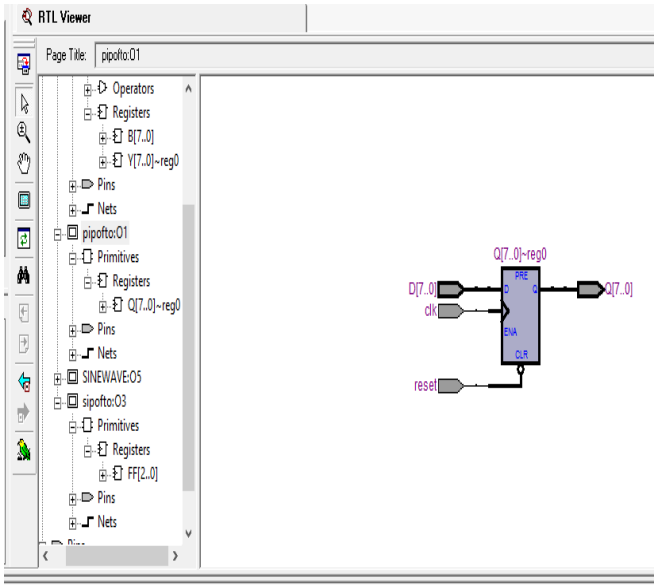

Fig-4 RTL view of 8 bit pipo register

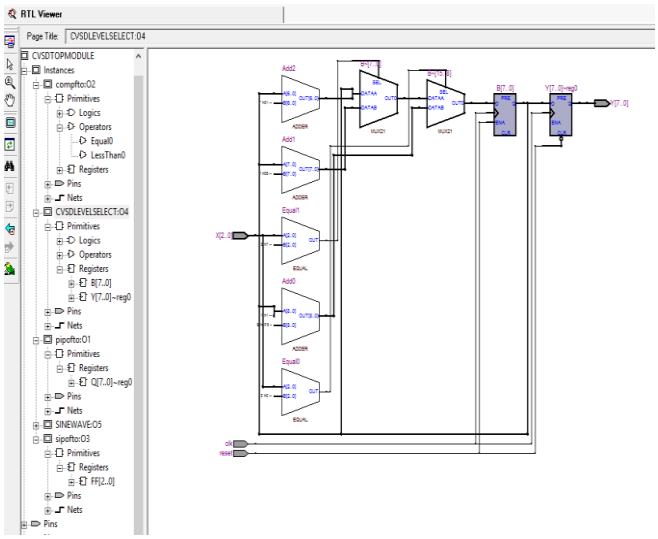

Fig-5 RTL view of CVSD level select module

The CVSD demodulator consist an 3 bit sipo(serial in parallel out) register, overload detect and CVSD level select as shown in figure 2. The 3 bit sipo take 3 bit digital input and then this input is checked by overload detect block, according to the digital input the step size level is selected by level select algorithm. The level select output is the 8 bit Demodulated output which is decompressed 8 bit output. The algorithm used in both the modulating side and demodulating side are same. Here above figure shows the RTL schematic of various modules created in quartus-II in VHDL.

3. CVSD ENCODER AND DECODER ALGORITHM

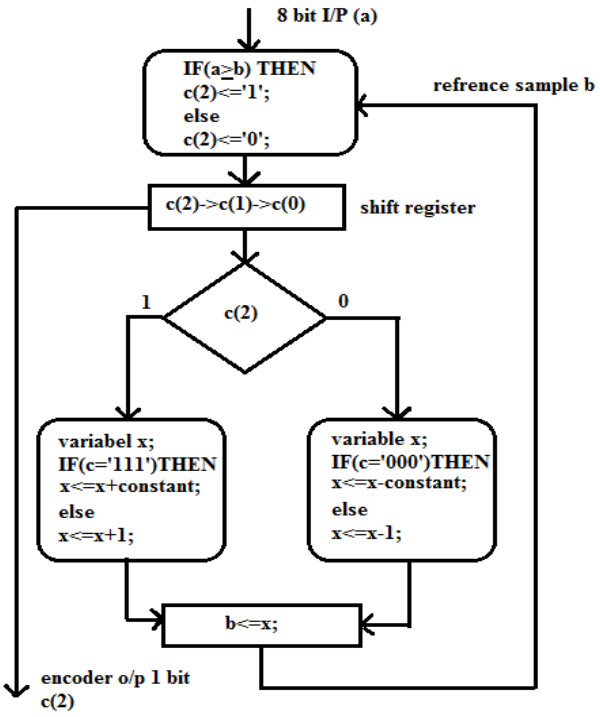

Fig-6 CVSD Encoder algorithm

Here Figure 6 shows the CVSD encoder algorithm. Here in this process in first step, the I/O 8 bit data is compare with the reference sample 8 bit magnitude. Then if the reference sample is less then I/P then output is '0' otherwise O/P of the comparator is '1'.In second step the output of comparator is input of 3 bit shift register. Here the MSB bit output of shift register is encoded 1 bit output, which is 8 to 1 bit compressed output. In the step 4, the reference sample 'b' is taken from CVSD level select algorithm. Here if shift register output is 111 or 000 then the slop of the input signal is continually increasing or continuously decreasing respectively, so reference output b is increased or decreased by an arbitrary constant value (i.e. Increment of step size). Otherwise increment or decrement by one step.

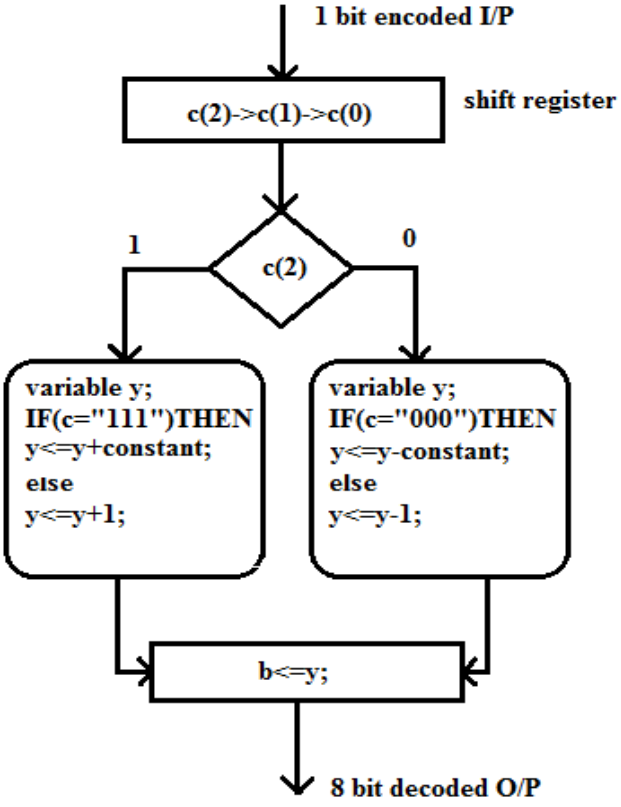

Fig-7 CVSD Decoder Algorithm

Here Figure 7 shows the CVSD decoder algorithm. In first step, encoder one bit output is input of 3 bit serial in parallel out shift register. If sipo register contain "111" or "000" then decoder analysis that there is continuously increment or decrement in slope of the input signal. So step size is increases or decreases by an arbitrary constant respectively. Otherwise increment or decrement by one step.

4. SIMULATION

Here in figure 8, 9 and 10 shows the waveform simulation at various data rates,
Sampling rate of input signal =1/(400×30) = 83.33µs
i/p signal frequency = 400Hz
grid size = 83.33 µs

Clock rate for 16kbps = 1/(1024×16)=61.035 µs
Clock rate for 32Kbps =1/(1024×32)= 30.51 µs
Clock rate for 32Kbps =1/(1024×64)= 15.25 µs

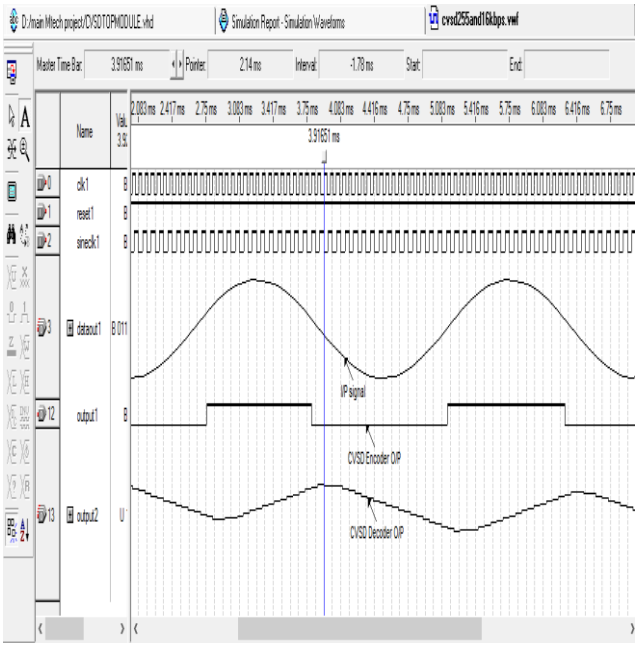

Fig-8 CVSD waveform simulations at 16 kbps data rate

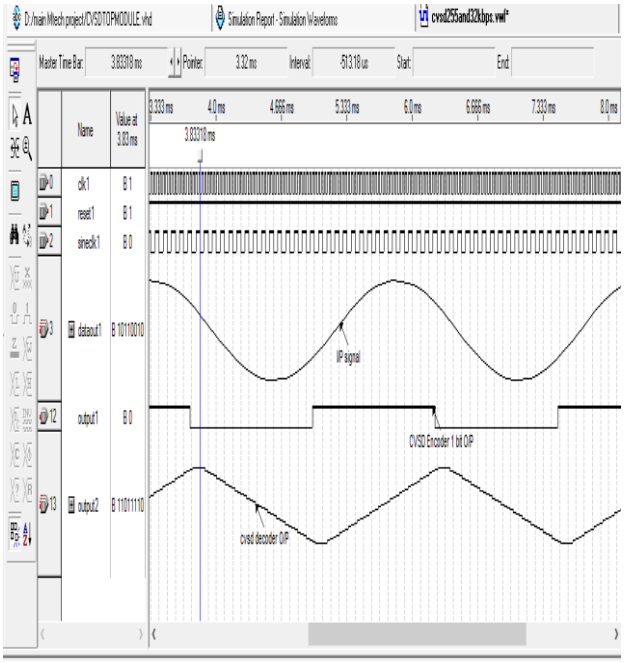

Fig-9 CVSD waveform simulations at 32 kbps

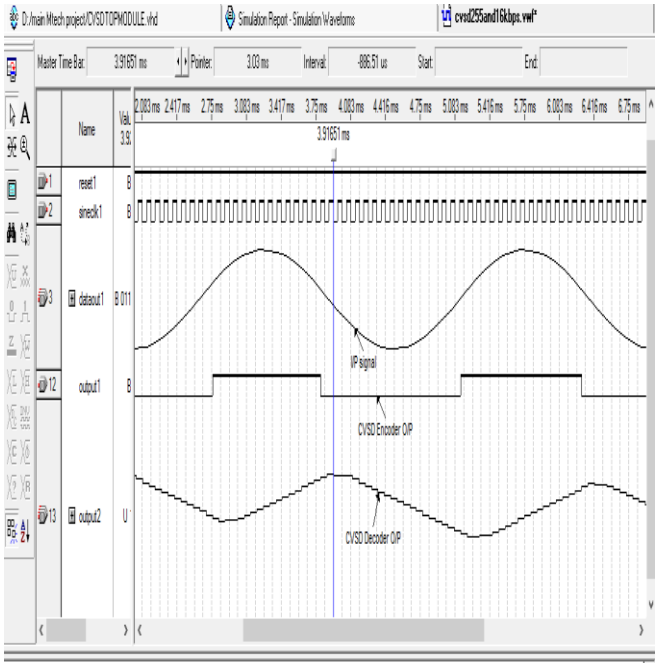

Fig-10 CVSD Waveform simulations at 64 kbps data rate

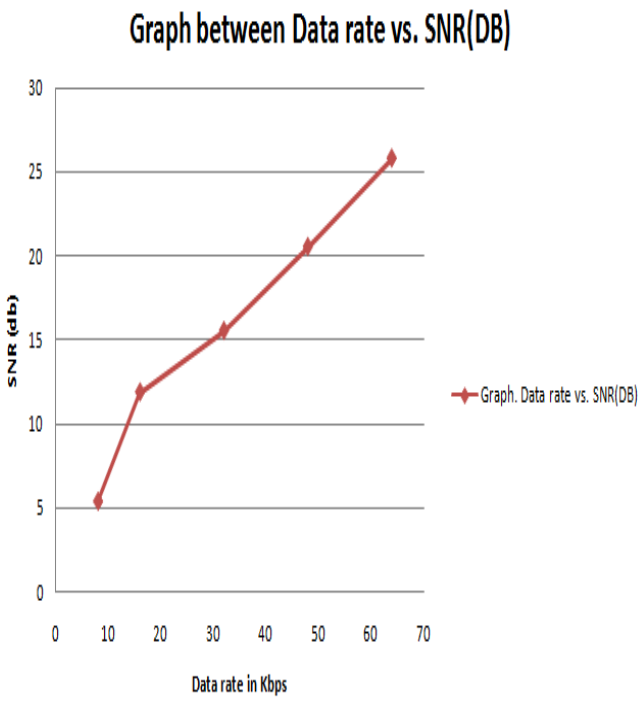

Fig-11 Graph between SNR vs Data Rate

Table-1 Data rate Vs SNR

Data Rate (kbps)	SNR(db)
8	5.367
16	11.8892
32	15.5511
48	20.5544
64	25.824

Here in above graph shows that by increasing the data rate SNR of cvsd is increases. The SNR calculation at different data rate is done by the following formula at sampling rate 83.33 µs.

$$SNR = 10\log_{10}\frac{variance\ (Input)}{variance(Output - Input)}$$

(or)

$$SNR = 10\log_{10}\frac{\sum_{n=1}^{N}(x_n)^2}{\sum_{n=1}^{N}(x_n - \hat{x}_n)^2} \quad \text{.....[7,8]}$$

$\{x_n\}$ → samples of original signal (speech signal)

$\{\hat{x}_n\}$ → samples of final reconstructed signal

5. CONCLUSION

Here, I described a brief introduction to continuous variable slope delta modulation and Algorithms of CVSD Encoder and Decoder. The main benefit of CVSD is that it reduces the slope overload error as compare to Delta Modulation because of step size is continuously changeable by CVSD algorithm. It is most efficient lossy compression technique for voice coding and decoding with less error. The CVSD codec eliminate the need of complex framing because of one bit encoding (i.e. compression from 8 bit to 1 bit and Decompression of 1 bit to 8 bit).

Here I also described the various SNR in DB at different data rates in kbps. As we increases the data rate of cvsd codec the SNR of the output is increased.

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