PERFORMANCE ANALYSIS OF ULTRA LOW POWER MCML BASED VCO DESIGN

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Abstract

Power has always been a concern due to the adaptation of technology scaling. Power mitigation techniques needs to be adopted. Due to the advancement in VLSI design, the ultra low power designs have acquired a great importance. The subthreshold design has proven to be a boon for ultra low power applications. The paper explores the operation of voltage controlled oscillator design. The VCO is designed using MOS current mode logic style. Further, the performance analysis is carried out and the design is compared with the conventional current starved VCO. It is found that the VCO design provides improved phase noise margin of about -16.2dbc/Hz. The temperature and power supply sensitivity of the design has also been carried out. It is found that the supply sensitivity is reduced to 0.054GHz/V.

Keywords—*Current starved; Sensitivity.*

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1. INTRODUCTION

The VLSI design has always played a vital role in the field of digital signal processing, automation, robotics etc. The ultra low power design is the most recent trend in VLSI. Since power reduction the main objective behind adopting the ultra low power design. The ultra low power design exhibits various various characteristics such as high performance, high speed and low power operations. The CMOS technology have always been a boon to the VLSI area. The design of CMOS using MOS current mode logic concept has gained a lot of importance. The operation of MOS current mode design exhibits a lot of importance due to its various advantage over the conventional CMOS. Some of its advantages includes high speed, high performance, and stability. Hence, using such design a voltage controlled oscillator can be designed.

Voltage control oscillator is the main component in various circuitry such as digital circuits, timing circuits, radio receivers, PLL etc. The voltage control oscillator operation depends on various parameters. Some of the parameters are tuning range, phase noise, supply sensitivity etc. These factors decides the performance of the given voltage controlled design. The performance of VCO is degraded due to power supply noise. Ring oscillator is greatly affected by such power supply noise. There are various VCO metrics that gets affected due to noise. Hence, there is a need to design a robust system that can counter balance the variations caused by the power supply noise. There are various techniques that can be adopted in order to reduce supply sensitivity.

A lot of techniques can be adopted like using a D flip flop at the output stage. Some techniques involved designing a VCO along with a source follower instead of dc current source. This paperdepicts a technique of implementing a VCO using mcml logic design with low supply sensitivity as proposed by the author in [20].Further, the performance analysis is carried out using various VCO design parameters. The VCO design is then compared with the conventional current starved VCO. In section II, MOS current mode logic design technology is explained. In section III, the voltage controlled oscillator design based on MCML is explained. In section IV, the performance comparison is carried out. In section V, the conclusion is drawn out.

2. MOS CURRENT MODE LOGIC DESIGN

Fig.1. shows the basic MCML buffer logic style. The current mode logic style consist of driven and the driver elements. The PMOS acts as a linear resistor. The NMOS works as a switch. The switching operation is controlled by the current present in the NMOS which at the tail of the circuit and hence the design is called as MOS current mode design. Such a design enables fast switching operation.

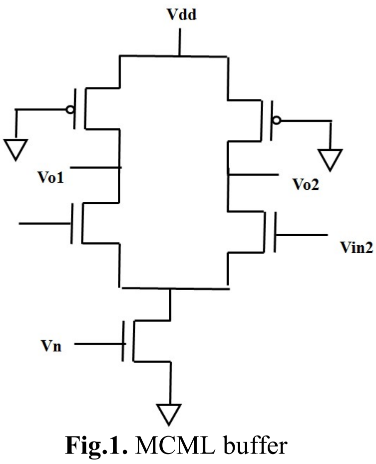

Fig.1. MCML buffer

MCML has numerous applications like multi GHz communication system, High speed cross point switches, high speed buffers, mixed signal applications, RF applications. Hence, MCML design based VCO will prove to be a great design.

3. THE VOLTAGE CONTROL OSCILLATOR DESIGN BASED ON MCML LOGIC

The voltage control oscillator can be termed as the oscillator whose out frequency is controlled by the voltage applied to it. The frequency of operation and the range of it is decided by the voltage applied to it. The frequency of ring oscillator is given as

$$fos \quad 1/(\ 2*n*d) \qquad (1)$$

where$n$=number of stages
td= time delay

VCOs can be made to oscillate from few Hertz to hundreds of GHz. VCO plays a very vital role in many applications. A high frequency VCO is used in devices like processor clock distribution and generation, system synchronization and frequency synthesis. The application of VCO are electronic jamming equipment, function generator, production of electronic music.VCO can be designed by the logic style MCML by using the buffer as show in Fig.1. This buffer can be used for designing VCO. Ring oscillator is cascaded combination of delay stages, connected in a close loop chain. Hence, a 4-stage ring oscillator using MCML logic is implemented by cascading the buffer. The performance of the VCO design can get affected due to the presence of noise component in the power supply. In order to overcome this interference, the cascaded MCML based buffer is interpolated with one more stage that helps to counter balance the noise effect.

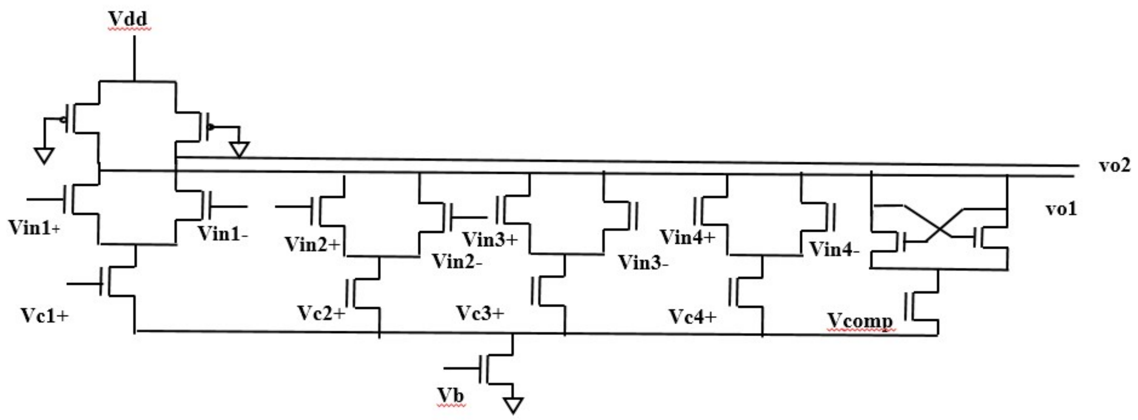

Fig.2 Compensated stage interpolated to the ring oscillator. [20]

Resonator such as capacitance and inductor will oscillate continuously if no resistive element is present to dissipate the energy. So, there is a need to generate a negative resistance and maintain oscillation by supplying an equal amount of energy equal to that dissipation. There are circuits which exhibit negative resistance where positive small signal voltage exhibit a negative small signal current. Such circuit can be built by either in series or parallel with positive resistor of same magnitude. Since, positive resistance consume power, the negative resistance must produce signal power to compensate. Such resistance does not exist but have to design it. That means MOS can operate as a negative resistor. Such negative resistance concept is used to compensate the signal loss. The cross coupled pair as shown in Fig.2 provides the negative resistance.

The performance comparison is carried out by inducing noise of 10MHz frequency. The performance comparison is done between the 4 stage ring VCO and then the interpolated 4-stage ring VCO and both the design is compared with the conventional current starved VCO design.

4. PERFORMANCE ANALYSIS

Initially, the performance of 4-stage CML ring oscillator is analyzed in the presence of power supply noise. Fig.4. shows the tuning range of 4-stage CML ring oscillator. The tuning range is calculated by varying the control voltage Vn and measuring the frequency of oscillation. The tuning range should be as wide as possible so that oscillator can be tuned to a wide range of oscillating frequencies.

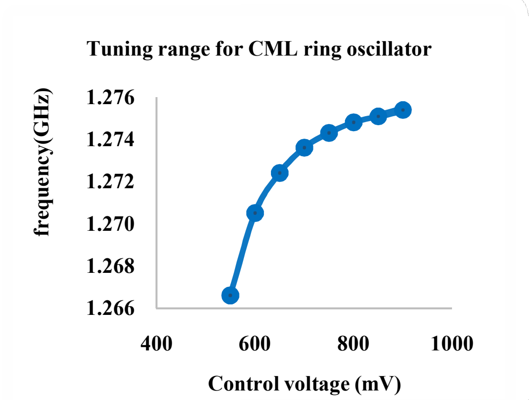

Fig. 3 Tuning range of 4-stage CML ring oscillator

Fig.3 shows that the tuning range of 4-stage CML ring oscillator. Secondly, the performance of compensated 4-stage ring CML oscillator is evaluated with the addition of power supply noise. Fig.5 shows the tuning range of compensated 4-stage CML ring oscillator. The tuning range of the compensated ring oscillator is obtained by varying the voltage levels of the tail NMOS transistor. The voltages are varied from -200mV to 200mV. This range is the difference of vc1+ and vc2+ so as to get full swing as per CMOS standard voltage level.Fig.4 shows the tuning range plot of compensated CML ring oscillator.

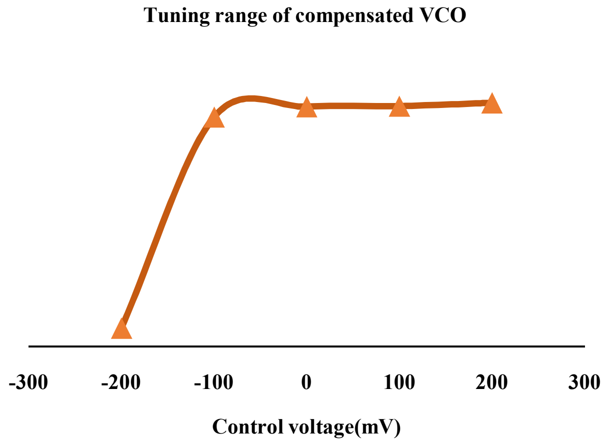

Fig.4 Tuning range of compensated ring

The tuning range is plotted as shown in Fig.4.The tuning range obtained is 1.17-1.1185GHzwhile the conventional cml ring has only 1.266-1.2754 GHz. Therefore, compensated ring VCO has wide tuning range. Similarly, the sensitivity of both the oscillators has been compared. The performance comparison of both the oscillators is done with the conventional current starved ring oscillator. Further, the variation of frequency with temperature is examined and is tabulated in Table I.Similarly, the comparison of phase noise of both the VCOs was done at an offset of 10MHz. The phase noise plot for CMLVCO is as shown in Fig.5 a) and the phase noise plot for compensated CML VCO is plotted in Fig.5 b).

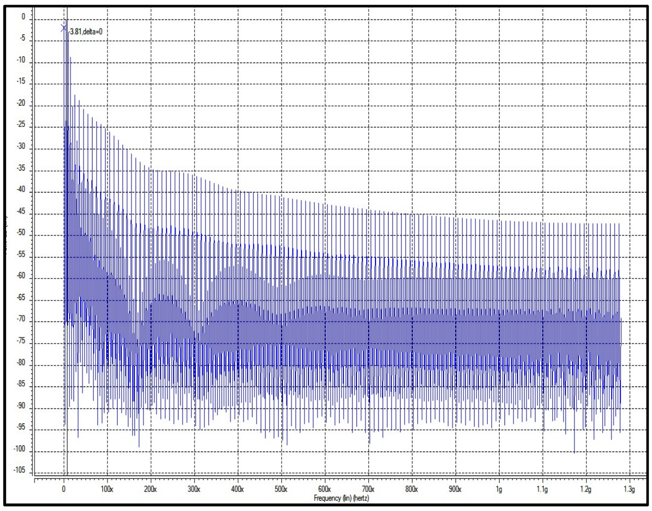

Fig.5 Phase noise plot for a)CML ring VCO

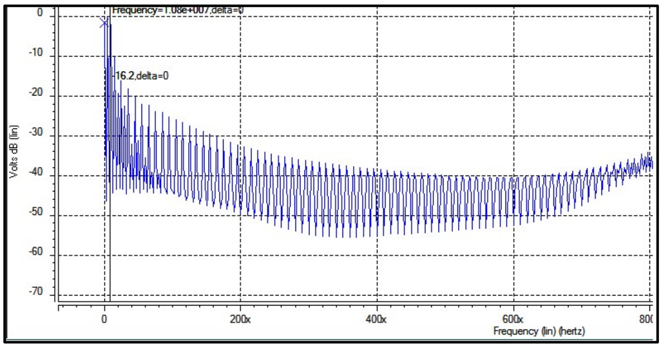

Fig.6 Phase noise plot for a) compensated VCO

The compensated phase noise is about -16.2dbc/Hz at an offset of 10MHz.While, the phase noise of the CML VCO is about –3.81dbc/Hz. Next, the temperature sensitivity and supply sensitivity of both the VCO were compared with the conventional current starved CMOS ring VCO.Fig.7 shows the comparison of temperature sensitivity of the CML ring, compensated VCO and the current starved VCO.

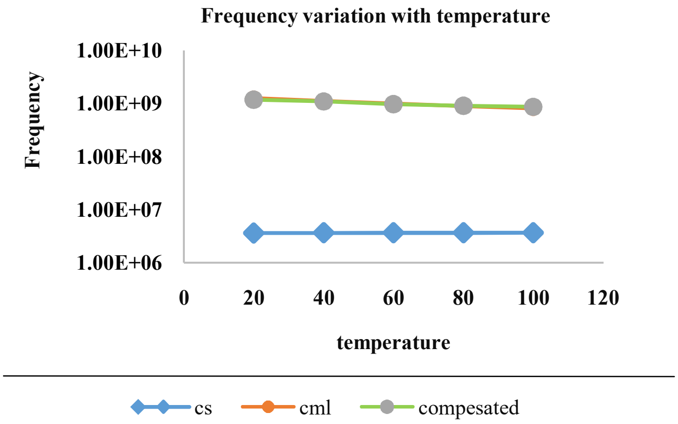

Fig.7 shows the plot of temperature sensitivity of CML ring, compensated ring and current starved VCO.

It is found that the temperature sensitivity of CML ring and compensated is almost same. The temperature variation is tabulated in table I

Table 1: Comparison Of Frequency Variation With Temperature Of Vcos

Temperature	CML ring(GHz)	Compensated (GHz)	Current starved (MHz)
20	1.266	1.1794	3.628
40	1.1252	1.105	3.63
60	1.00	0.9739	3.649
80	0.9004	0.907	3.65
100	0.818	0.874	3.681

The temperature variation in CML ring is about 35% while that in compensated CML VCO is reduced to about 25.8%. Further, the supply voltage was varied and the sensitivity was calculated for all three designs. Fig.8. shows the plot of supply sensitivity comparison.

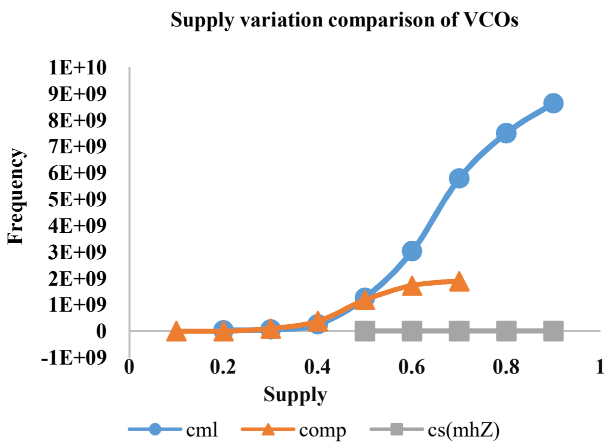

Fig.8 shows the plot of supply sensitivity of CML ring, compensated ring and current starved VCO.

The CML ring VCO is highly susceptible to the supply variation. The supply sensitivity calculated is about 0.176GHz/V. The compensated VCO has low sensitivity of about 0.054GHz/V. The performance comparison is carried out and tabulated in table II.

Table 2: Performance Comparison Of CML Ring, Compensated Ring And Current Starved Ring Oscillators.

Parameter	Current starved	CML ring VCO	Compensated VCO[20]
fosc	3.63MHz	1.266GHz	1.17GHz
Average power	2.3169uW	0.588mW	0.17682mW
Tuning sensitivity	0.38MHz/V	0.74GHz/V	0.85GHz
Tuning range	3.627-3.62MHz	1.266-1.27GHz	1.17-1.118GHz
Phase noise	-15.4dbc/Hz	-3.81dbc/Hz	-16.2dbc/Hz
Supply sensitivity	0.013MHz/V	0.176GHz/v	0.0546GHz/V
Temperature variation	1.4%	35.38%	25.8%

The performance comparison table shows that the tuning range of the compensated 4-stage CML ring oscillator is moreas compared to the conventional current starved oscillator. The tuning range obtained for 4-stage CML ring oscillator is only 1.266-1.2754GHz. The current starved provides a tuning range of 3.6275-3.6283MHz.The supply sensitivity of 4-stage CML ring is 0.176GHz/Vand for current starved it is about 0.013MHz/V.This compensation circuit stage provides a low supply sensitivity as compared to the CML ring oscillator. The supply sensitivity obtained is about 0.0546GHz/V.The compensated 4-stage oscillator provides low sensitivity to supply variation while maintaining same oscillatory frequency. The average power is also low of about 0.17682mW for the compensated VCO than CML ring VCO.

The variability is an issue in the design of various technology. The three main component for variability are process, voltage and temperature. When the CMOS is scaled, the effect called random dopant fluctuation is caused. This affects the threshold voltage and voltage swing. Eventually, this causes changes in voltage rise and fall time. This variation causes fluctuation in frequency. Hence, there is a need to encounter this problem. The variability test of the VCO was investigated under PVT variation. The parameters were varied and the effect of PVT variation on the frequency of the VCOs was studied. The probability density function was plotted for all the VCOs and compared. Monte Carlo analysis was carried out for 30 runs and variation in the frequency was noted.

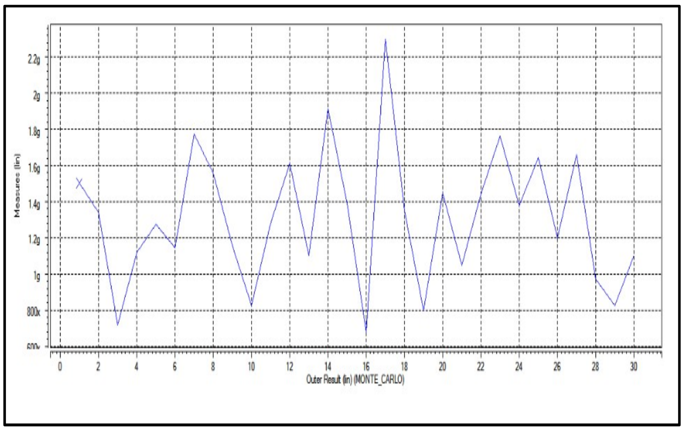

Fig.9 Variation in frequency for 30 runs for CML ring VCO.

Fig.9 shows the variation in frequency for 30 runs using Monte Carlo simulation and it was found that frequency varies from 600MHz-2.2GHz. The variation in frequency is about 1.6GHz for CML VCO.

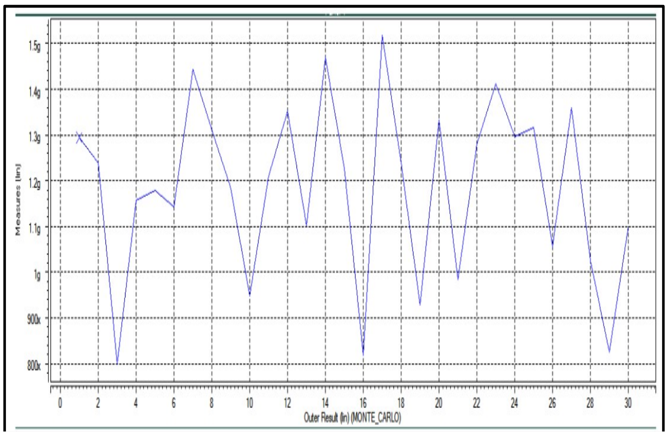

Fig.10 Variation in frequency for 30 runs of CML ring compensated VCO

Fig.10 shows the variation in frequency for 30 runs using Monte Carlo simulation and it was found that frequency varies from 800MHz-1.5GHz. The variation in frequency is about 0.7GHz.Further, the probability distribution for frequency was plotted and investigated as shown in Fig.10. The table III depicts the comparison of mean, variance and coefficient of variation for current starved, CML ring and compensated VCO. The coefficient of variation should be as low as possible. The coefficient of variation signifies the ratio of variance to the mean.

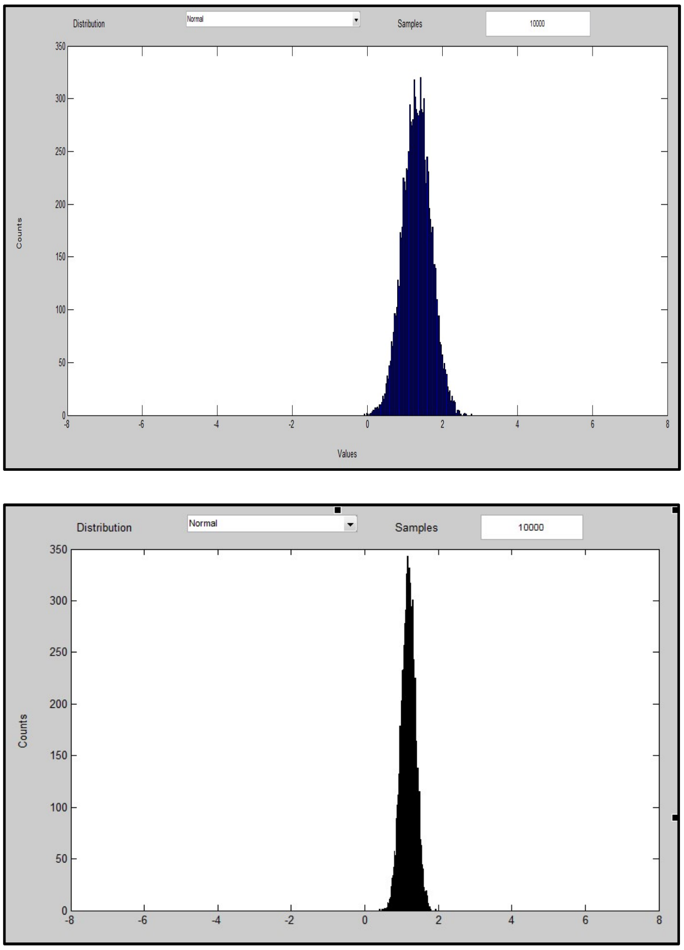

Fig.11 Probability density function for frequency for a) CML VCO and b) Compensated VCO

The probability density function for frequency indicates that the frequency is tightly clustered for the compensated VCO with mean=1.1875. The frequency function is loosely clustered for CML ring VCO at mean=1.311. Also, for the current starved the frequency is tightly clustered with the least coefficient of variation. The comparison of mean, variance and coefficient of variation is tabulated in table III.

Table 3: Varibility Test

Parameter	Current starved	CML ring VCO	Compensated VCO
$mean(\mu)$	3641.1	1.311	1.1875
Sigma(σ)	98.3	0.375	0.194
Coefficient of variation(CV)	0.026	0.28	0.163

The coefficient of variation is also called as relative standard deviation. It is defined as the standard measure of dispersion for the probability distribution. The coefficient of variation is minimum for the current starved VCO and it is about 0.0546.

The coefficient of variation is less for compensated than the CML VCO ring.

5. CONCLUSION

The phase noise of the compensated system obtained is -16.2dbc/Hz. The compensated system has low supply sensitivity of about 0.0546GHz/Vthan conventional current starved as well as conventional ring oscillator while maintaining nearly constant oscillatory frequency. The tuning range is also improved than conventional CML ring oscillator. Its average power is also low. Further, the analysis shows that compensated VCO is more stable for temperature variation and supply sensitivity. The coefficient of variation obtained is 0.163.

REFERENCES

[1]. D. Bol, Student Member, IEEE, R. Ambroise, Denis Flandre, Senior Member, IEEE, and J. Legat, Member, IEEE, “Interests and Limitations of Technology Scaling for Subthreshold Logic,” IEEE transaction on Very Large Scale Integration (VLSI) system, vol. 17, no. 10.Ocotber 2009.

[2]. N. Geetha Rani, N. Praveen Kumar, Dr. B. Dr. B. Stephen Charles, Dr. P. Chandrasekhar Reddy, S.Md.Imran Ali, “Design of Near-Threshold CMOS Logic Gates,” International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.2, April 2012.

[3]. T. Kumar Agarwal1, A. Sawhney, K. A.K., M..Hasan. Department of Electronics Engineering Zakir Hussain College of Engineering and Technology, “Performance Comparison of Static CMOS and MCML gates in sub-threshold region of operation for 32nm CMOS Technology,” Proceedings of the International Conference on Computer and Communication Engineering 2008 May 13-15, 2008 Kuala Lumpur, Malaysia.

[4]. A. Shapiro, E.G.Friedman, “MOS Current Mode Logic Near Threshold Circuits,” J. Low Power Electron. Appl. 4, 138-152, 11 June 2014.

[5]. I. Arora, “Effect of temperature and threshold voltage on subthreshold logic families,” International Journal of Advanced Computer Technology (IJACT).

[6]. F. Cannillo and C. Toumazou, “Nano-power subthreshold current-mode logic in sub-100nm technologies,” Electronic Letters, Vol. 41 No. 23, 10th November 2005.

[7]. .M. Alioto, Y. Leblebici, “Analysis and Design of Ultra-Low Power Subthreshold MCML Gates,” IEEE, 2009.

[8]. M. Sumathi, K. Y. C, “Performance and analysis of CML Logic gates and latches,” IEEE International Symposium on Microwave, Antenna, Propagation, and EMC Technologies For Wireless Communications, 2007.

[9]. F. Cannillo, C. Toumazou, T. Lande “Nanopower Subthreshold MCML in Submicrometer CMOS Technology,” IEEE transaction on circuits and system, Vol. 56, No. 8, August 2009.

[10]. A Tajalli, E.Vittoz, Y. Leblebichi, “Ultra low power subthreshold current mode logic utilizing PMOS load device,” Electronic Letters, Vol No. 43, 16th August 2009.

[11]. U. Seckin, Member, IEEE, and C. K.Yang, Member, IEEE, “A Comprehensive Delay Model for CMOS CML Circuits,” IEEE transaction on circuits and system, Vol. 55, No. 9, October 2008.

[12]. H.Hasan, M. Anis, M. Elmasry, “Design and Optimization of MOS Current Mode Logic for Parameter Variations,” Conference paper in integration the VLSI journal, January 2004.
[13]. M.Alioto, G. Palumbo, “Power-Aware Design of Nanometer MCML Tapered Buffers,” IEEE transaction on circuits and system, Vol. 55, NO. 1, January 2008.
[14]. G. Jain, K. Vyas, V. Maurya, “Comparative Analysis of Universal Gates using MCML and CMOS Technique,” International Journal of Computer Applications (0975 – 8887) Volume 118 – No. 5, May 2015.
[15]. Ajay Kumar Mahato,“Ultra Low Frequency CMOS Ring Oscillator Design,” Proceedings of 2014 RAECS UIET Panjab University Chandigarh, 06 – 08 March, 2014.
[16]. To-Po Wang,” A Low-Power Low-Phase-Noise Wide-Tuning-Range 60-GHz Voltage-Controlled Oscillator in 0.18- m CMOs,” IEEE 2011.
[17]. R.RJagtap, Dr.S.D.Pable,” Design of Low Power Current Starved VCO with Improved Frequency Stability,” IEEE International Conference on Recent Advances and Innovations in Engineering (ICRAIE-2014), May 09-11, 2014, Jaipur, India.
[18]. Jyoti Garg, Seema Verma,” Design of Low Power Voltage Controlled Oscillator,” 1st International Conference on Emerging Technology Trends in Electronics, Communication and Networking, 2012.
[19]. Ms. Shruti Suman, Ms. Monika Bhardwaj, Prof.B.P.singh, “An Improved Performance Ring Oscillator Design,” Second International Conference on Advanced Computing & Communication Technologies, 2012.
[20]. Michael M. Green, “Design of CML Ring Oscillators With Low Supply Sensitivity,” IEEE Transactions on Circuits and Systems, Volume:60, July 2013.
[21]. Saraju P. Mohanty, Ph. D, “Power Dissipation, Advanced Topics in VLSI Systems.”
[22]. www.cadence.com,www.snopsys.com
[23]. R. Dhiman and R. Chandel, “Design Challenges in Subthreshold Interconnect Circuits,” Compact Models and Performance Investigations for Subthreshold Interconnects, Energy Systems in Electrical Engineering,