

DESIGN AND IMPLEMENTATION OF DIGITAL FILTER USING CIC AND FIR FILTER

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Abstract

This paper focuses on design and implementation of CIC-FIR (cascaded integrator-comb-finite impulse response) filter structure for receivers. In Digital Signal Processing, BPFs are essential element of everyday electronics where signals are to be restricted for particular high pass and low pass cutoff frequencies. BPFs (band pass filters) can be designed using FIR filters but due to the increase in complexity of hardware and challenge in meeting timing closure of the design, CIC-FIR filter structure has been proposed to overcome these disadvantages of FIR filter based BPF design. Hence several comparisons made using CIC-FIR Structure for different order and sampling frequency to prove that CIC-FIR structure is better to design BPF. This structure will reduce the sampling rate of the filter making system requirements feasible to implement. This design helps to reduce power consumption indirectly and also timing closure could be met easily.

Keywords—CIC Filters, FIR Filters, FIR-CIC filter, Decimator, Interpolators, Matlab.

1. INTRODUCTION

In signal processing, a filter is a device which is used to remove the unwanted component or the feature of the signal. Discrete time samples are used in the digital filters. The processing is done on the discrete sample to obtain the desired output. The Fourier Transform Theory states that multiplication of two sequences in frequency domain is same as linear convolution of two sequences in time domain. Impulse response of the filter and the multiplication of signal spectrum in frequency domain with it is impact of Digital Filtering. As we know, an ideal bandpass filter has completely flat passband and will completely attenuate all frequencies outside the passband range. The digital filter has all the digital components; it takes in digital input and gives

digital output. The filtering is a process in which analog signal is converted to digital signal using particular sampling frequency F_s . According to Nyquist rate signal which contains the frequency component higher than sampling frequency $F_s/2$ are eliminated. This concept is used to design the BPF for desired high pass and low pass cutoff frequencies using MATLAB.

2. FIR FILTER

The Finite impulse response (FIR) filters structure that can be used to implement almost any sort of frequency response digitally. A series of delays, multipliers and adders is used to get FIR filter output.



Fig.1. Block of basic filter

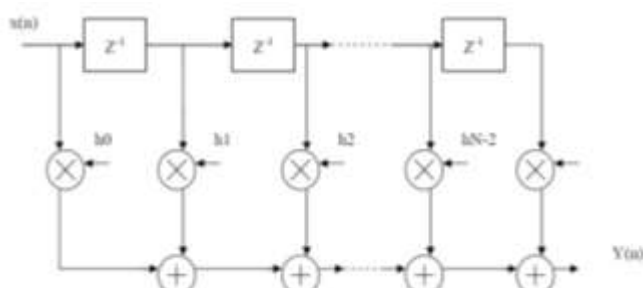


Fig.2. Block diagram of FIR filter

An FIR filter of order N is shown in the block diagram of Fig 2. Due to the operation on past input samples it results in delays. For multiplication the coefficient $h[N]$ values are used, where N is the order of the FIR filter which ranges from 0 to $N-2$. The delayed samples are multiplied by appropriate coefficient. This summation is output at time ' N '. An FIR filter works on the operation known as Dot Product. This is achieved by multiplying the Tap coefficients (an array of constants) and summing the old data and takes in another sample as input. This process is

repeated. A finite impulse response (FIR) filter is a category under digital filter. The filter’s response to impulse comes down to zero. This is known as ‘Finite’ Filter. This finite filter is way different from infinite response response filter. In an Infinite impulse response (IIR) filter, it consists of internal feedback system and continues to response indefinitely i.e; it is unstable. FIR filters have complex filter coefficients for order N due to the presence of multipliers in it.

3. CIC FILTER

A combination of digital integrator and digital differentiator is known as CIC filter. The operation of decimation and digital lowpass filtering is done by CIC filters. The CIC filters are most economical for hardware implementation as no multiplier circuits are required. Also the design complexity with FIR filter can be recovered with the CIC filter. Fig 3 shows the CIC first order block diagram. Since the delay elements used in differentiator stage, hardware implementation is significant. M delay elements are required for differentiator circuits. Registers are used for delay elements. As the registers are delay elements, the number of bits used to store data and number of delay elements increased with oversampling ratio. N cascaded digital integrators operating at a high input sampling rate, F_s and N cascaded differentiators at a low rate F_s/R , where R is the decimation factor which is an integer shown by Hogenauer’s CIC decimation filter, which is shown in Fig.3,. Its transfer function is $H(Z)$, which is an N-stage sinc function.

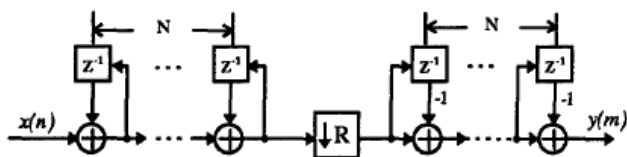


Fig.3: Block diagram for CIC decimation filter.

$$H(z) = \left(\frac{1 - z^{-R}}{1 - z^{-1}} \right)^N \tag{1}$$

This kind of decimation filter is very efficient in the following aspects:

- (1) Required multipliers circuits are zero.
- (2) No need to store the filter coefficients
- (3) Integrating at comb and high sampling rate reduces the intermediate storage.
- (4) At low sampling rate, filtering of CIC filter is done.
- (5) A small external control or complicated local timing is required.
- (6) With small change to filter timing and addition of scaling circuit, the decimation filter design is used for various ranges of rate change factor R.

4. CIC-FIR STRUCTURE

The proposed structure is obtained by giving CIC low pass filter output as input to the FIR high pass filter to obtain

bandpass filter. CIC-FIR structure has following superior advantages when compared to only FIR structure as:

- (1) CIC decimation filters helps to reduce the sampling rate. This feature adds benefit to increase the performance of the system by adopting time multiplexing
- (2). The order of the FIR filter reduces due to the reduction in the sampling rate. In turn the resource utilization and complexity of FIR filter reduces
- (3). FIR filters enables good transition band (sharp) response based on the order of the filter
- (4). CIC filters are simple in implementation.

Combination of CIC and FIR filters cascaded to form BPF is a very good idea in many applications. Because of all this above features CIC-FIR structure is more economical when compared to only FIR structure to obtain the band pass filter. Fig.4, is the block diagram which is used to obtain the CIC-FIR structure .The main characteristics of CIC structure is that sampling rate F_s is reduced to F_s/R where R is the rate change factor (decimation factor). The first block always operates at sampling frequency F_s . CIC filter followed by FIR is used first then that block output will be in F_s/R sampling rate. It will force FIR filter block to operate in same rate. This will not happen if the first block is FIR filter. Hence using CIC filter in the first block is more economical filter structure that can be obtained using CIC-FIR design approach for BPF. Therefore CIC-FIR structure is used for the design.

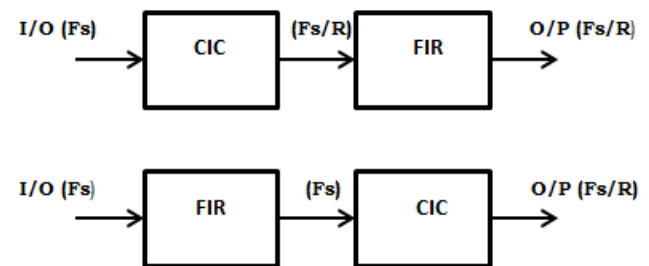


Fig.4. Block diagram of CIC-FIR structure

5. ADVANTAGES OF CIC-FIR FILTERS

CIC decimation filters helps to reduce the samples rate. This feature adds benefit to increase the performance of the system by adopting time multiplexing. The order of the FIR filter reduces due to the reduction in the sampling rate. In turn the resource density and complexity of FIR filter reduces. FIR filters enables good transition band (sharp) response based on the order of the filter. CIC filters are simple in implementation. Combination of CIC and FIR filters cascaded to form BPF is a very good idea in many applications.

6. COMPARISON BETWEEN REVEALED STRUCTURE AND PROPOSED STRUCTURE

Here FIR structure parameters are compared with the CIC-FIR Structure parameters. FIR structure is designed for high pass cutoff 8.28MHz, low pass cutoff at 11MHz, sampling frequency of 100MHz and filter order of 40. The CIC-FIR

structure can be designed for the same low pass and high pass cutoff at filter order 10. This indicates that the sampling rate can be reduced by 4 times. Table 1,2 shows the design parameters of FIR filter and CIC-FIR filter respectively. FIR and CIC filters both are combinational circuit which consists of adder and multiplier elements in it. From [2] each FIR filter consist of one adder and multiplier at single stage hence it consist of N multiplier and N adder at the Nth-stage. Due to the presence of multiplier element FIR filter structure will have hardware complexity. This complexity can be reduced by using CIC-FIR structure as the same cutoff frequency BPF can be designed as that of FIR filter by decreasing the order of the filter. From Table 3, as the order of the filter increases the MAC element required also increases hence the structure of the filter becomes more complex and it requires more time cycles to execute.

This disadvantage can be recovered using CIC-FIR structure in which CIC filter doesn't require multiplier element. As the number of time cycles decreases power consumption can be reduced. The Same approach can be met using FPGA in which the timing closure can be met easily using CIC-FIR structure than the FIR structure. The bandpass frequency plot for FIR filter and FIR-CIC filter approach is shown in the Fig.5 and Fig.6. This implies sharp transition band output from the CIC-FIR structure than The FIR structure only. The designed structure operates at 2.72 MHz bandwidth. Similar way it can be designed for 0.39MHz bandwidth. Both are narrow bandpass filter structure. The design parameters are as tabulated in Table 4 and Table 5. From these two different design parameter we can observe that sampling rate is reduced and also the order of the filter. Fig.7 and Fig.8 are the frequency plot in both CIC-FIR and FIR filter for bandwidth 0.39MHz.

Table1.Design parameter for FIR filters.

DESIGN PARAMETERS	VALUES
Sampling rate	100MHz
Order	40
High pass cutoff	8.28MHz
Low pass cutoff	11MHz

Table2.Design parameter for CIC- FIR filters.

DESIGN PARAMETERS	VALUES
Sampling rate	100MHz
Order	10
CIC sampling frequency	40MHz
R(Decimation factor)	2
M(differential delay)	2
N(Number of sections)	4
High pass cutoff	8.28MHz
Low pass cutoff	11MHz
Bandwidth	2.72MHz

Table3.Comparison between FIR and CIC-FIR for order, sampling rate and number of taps

FILTER TYPE	ORDER	SAMPLE RATE	MAC PER TAP
FIR	40	100MHZ	40 MAC
FIR-CIC	10	100MHz	10 MAC

Table 4.Design parameter for FIR filters.

DESIGN PARAMETERS	VALUES
Sampling rate	100MHz
Order	200
High pass cutoff	0.82MHz
Low pass cutoff	1.21MHz

Table 5.Design parameter for CIC- FIR filters.

DESIGN PARAMETERS	VALUES
Sampling rate	100MHz
Order	20
CIC sampling frequency	10MHz
R(Decimation factor)	2
M(differential delay)	4
N(Number of sections)	4
High pass cutoff	0.82MHz
Low pass cutoff	1.21MHz
Bandwidth	0.39MHz

Table 6. Comparison between FIR and CIC-FIR for order, sampling rate and number of taps.

FILTER TYPE	ORDER	SAMPLE RATE	MAC PER TAP
FIR	200	100MHZ	200 MAC
FIR-CIC	20	100MHz	20 MAC

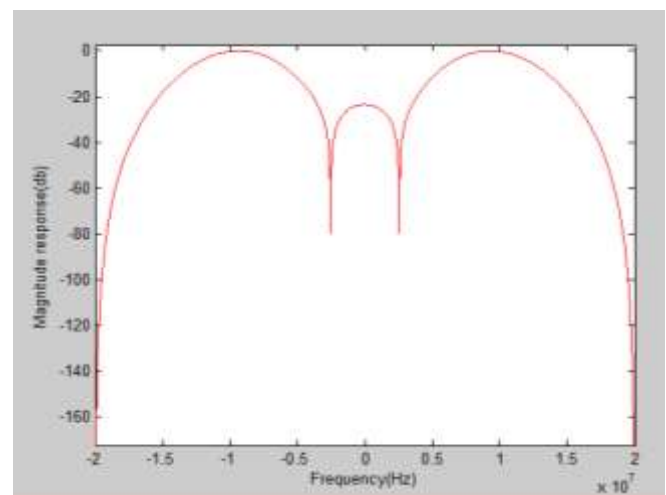


Fig.5 BPF for CIC-FIR structure(BW=2.72MHz)

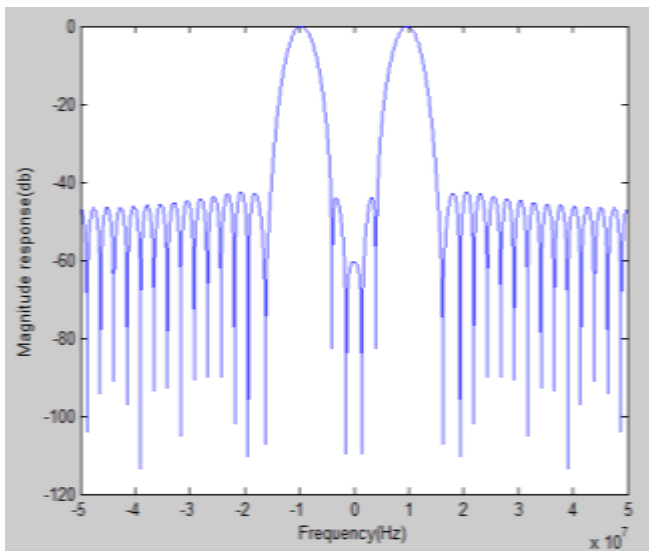


Fig.6 BPF for FIR structure only(BW=2.72MHz)

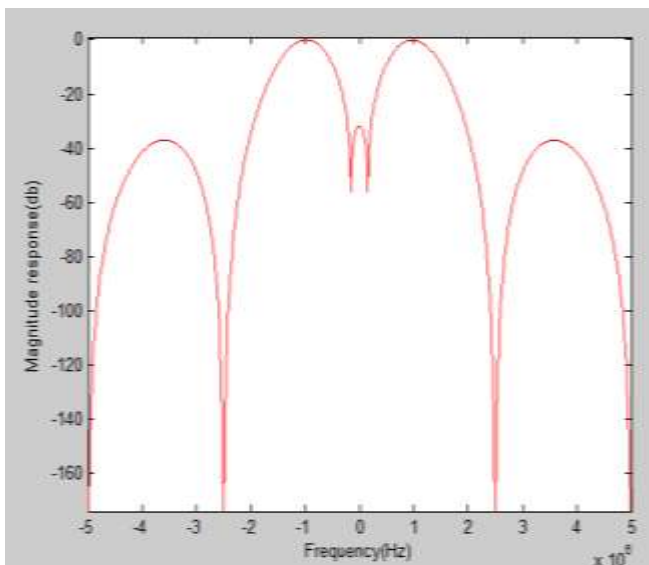


Fig.7 BPF for CIC-FIR structure (BW=0.39MHz)

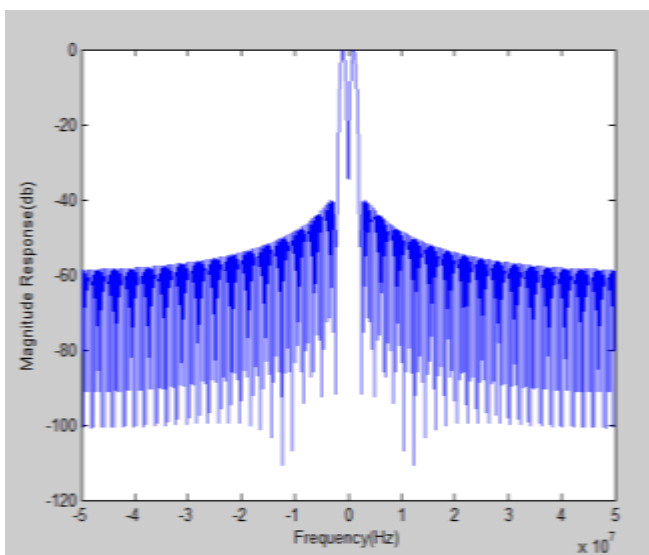


Fig.8 BPF for FIR structure only ((BW=0.39MHz)

7. CONCLUSION

In this paper, we propose a CIC-FIR Filter structure based BPF. The CIC-FIR structure is superior to FIR structure in terms of the simplicity in the hardware. This reduces the complexity of the hardware and area consumed. It helps to meet the timing closure in FPGAs. The timing closure depends on the combinational elements such as multipliers and adders. These elements are more in FIR based BPF resulting challenge to meet the performance. In order to increase the performance pipelining has to be approached which in turn adds additional area consumption for FFs. These additional aspects call for power consumption factor.

The result of CIC-FIR indicates a significant superiority and comparable performance with the FIR filter. It has been observed that the order of the filter can be reduced to the lower order for the same filter parameters.

The proposed framework can also be used to reduce the sampling frequency which reduces power consumption. Hence using CIC-FIR design approach hardware complexity and the power consumption of the system can be reduced, so it is very economical filter structure for the narrow band BPFs. This structure could be considered in the cases where in roll off characteristics are not stringent. Otherwise compensation filters should be accommodated to overcome the droop of the CIC.

FUTURE SCOPE

This project could be taken to the next level as a future scope by using this design in any of the receiver implementation. It has main scope in design of heterodyne receiver in choosing particular TV channels.

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