INVESTIGATION OF PARASITICS IN POWER CIRCUITS SWITCHED WITH CASCODE GAN HEMTS

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Abstract

Gallium Nitride (GaN) devices due to its superior material properties over Si has the potential to provide better system level performance when integrated into power electronic applications. These fast switching devices are continuously evolving in the market with 600 V devices getting commercialized and manufacturers coming up with different variants of normally-off devices to completely exploit the wondrous properties of this novel material. The growing acceptability of these devices has seen a strong interest in cascode structures. However, there is a lack of understanding of the issues caused by these nearly ideal devices when used in real circuits. Therefore, this paper is aimed at investigating the influence of parasitic inductances and capacitances that causes unexpected behavior in cascode GaN based half-bridges. This problem is addressed by performing detailed theoretical analysis and Pspice simulations to formulate design rules. These predictions are then experimentally validated by designing and demonstrating 1 kW, 500 KHz GaN half bridge prototypes using different gate drives. The novelty of this paper lies in providing a holistic approach to the instability issues in cascode GaN high electron mobility transistor (HEMT) based half-bridge circuits caused due to parasitics of the device, package and the PCB layout.

Keywords— *Gallium Nitride(GaN), HEMT, Cascode, Half-Bridge, Power Converters, Parasitics.*

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1. INTRODUCTION

GaN power devices due to its excellent material properties together with a low-cost manufacturing scheme (GaN-on-silicon), are rising as strong contenders challenging the age old Si devices to meet the changing energy needs of our times [1,2]. It has moved from being a fascinating laboratory curiosity to being active in industrial research arena with companies like EPC, Panasonic and GaN Systems commercializing their 600 V products. This has led the industry to actively engage in accelerating research activities aimed at finding a huge volume application that will drive the GaN market [3].

The momentum gained by these devices has been driven by astrong interest in cascode devices. Motivated by the reasonably high–threshold gate voltage, normally-off structure, very low reverse recovery charge, small output capacitance, conventional TO package and ease of use, GaN cascode devices have generated a lot of hype and enthusiasm in the market [4].

Despite widespread interest in these structures, there is surprisingly limited literature on them. There is a few on the characterization and working of cascodes, driving methods and applications [5,6]. The use of these cascodes in zero-voltage switching topologies and packaging issues has attracted some interest [7,8]. There has also been reported work on variations of cascode like-the capacitor clamped and cascade light configurations though its suitability for bridge circuits are yet to be investigated [9].

There is a good deal of literature aimed at developing accurate loss models of depletion e-mode devices that can estimate the switching loss and eventually give a good prediction of the overall efficiency of the power converter; however, attempts to model the cascode operation has been limited [10]. Recently, a good analytical model for high voltage GaN HEMT in cascode configuration has been proposed by Huang in [11] which forms the basis of the model used in this paper.

So it is clear from the review that, at large, cascode GaN HEMTs still remain to be fully explored and understood in terms of the effect of parasitics and instability issues they cause when deployed in half-bridge circuits which is the main aim of this paper. This paper thus addresses the unexpected behavioral issues by evaluating and quantifying the effect of different types of parasitics on the performance of the circuit so that it can be effectively used in real circuits. The design rules framed is thus intended to act as a reference guideline for system engineers wishing to translate the device properties into excellent system level benefits.

This paper is organized as follows: Section II briefly describes GaN cascodes and their device structure detailing the issues concerning their performance. In section III, the theoretical analysis of cascodes is performed followed by simulation in Pspice and design rule formulation. Section IV demonstrates and analyses the stability of half-bridges using the two gate drivers with discussion on pros and cons of both. Section V includes conclusion and future work followed by acknowledgment and references.

2. STRUCTURE AND WORKING OF GAN CASCODES

The basic GaN device structure is generally normally-on type. But these are not preferred in power applications due to safety and acceptability considerations and hence the power device engineers came up with the cascode configuration to convert it into normally off type [4,5].

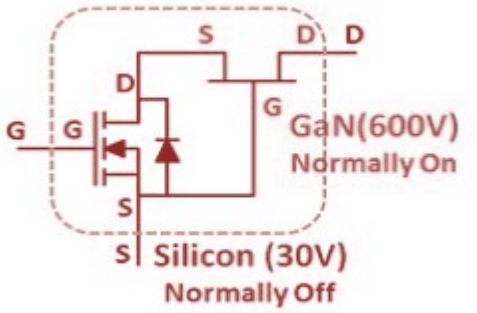

Fig 1: Structure of GaN cascode

As shown in figure 1, a normally-off low-voltage Si FET (typically 30 V) is connected to normally-on high-voltage GaN HEMT (600 V) in series while the gate of the GaN HEMT is connected to the source of the Si FET. This hybrid configuration produces an effective normally-off switch. Controlling the state of the low voltage Si MOSFET in order to control the on/off state of the high voltage GaN HEMT makes the cascode GaN HEMT compatible with the commercial Si drivers. But cascodes have uneven voltage distribution issues between the GaN and MOSFET, is more lossier due to low voltage Si switch and is preferred only for certain topologies and switching modes.

The switching performance of the cascode is governed by the effect of parasitic inductances and capacitances, as well as the gate resistances and there is the potential for high instability due to these parasitics as frequency increases [14]. Stability can be assured by slowing down the switching of the GaN FET with a very large gate resistor, but this significantly increases switching losses. While considering its performance in a half-bridge circuitry as in figure 2, which is the building block for most of the converter systems today, effects due to parasitic inductances, capacitances and oscillations are very important as this would all lead to high instability in the circuit [15,16].

So in order to analyze these effects, firstly, the hybrid cascode switch based half-bridge leg is analyzed in detail and then simulated in P-SPICE to understand its working so as to translate all the device properties to useful system level performance benefits and then gate drives are designed and optimized to mitigate the instability and make the switches work reliably and efficiently.

3. THEORETICAL AND SIMULATION ANALYSIS

This section will investigate the effect of parasitic inductances and capacitances of the PCB layout and package inductances of the device on the performance of the circuit through theoretical analysis and simulations. In figure 3, the equivalent circuit of the high voltage GaN transistor in half-bridge configuration, including its parasitics elements, is shown. Inductances Lg, Ld, and Ls represent the package lead frames, while Lint1, Lint2, and Lint3 represent the parasitic interconnections between the GaN die, the Si die and the lead frames. [12,13] These inductances are in the nH range, but they influence the switching transition significantly when the frequency is increased and hence they contribute to majority of the problems in GaN circuits. So the design of the PCB layout becomes very critical in order to minimize these parasitic inductances that distorts the circuit and destroys the device [17].

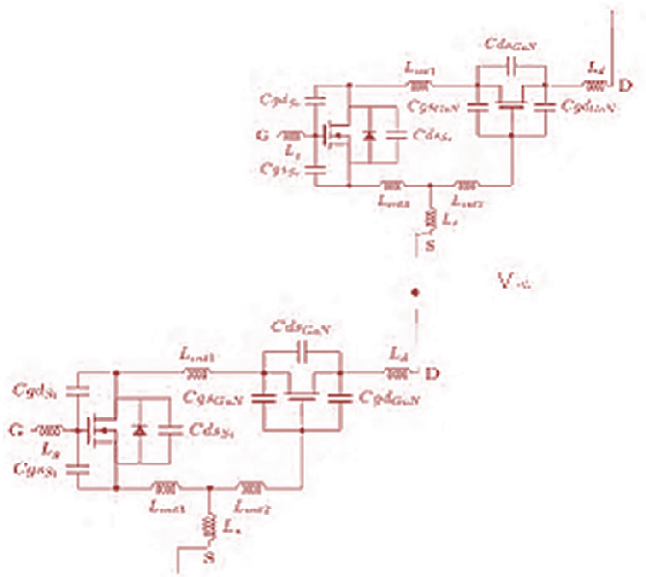

Fig 2: GaN cascode half-bridge circuit with parasitic inductances and capacitances

Looking at figure 2, the output capacitance of the low voltage Si MOSFET must be charged first. Moreover, the gate-source capacitance of the GaN transistor is connected in parallel with the output capacitance of the MOSFET. As the drain-source voltage of the Si MOSFET is lower than the absolute value of the pinch-off voltage of the GaN transistor, the GaN channel is conducting, connecting the gate-drain capacitance of the GaN in parallel with the capacitances mentioned above [19].

Consequently, for voltages lower than the pinch-of voltage of the GaN transistor, the output capacitance of the cascode structure is given by the sum: $C_{gdS}i + C_{dsSi} + C_{gsGaN} + C_{gdGaN}$. When the drain-source voltage of the MOSFET reaches the pinch-off voltage of the GaN transistor, the further increasing voltage of the cascode structure is supported only by the GaN transistor and the output capacitance is given by

the sum:C_{dsGaN} + C_{gdGaN}. This has significant impact in bridge configurations.

Since we are considering a half-bridge; for analysis, let us consider the stage at which bottom switch is off and top switch is conducting. At this stage, the capacitances of top switch can be neglected and only parasitic inductances would matter. Whereas, for bottom switch, which if off, only the capacitances would be relevant. Considering these factors and applying circuit analysis, following equations are derived for turn-on and off transitions of the top switch. For turn off transition: The value of the current i_L at the end of the previous stage determines the remaining energy of the parasitic inductors and, eventually, the overshoot of voltage across the cascode.

Turn-on transition:

The parasitic capacitances of the top switch and the inductor resonate with the parasitic inductances in the circuit and the current ringing period begins.

$$(L_d + L_s + L_{ploop} + L_{int1} + L_{int3}) di_L/dt + (R_{chsi} + R_{chGaN} + R_{stray}) i_L = V_{in} \quad (1)$$

where Rch is the ohmic resistances of Si and GaN

$$\{V_{in} - (R_{chsi} + R_{chGaN} + R_{stray}) i_L\} / di_L/dt - (L_d + L_s + L_{int1} + L_{int3}) = L_{ploop} \quad (2)$$

This equation will help us estimate the maximum allowed PCB inductance and the overshoot it will cause.

When the GaN drain to source voltage-Vds reaches zero, the parasitic capacitances of the GaN switch and the inductor resonate with the parasitic inductances in the circuit and the current ringing period begins. The GaN Vds increases to zero and the Si-Vgs exponentially increases to the gate voltage Vg. Normally, the ringing will be damped long before the Vgs-Si reaches the gate voltage, but the parasitic capacitance of the load /supply voltage is found to have has a significant impact during this stage [11].

Turn-off transition:

$$(L_d - L_s + L_{ploop}) di_L/dt + (R_{chsi} + R_{chGaN} - R_{stray}) i_L - \int(i_L) dt = V_{in} \quad (3)$$

However, the values of these parasitic inductances are not easy to accurately calculate, since, based on the electromagnetic theory, parameters like the dimensions, the positions, and the current directions in the conductors, have significant effect on self-inductance and mutual-inductance [11]. They can be predicted, if the spatial configuration of the Si MOSFET die and GaN die in the package, and the bonding diagram of the device are known and the following values extracted in [12] has been used for reference in this work.

The influence of the package's parasitics called common source inductance (csi) on the switching is defined as the inductance shared by the driving and power loop, and is of great importance [12]. The CSI acts as negative feedback slowing down the driver of the device during the turn-on and turn-off switching transitions. This mechanism prolongs the voltage and current slew rate causing a significant increase in the switching loss. Consequently, the CSI is proven to have the biggest impact on the device's switching loss. However, the unique structure of the cascode GaN HEMT makes the definition of the CSI complicated and the conclusions of the above publications are found to be not applicable to them.

Z. Liu investigated the influence of the cascode GaN HEMT's package parasitics by defining the CSI of the low-voltage Si MOSFET and the high-voltage GaN HEMT separately. It can be seen from (figure 2) that for the Si MOSFET, the CSI consists of the inductances Lint3 and Ls, while from the perspective of the GaN HEMT, the CSI is formed by the Lint3 and Lint1. Consequently, the Lint3 is considered to be the most critical parasitic inductance as it is CSI for both the GaN HEMT and the Si MOSFET. Next, the Lint1 is considered the second-most critical inductance as it is the CSI for the GaN HEMT. Finally, the Ls is considered as the third most important.

In a half bridge leg, the effect of these parasitics gets even more complicated as Ld, Lint1 and Lint3, gate capacitance, and gate drive pull down loop will form multiple LCR resonant circuits that needs to be damped to avoid an equivalent positive voltage ringing across the gate. This ringing could turn the device on again near the end, or even past the end of the voltage transition as shown in figure 3. All these effects can cause one of the switches to conduct when it should be off and will ultimately lead to shorting of the leg as shown in these figures 3 and 4. Detailed analysis of these multiple resonant circuits and their effects will be pursued by author as future work.

Fig 3: Shorting of the leg due to cross-conduction

Fig 4: Switch voltage going negative and rising above Vth

Thus, based on these studies, simulation was performed in Pspice to determine the effect of CSI and other parasitic parameters on V_{DS}. The converter consists of HS and LS GaN FETs and their gate drivers, the input capacitors and the output LC filter. The PWM signal is typically generated from a control IC. Both HS and LS FETs have CSI which causes current to flow through the gate drive and the load.

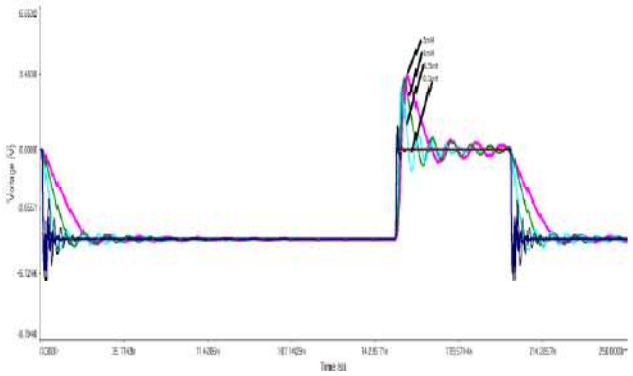

Fig 5: Effect of different values of total parasitic inductances on gate voltage

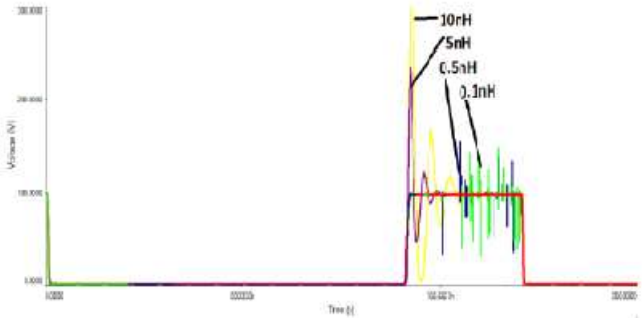

Fig 6: Effect of different values of total parasitic inductance on drain voltage

The figures 5-7 shows the variation of gate and drain voltage with parasitic inductances and gate resistance variation. The results comply with the calculated values. As inductance increases above 5nH, the ringing starts to increase significantly for the drain voltage and gate voltage.

We can see that the package inductances from our calculations exceed 5nH when we solve it for the extracted parameters in [12] and hence the ringing and oscillations observed in experimental results indicate the presence of high parasitics and this increases with frequency. As parasitics increases beyond few nH, the ringing in the drain voltage becomes severe and increases exponentially thereafter. This signifies the importance of these low level parasitics in GaN circuits.

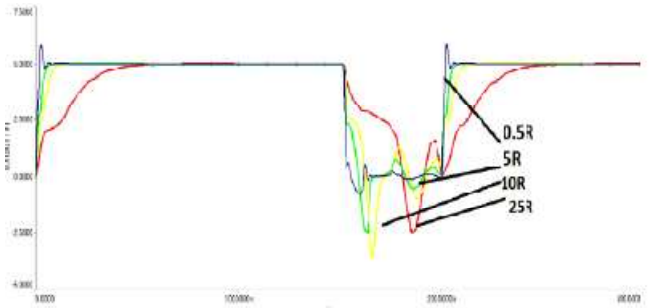

Fig 7: Effect of different values of gate resistances on gate voltage

4. EXPERIMENTAL ANALYSIS

The hardware prototypes are designed with 600 V GaN devices (figure 8) based on the analytical and simulation studies and two different gate drive circuits are demonstrated to analyze the stability of the circuit. Two different sets of layout tracks traced are as short as possible, especially between the drivers and the GaN FETs to reduce the undesirable effects due to the parasitic inductance introduced when using large tracks [19,20].

The PCBs have been designed in Orcad and a four layer configuration is used. The PCB is made as small as possible (2.5 x 1.5cm and 4.5 x 3 cm) with a tight layout with the driver circuit placed very near to the gate to avoid loop inductances. Capacitors are placed as close as possible to the devices for reducing unwanted losses [21-24].

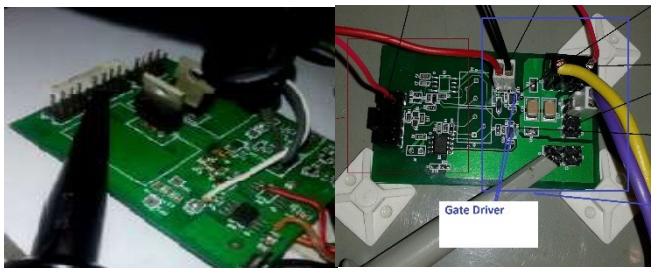

Fig 8: Prototype of GaN cascode half- bridge circuits

The results of the study suggest that the gate driver based on the GaN specific IC, gave nearly ideal switching characteristics with rise and fall times around 3.5ns and hence worked according to device specifications (figure 10). The overshoot and ringing was within 5-10 % of the Vds as the input voltage was increased from a few volts to 400 V but was sensitive to voltage disturbances and noise. As noticed in the analytical analysis the turn-on spikes and oscillations are higher than during turn-off (figure 9). Thus these devices gave excellent switching performance till a few MHz but required stringent PCB design considerations and gate voltage stabilization for reliable working.

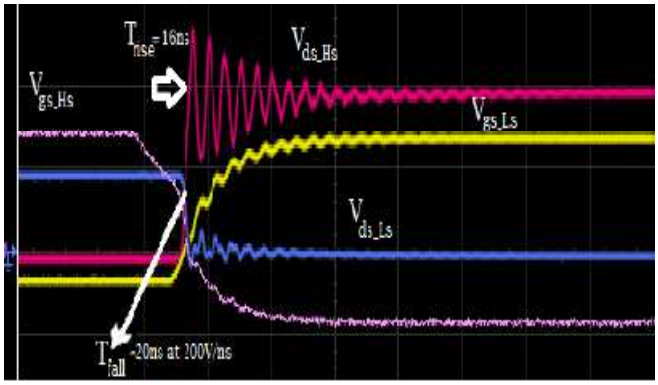

Fig 9: Vds and Vgs of high & low side GaN switches with LM5114 driver

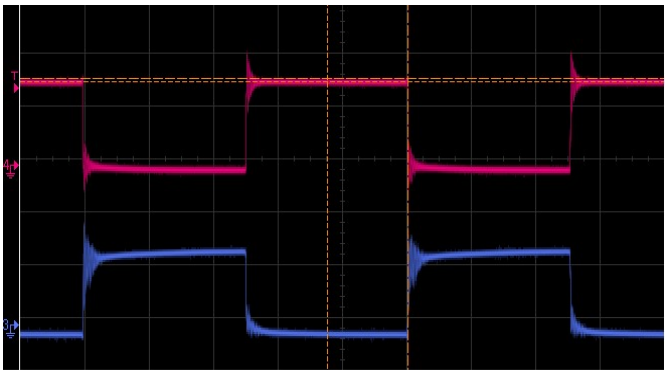

Fig 10: Switching node voltage of low & high side switches with rise and fall around 3-4 ns

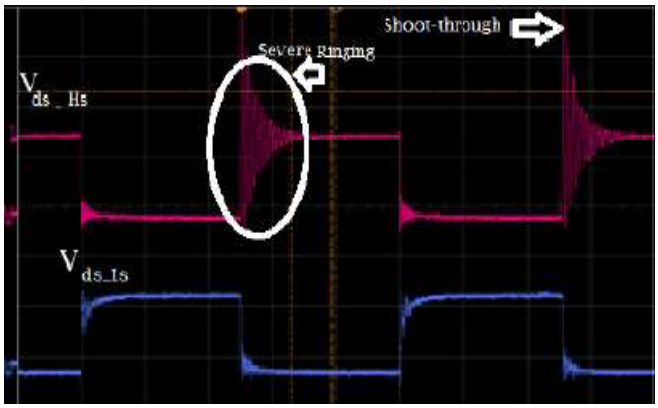

Fig 11: Vds of high and low side GaN switches using ADuM3221 driver

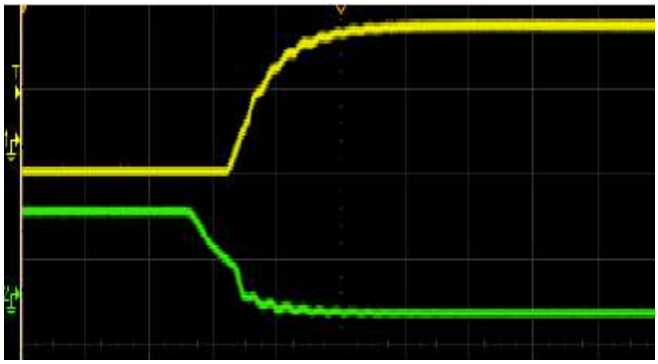

Fig 12: Gate voltages of high and low side switches with slow rise time around 35ns

The second gate driver was built using commercial Si driver- ADuM3221 with a negative drive voltage circuitry to avoid spurious turn on. This system was more robust with increased rise and fall times around 15-20ns; the switching performance was compromised due to slow drive characteristics and more ringing which required damping components (figure 11,12). This drive worked reliably in the frequency range of 10 KHz to 500 KHz but the system complexity and cost is increased due to the negative drive voltage generation circuity.

5. CONCLUSION

The main objective of this research work was to investigate the influence of the different parasitic inductances and capacitances on the switching behavior of the high voltage GaN cascode in a half-bridge configuration, so as to enable better design of circuits using these devices. Towards achieving this goal, a thorough study with analytical analysis followed by simulation studies and experimental demonstration has been performed. The results of this work suggest that the effect of certain parasitics like the power loop inductances are more significant than others and the overall effect can be minimized by careful PCB layout and component placement. The effect of CSI in these circuits have been found to be more complex and will be explored in more detail by the author as future work.

The current gate drivers available for GaN are targeted at HEMT devices and are not suitable for cascodes. GaN specific driver used in this work will prove useful in high-performance related applications and a gate feedback control will stabilize the gate voltage oscillations which can lead to more reliable working. The IGBT based drive can be used for GaN cascodes, but for optimum performance, transient voltage suppressing diodes and decoupling capacitors are required for damping oscillations and limiting overshoots which increases complexity and cost. The primary contribution of this paper is the analytical validation and experimental verification of the cascode model that can serve as a guideline for designers to deal with GaN cascodes in half-bridge based applications.

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He is an inventor of over 70 patents and has over 350 publications in journals and international conferences. For his "outstanding contribution to British Engineering" he has received the Silver Medal from the Royal Academy of Engineering in 2012. In Oct 2015, he was elected Fellow of the Royal Academy of Engineering. He is also the global editor for power semiconductor devices of the IEEE Transactions on Electron Devices, the preeminent international journal in electronic devices.