DESIGN AND OPTIMIZATION OF INTERDIGITAL CAPACITOR

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Abstract

As the wireless communication system continues to progress, higher levels of integration, smaller size, lower weight, lower power consumption, higher performance, and lower product costs are required. The planar passive components (Inductor and capacitor) playa majorrole to design RF/Microwavecircuits. In this we paper propose a design and optimize inter digital capacitor using RT/Duriod substrate material. The substrate materials has lower dielectric constant (3.66) and tangent loss (0.0013). The physical parameters of interdigital capacitors directly depend on magnitude of the capacitanceand quality factor. The variation of physical parameters like fingers (N), finger width (W) and space between the fingers (S) arethe desired scale (in mm) will changethe capacitance value significantly. The interdigital capacitor is designed with the help of existing formulas and designed structures areoptimized. The EM (electromagnetic) simulation is done byusing NI/AWR tool. The observed results show that the designed capacitors can be smaller in size and display higher Quality factor (QF) at 600MHZ operating frequency.

Keywords–*NI/AWR, Interdigital Capacitor, EM Simulation, MMIC, Microstrip line, Quality Factor*

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1. INTRODUCTION

The passive RF/Microwave circuit components find wide applications in communication, industries and different fields of medicine, military and space. The interdigital capacitors are used as antenna radiators connected with RF-amplifiers as active component in receiver circuit [1]. The passive components like inductors and capacitor play a major role in system level development. In this paper we discussed design and optimization of interdigital capacitor.

The microstrip lines are frequently used to construct multilayer integrated circuits (MIC). The traditional flat and cylindrical capacitors are well known structures than the interdigital capacitor. The electric and magnetic field distribution in flat and cylindrical capacitors is different than interdigital capacitor [2]. The interdigital planar capacitors are preferred for high frequency applications.

The efficiency of a capacitor is varied with respect to change in physical parameters of the interdigital capacitor. The major parameters are number of fingers (N), finger width (W) and space between the fingers (S).These parameters are varied according to the desired capacitance of capacitor for particular applications. In this discussion dielectric value is kept constant.

The physical parameters of the interdigital capacitors are varied and it is increases capacitance value and decreases quality factor due to increase in reactive resistance and inductance.In this paper we propose a design and optimizethe interdigital capacitor using RT/Duroid substrate material. The designed structures shows that smaller sizesare flexible to use at higher frequency applications. The obtained result shows that better quality factor can be observed at 600MHZ operating frequency.

The paper is organized as follows; Section II presents the basic design approach for interdigital capacitor. In section III specific realization of interdigital capacitor in MIC is discussed briefly. In section IV, design and optimization of interdigital capacitor with different space between the fingers, and width of the fingers and length of the fingers is discussed. In section V results and discussions using graph we explained and section VI, we summarize the obtained results.

2. BASICS OF IDC CAPACITOR

The interdigital capacitor is a multi-finger periodic structure and it uses lumped circuit elements for RF/microwave development. This has higher quality factor than gap capacitor and MIM capacitor. The interdigital capacitors use the capacitance that occurs across a narrow gap between copper conductors. These gaps are essentially very long and folded to use a small amount of area [2]. The structure of an interdigital capacitor is designed using copper as conducting material with 0.032 thickness and the parameters are shown in figure 1.

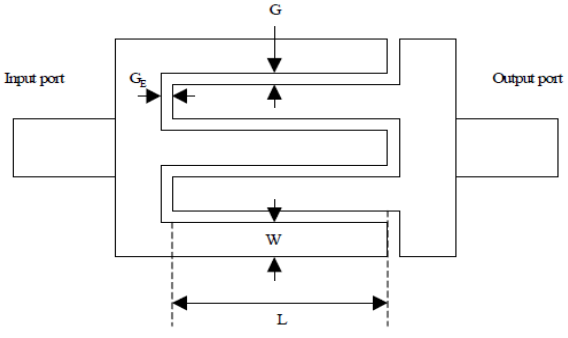

Fig. 1. Inter Digital Capacitor

The figure shows that gaps (G) or space (S) between fingers at the end of the fingers (GE) are the same. The length (L) and width (W) of the fingers are also specified and the conductor is mounted on a substrate. The characteristics of substrate will also affect the performance. The interdigital capacitor frequently uses microstrip line planar transmission line because of easy of design and fabrication. The properties of this type of capacitor have been studied by many authors [3-7]. They are many assumptions made, some of which are: (1) only coupling between adjacent fingers is considered; (2) the number of fingers is large such that a periodic smooth structure can be assumed; (3) capacitor dimensions are much less than a quarter wavelength; and (4) capacitance at the end of each finger is neglected [8]. An improved model in which the capacitor is divided into its basic subcomponents is briefly described in reference [2].

3. DESIGN OF INTERDIGITAL CAPACITOR

The area of capacitor should be small relative to the wavelength so that it can be called and treated as a lumped element. This type of capacitor can be fabricated using MMIC technology because there is no need of additional processing steps. The total capacitance is given by [2,3]

$$C = (\epsilon_r + 1)l[(N-3)A_1 + A_2\,](pF) \qquad (1)$$

In equation 1, ϵ_r represents the dielectric constant of the substrate material, *l*-is the length of the interdigital capacitor finger, N is the number of fingers. The approximation expressions for A_1 and A_2 are obtained by curve fitting the data and are given by (1).

$$A_1 = 4.409\tanh\left[0.55\left(\frac{h}{W}\right)^{-0.45}\right]\times 10^{-6}(pF/\mu m) \qquad (2)$$

$$A_2 = 9.92\tanh\left[0.52\left(\frac{h}{W}\right)^{-0.5}\right]\times 10^{-6}\left(\frac{pF}{\mu m}\right) \qquad (3)$$

The h and W represents the height of the substrate material and width of the conductor respectively. The equation 2 and 3,represents the interior and exterior fingers respectively in the interdigital capacitor structure [3].

The figure 3, shows the lumped equivalent circuits (EC) of the interdigital capacitor. These structures are used for lower frequency applications and for higher frequency we repeat the same structure one more time of the scattering parameters of the equivalent circuit match with interdigital structure then it gives same characteristics [2, 9].

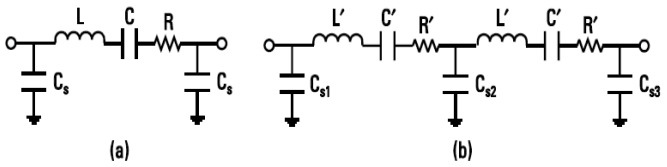

Fig. 3.EC Model of Interdigital Capacitor: a) Lower Frequency b) Higher Frequency

With the help of equivalent circuit to calculate the series resistance is given by

$$R = 1.33\frac{l}{WN}R_s \qquad (4)$$

Where $R_s$is the sheet resistivity in ohms per square of the conductors used in the capacitors.

The capacitance *Cs* and inductance *L* are approximately calculated on the basis that for *S* /*h* << 1, magnetic field lines do not loop around each finger but around the cross section of the interdigital width (Figure.1). The Cs and L are calculated using microstrip transmission theory.

$$C_s = 0.5\times\frac{\sqrt{\epsilon_{re}}}{Z_o\,c}\times l \qquad (5)$$

$$L = \frac{Z_o\sqrt{\epsilon_{re}}}{c}\times l \qquad (6)$$

Where Z_o and $\varepsilon_{re}$are calculated using *W* and *h* microstrip parameters and $c = 3\times10^{10}$ cm/s is the velocity of light in free space. A general expression for the total series capacitance of an interdigital capacitor can also be written as [10].

$$C = \frac{\epsilon_{re}\times 10^{-3}}{18\pi}\frac{K(k)}{K'(k)}(N-1)\times l\ (pF) \qquad (7)$$

where , is in microns, *N* is the number of fingers, and e *re* is the effective dielectric constant of the microstrip line of width *W*. The ratio of complete elliptic integral of first kind *K* (*k*) and its complement *K'*(*k*) is given by.

$$\frac{K(k)}{K'(k)} = \begin{cases} \frac{1}{\pi}ln\left\{2\frac{1+\sqrt{k}}{1-\sqrt{k}}\right\}\ for\ 0.707\le k\le 1 \\ \frac{\pi}{ln\left[2\frac{1+\sqrt{k'}}{1-\sqrt{k'}}\right]}\ for\ 0\le k\le 0.707 \end{cases} \qquad (8)$$

$k = tan^2(\frac{a\pi}{4b})$, $a = W/2$, $b = (W+S)/2$ and $k' = \sqrt{1-k^2}$.

4. DESIGN AND OPTIMIZATION

The figure 2, shows the electromagnetic simulated 3D structure. In this design we consider three layers with RT/Duroid substrate material. It has two port and five fingers with space between the fingers as 1mm. similarly we design with different finger width, number of fingers, space between the fingers and different length of the finger. The simulation repeats as shown in following section.

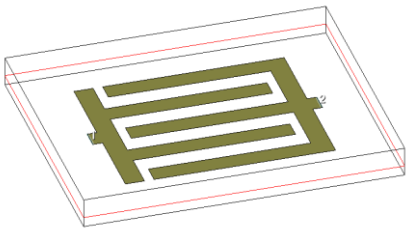

Fig. 2.EM IDC Structure

4.1 Finger Width

The finger width (W) is directly proportional to capacitance of an interdigital capacitor as the width of a finger increases the capacitance of a capacitoralso increases and as shown in figure 4 to 9. The three different finger width like 0.5mm, 1mm, 1.5mm and 2mm with number of fingers from 4 to 10.

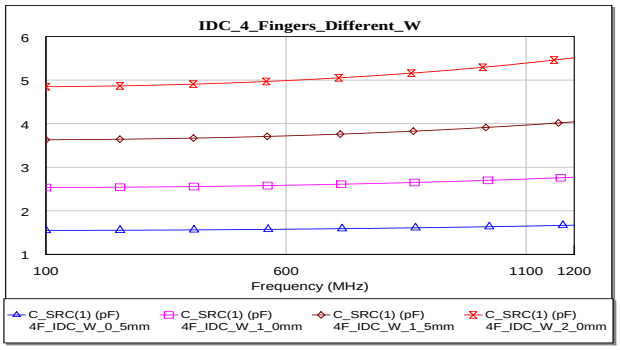

Fig. 3.4_fingere- Capacitance V/S Frequency

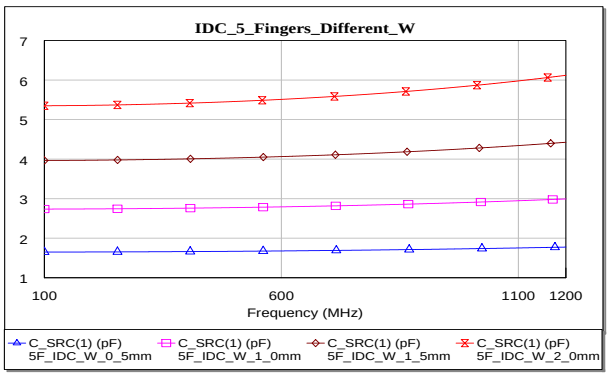

Fig. 4. 5_fingere- Capacitance V/S Frequency

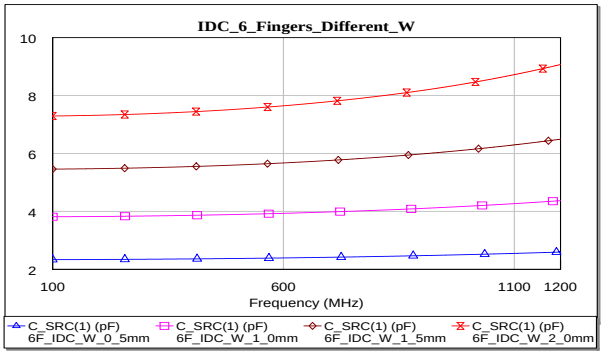

Fig. 5.6_fingere- Capacitance V/S Frequency

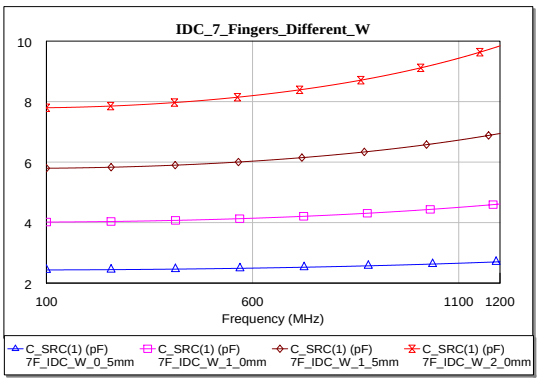

Fig. 6.7_fingere- Capacitance V/S Frequency

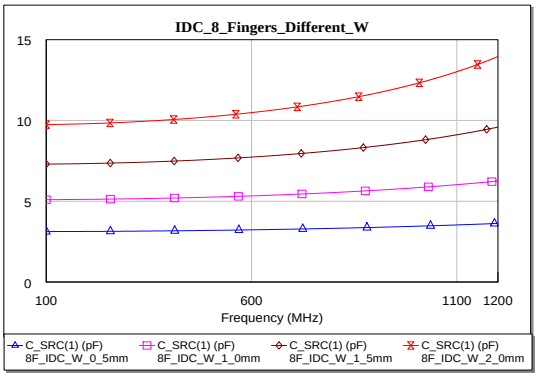

Fig. 7.8_fingere- Capacitance V/S Frequency

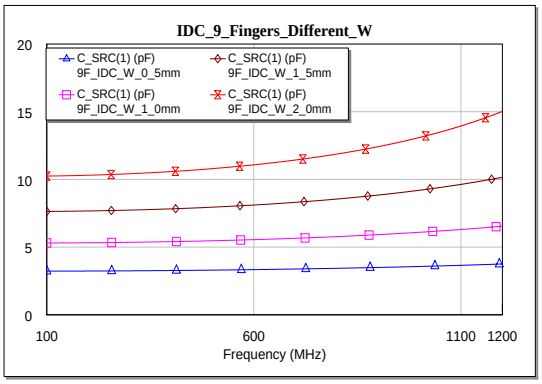

Fig. 8. 9_fingere-Capacitance V/S Frequency

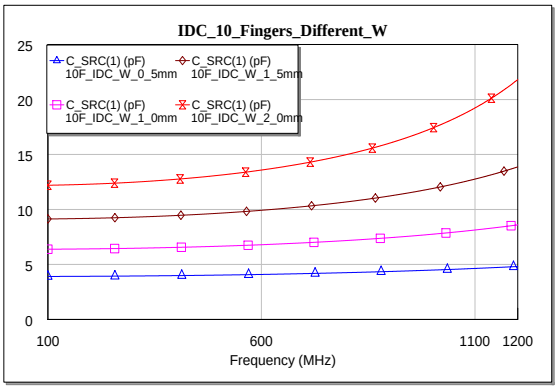

Fig. 9.10_fingere- Capacitance V/S Frequency

4.2 Number of Fingers

The figure 10, shows that capacitance of an interdigital inductor. The fingers of the interdigital capacitors is varied from 4 to 16 with constant finger width and space between the fingers.The capacitance increases quality factor decreases. The electromagnetic simulated results are shown below. The dielectric of RT/Duroid substrate material is constant and designed operating frequency is 600MZH.

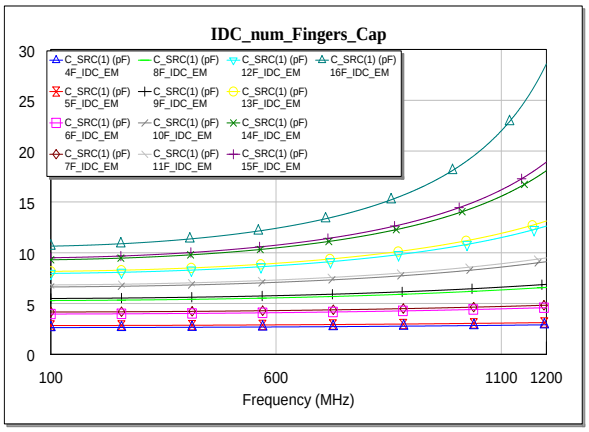

Fig. 10. Fingers From 4 to 16 - Capacitance V/S Frequency

4.3 Space between the Fingers

The space between fingers increases to increase capacitance of an interdigital capacitor by considering the width and dielectric value as constants. The space between is the fingers 4 of the IDC to 10 are varied. The electromagnetic simulated results are shown in the following figures from 11 to 17.As the space between fingers increases the total size of the structure also increases and this increases the vertical length of the interdigital capacitor.

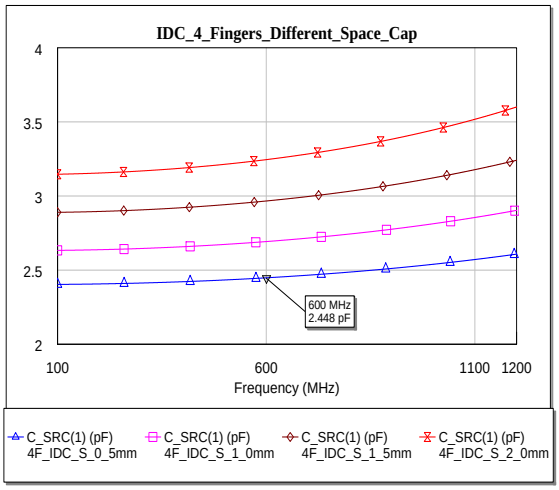

Fig. 11.4_fingere- Capacitance V/S Frequency

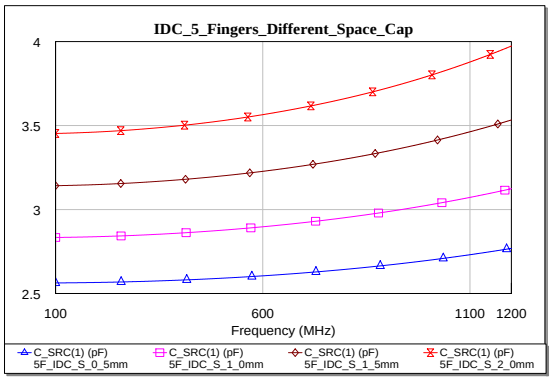

Fig. 12.5_fingere- Capacitance V/S Frequency

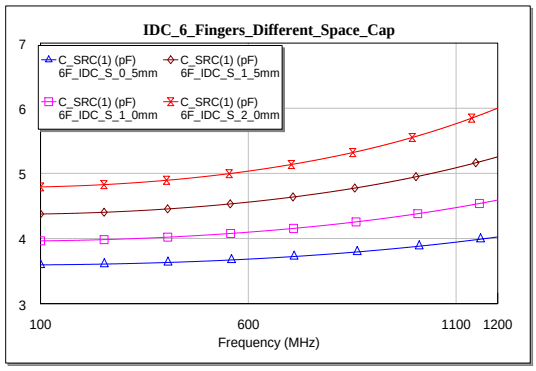

Fig. 13.6_fingere- Capacitance V/S Frequency

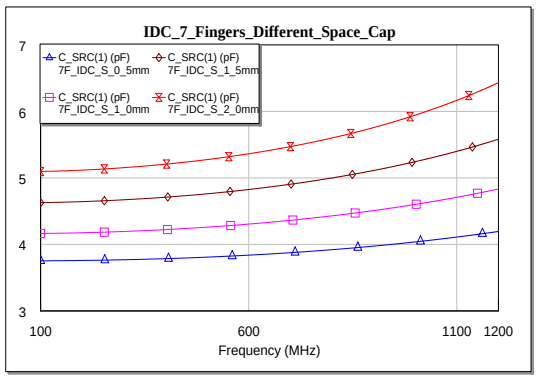

Fig. 14. 7_fingere- Capacitance V/S Frequency

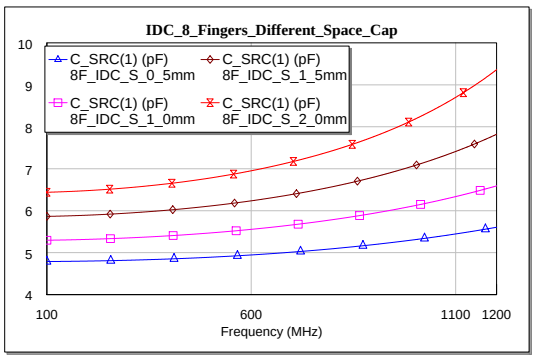

Fig. 15. 8_fingere-Capacitance V/S Frequency

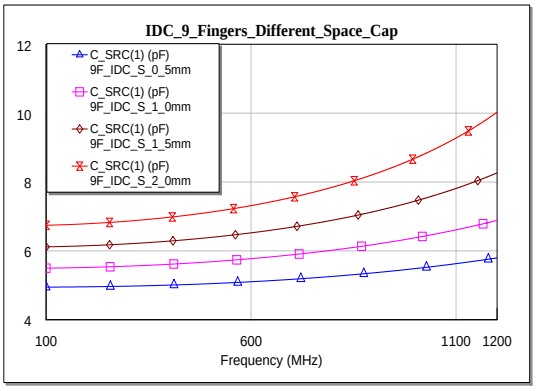

Fig. 16. 9_fingere-Capacitance V/S Frequency

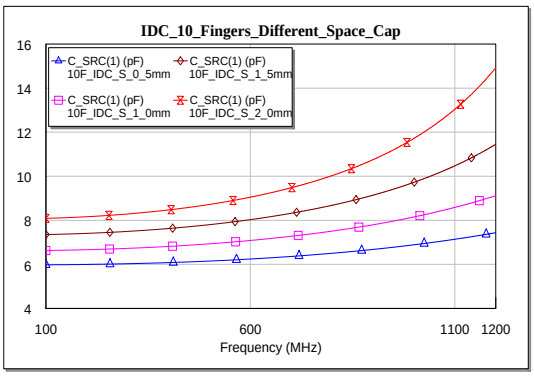

Fig. 17.10_fingere- Capacitance V/S Frequency

5. RESULTS AND DISCUSSION

As the simulated results shows that capacitance increases with respect to increasing conductor width (W), number of fingers (N) and space between the fingers with constant dielectric value. The quality factor is higher at lower capacitance value as thecapacitance increases the quality factor decreases. this shows passive component effect at higher number of fingers or increasing conductor width or space between the fingers. The noted values from the designed operating frequency of 600MHZ.

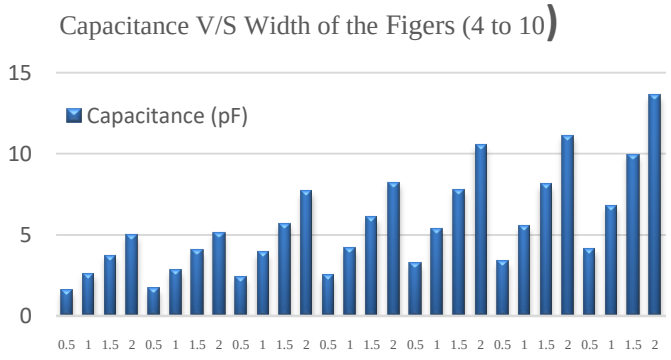

Fig. 18. Width of the Finger V/S Capacitance

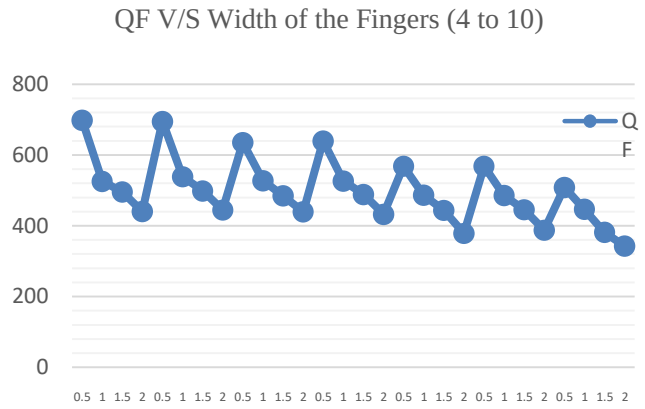

Fig. 19. Width of the Finger V/S QF

The figure 18 shows that capacitance is increased by increasing the finger width and number of figures. It means that as the figure width and number of fingers increases the conductor area and the capacitance also increases. The conductor width is varied from 0.5mm to 2mm with respect to different number of finger from 4 to 10. The figure 19 shows the quality factor for different conductor width with respect to capacitance.

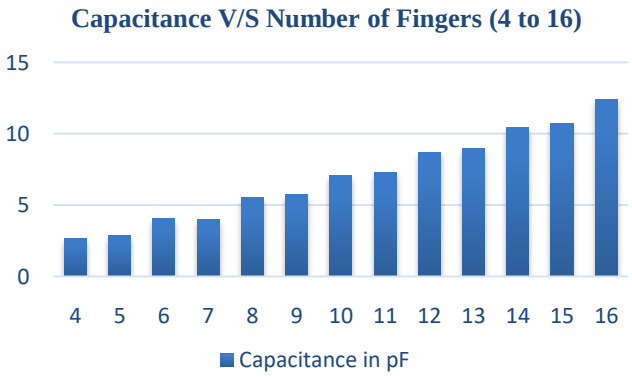

Fig. 20. Number of Finger V/S Capacitance

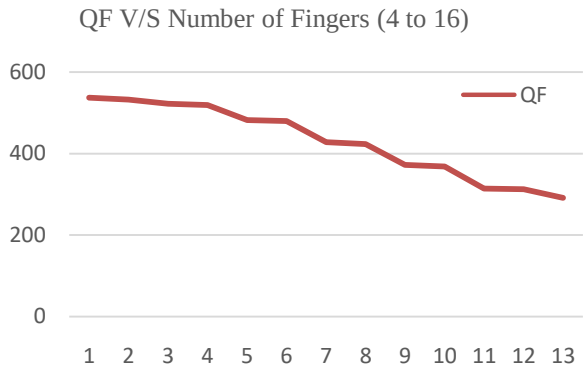

Fig. 21. Number of Finger V/S QF

The figure 20 show the capacitance of an interdigital capacitor with respect to number of fingers. The number of fingers are directly related to capacitance value such that is seen in number of the fingers will increase thecapacitance

value. The figure 21 as shows the quality factor with respect to number of fingers. The number of fingers will effect to decreases the quality factor.

The space between the fingers is also directly related to capacitance value shows in figure 22 and 23. As the space between the fingers increases the capacitance value also increases by keeping conductor width, anddielectric is value constant. This can be tested for fingers of 4 to 10. In each case (number of fingers) the space between the conductor is varied from 0.5mm to 2mm.

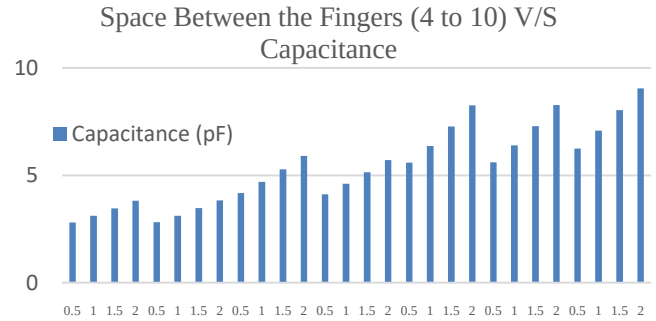

Fig. 22. Space Between the Fingers V/S Capacitance

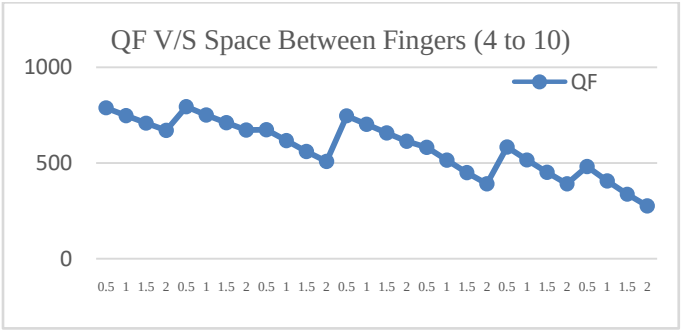

Fig. 23. Space between the Fingers V/S QF

6. CONCLUSION

The observed results of an inter digital capacitors show that an increase the finger width, numbers of fingers and space between the fingers will effect to increase the capacitance value. The total size of Inter digital capacitor increases with decreases in the quality factor because of the increasing reactive resistance and inductance participate in dissipation of energy. The designed capacitor structures are very small in size of the order of 7mm×13mm (4-fingers) to 13mm×30mm (16-fingers),and this it helps to design desired capacitor in small area with higher quality factor. The capacitors are preferably used as biomedical sensors, RF/Microwave, RADAR and in satellite communication applications. This work helps to know the design and optimization of interdigital capacitor for desired value in particular applications.

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