QPSK MODULATOR FOR X-BAND IRS SATELLITES

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Abstract

The current work is applied to remote sensing satellites. IRS satellites in the orbits are not only sending data to Indian ground stations but also to other international stations for passing data to different countries. Multiple solid-state cameras are carried by the IRS satellite to operate in the visible and infrared bands that acquires imageries for earth survey such as agriculture and geology. Digital phase modulation that allows transmitting discrete phase angles is more popular and easily adaptable. Among the PSK schemes, the QPSK is adopted as it is relatively easy to realize and gives optimum performance in terms of power and bandwidth compared to other modulation schemes. The unit is realized in MIC form, which is smaller in size and weight compared to earlier ones. The data obtained from onboard camera is transmitted to ground on X-band carrier (8-8.4GHz). Keeping in view the future satellite applications, a QPSK modulator is designed with LVDS interface circuit for a data rate of upto 105 Mbps. The microwave simulation software used is EESOF.

Keywords: *Hybrid Coupler, Wilkinson Power Combiner, Thin Film Technology.*

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1. INTRODUCTION

This work emphasizes the simulation and testing of a QPSK modulator for Indian Remotes Sensing satellites with the intention of having a data rate upto 105Mbps. The entire modulator is housed in MIC form using microstrip techniques. The operating frequency range is X-band (8-8.4GHz). For optimum performance simulation and test results are done for a band of 600MHz range.

QPSK modulator in the parallel configuration consists of a quadrature power divider, two BPSK modulators and an in-phase power combiner. Parallel configuration is preferred because of good amplitude and phase imbalance. Here carrier signal is divided by an in-phase, 3-dB hybrid coupler and applied to two identical BPSK modulators on both arms. The output of BPSK modulators is combined in a power combiner to produce the desired QPSK signal.

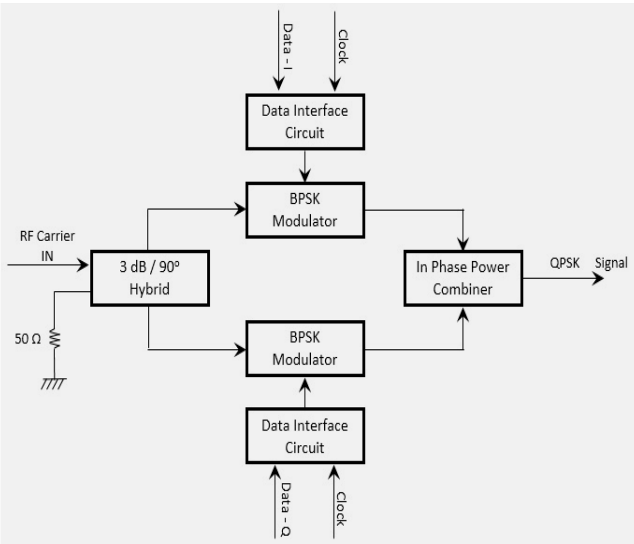

Fig-1: Parallel configuration of QPSK Modulator

1.1Hybrid Coupler

A 3dB, 90° hybrid coupler [4] is a four-port device that splits an input signal equally with a resultant 90° phase shift between output ports or combines two signals while maintaining high resolution between the ports.

A signal applied to port 1 gets equally split between ports 2 and 3 with one of the outputs exhibiting a relative 90° phase shift. Almost all the signal applied to port 1 is transmitted to loads connected to ports 2 and 3 that are properly terminated into matching impedances. Port 4is termed ''isolated 'and receives negligible power.

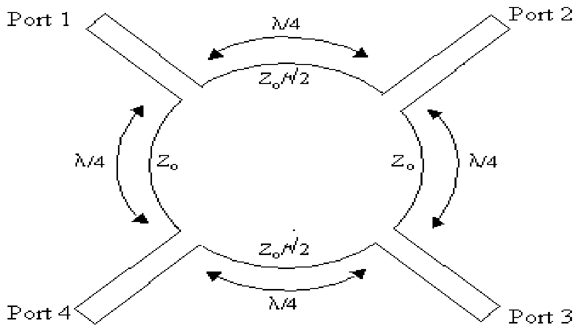

Fig-2: 90° Hybrid

Table-1: 3dB Hybrid phase Truth table

	Port 1	**Port 2**	**Port 3**	**Port 4**
Port 1	-	Isolated	-3dB -90˚	-3dB 0˚
Port 2	Isolated	-	-3dB 0˚	-3dB -90˚
Port 3	-3dB -90˚	-3dB 0˚	-	Isolated
Port 4	- 3dB 0˚	-3dB -90˚	Isolated	-

1.2 Wilkinson Power Combiner

Wilkinson power combiner combines the two bi-phase modulated signals. The output port isolation is achieved through a resistor. When divider splits a signal or combines coherent signals, each side of the isolation resistor is at equal potential and therefore no current flows through the resistor and no power is dissipated.

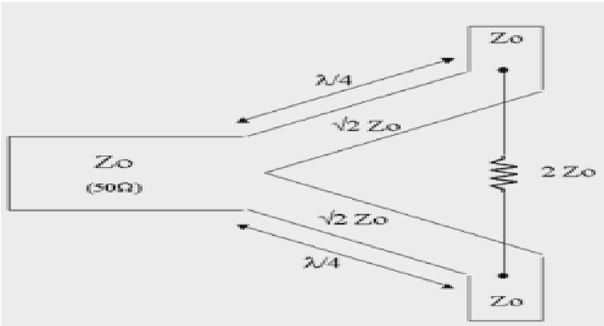

Fig-3: Uncompensated Wilkinson Power combiner

The simple Wilkinson power combiner [2]supports limited bandwidth applications. Since bandwidth required is more for current application, a broad band combiner is designed. The simulation results show that there is improvement in bandwidth by choosing compensated Wilkinson power combiner. The performance is improved by adding a λ/4 transformer in front of the power division step and a shift in the impedance levels.

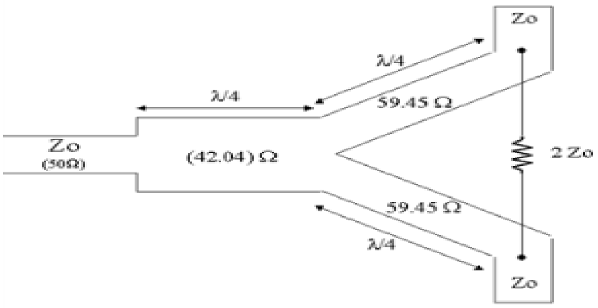

Fig-4: Compensated Wilkinson Power combiner

The output VSWR in uncompensated circuit is better than in compensated circuit, while input VSWR in compensated circuit is better. Therefore, the choice may be dictated by input/output characteristic as well as whether necessary space exists to add the extra quarter wave transformer.

2. DESIGN AND FABRICATION

MIC modulates two data streams provided by the base band system on X-Band carrier. The MIC is fabricated on Alumina substrate using microstrip line techniques and thin film technology. The two bi-phase modulators are hybrid reflection type and use a pair of high-speed PIN diodes (HPND 4050) as switching elements.

2.1 Choice of substrate

Dielectric constant is generally the first parameter to look for when choosing a microwave substrate material. It governs whether the circuit will fit in the allotted space or not and operate in its required frequency range. The material suitable for our application was found to be alumina with ε_r 9.8. It is made of polycrystalline Al2O3with small amounts of metal oxide glasses to achieve certain physical properties. Alumina is available in sizes ranging from 0.01″ to 0.05″ or greater and variety of shapes and design.

2.2 Design Equations

Hybrid coupler:
For Alumina Substrate $\varepsilon_r = 9.8$, h= 0.625mm, t=.005mm. At X-Band, f=8.2 GHz

Width of the transmission line [2]:
$W / h = 8e^{A} / (e^{2A} - 2)$ where
$A = (Z_o / 60) \sqrt{} (\varepsilon_r + 1) / 2 + (\varepsilon_r - 1 / \varepsilon_r + 1) (0.23 + 0.11/ \varepsilon_r$
For 50Ω,
W / h = 0.975 => W = 0.61mm
For $Z_o / \sqrt{2} = 35.35\Omega$,
W = 1.17mm

λ / 4 length:
For 50Ω, $\lambda = \lambda_o / \sqrt{\varepsilon_{eff}} = c / f \sqrt{\varepsilon_{eff}}$
Since $W / h \leq 1$,
$\varepsilon_{eff} = (\varepsilon_r + 1) /2 + (\varepsilon_r - 1) /2 [(1 + 12 h / W)^{-½} + 0.04 (1 - W /h)^2]$
So, $\varepsilon_{eff} = 6.6$
λ = 14.24mm,λ / 4 = 3.56mm
For 35.35Ω, since $W / h \geq 1$,
$\varepsilon_{eff} = (\varepsilon_r + 1) / 2 + (\varepsilon_r - 1) / 2 (1 + 12 h / W)^{-½}$
So, λ / 4 = 3.45mm

Ring radius:
λ / 4 = 2πr / 4 = 3.56mm
r = 2.26mm (for 50Ω)
= 2.19mm (for 35.35Ω)

Power combiner:
$W / h = 8e^{A} / (e^{2A} - 2)$ where
$A = (Z_o/60)\sqrt{} (\varepsilon_r + 1) /2 + (\varepsilon_r - 1/ \varepsilon_r + 1)(0.23 + 0.11/ \varepsilon_r)$
$\varepsilon_{eff} = (\varepsilon_r + 1) / 2 + (\varepsilon_r - 1) / 2 (1 + 12 h / W)^{-½}$
$\lambda = \lambda_o / \sqrt{\varepsilon_{eff}} = c / f \sqrt{\varepsilon_{eff}}$
λ / 4 = 2πr / 4

Table-2: Design values for power combiner

Z(Ω)	W(mm)	ε_{eff}	λ/4(mm)	r(mm)
70.7	0.27	6.27	3.65	2.32
42.04	0.85	6.8	3.5	-
59.45	0.41	6.42	3.6	2.29

2.3 Schematic And Simulation

The design of hybrid coupler and power combiner is fabricated on the alumina substrate using thin film technology. The schematics obtained using the simulation tool is given in fig-5and fig-6.

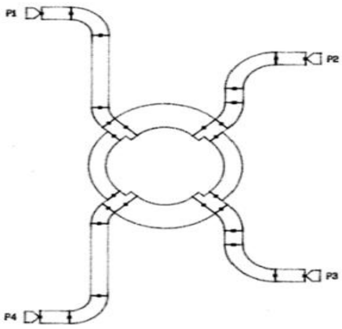

Fig-5: Schematic of hybrid coupler

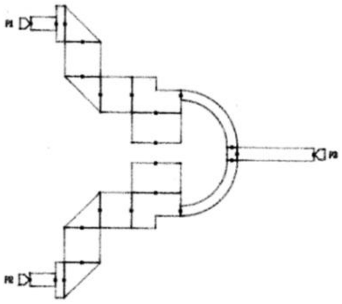

Fig-6: Schematic of power combiner

3. SIMULATION AND TEST RESULTS

3.1 Test Set-Up For QPSK Modulator

Modulator is basically tested for two conditions: static and dynamic. In dynamic condition the carrier suppression with 1010…..data and spectrum with random data is observed.

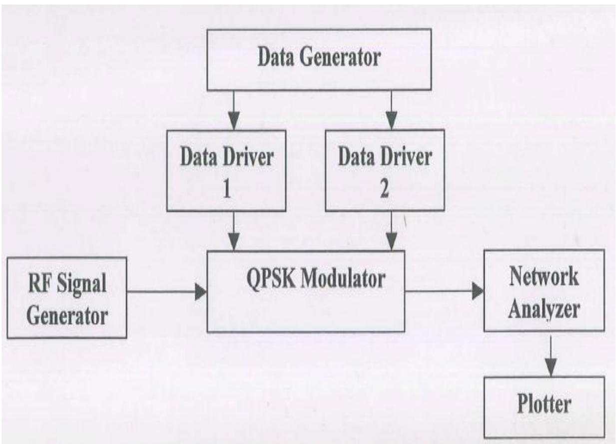

Fig-7: Test set-up

The base band systems and RF systems are placed in different deck plates in the spacecraft. Because of this, the coaxial cables between the two systems will be around 4 meters in length. The disturbed parasitic reactance of the cables deteriorates the rise time and fall time of the data. To solve this problem, an interface circuit using Low Voltage Differential Signaling (LVDS) chips are incorporated to forward/ reverse bias the PIN diodes of the modulator. The TTL levels are converted to bipolar levels using transistors.

This work replaces the TTL circuit which has a frequency limitation. With LVDS, higher data rates can be achieved.

FREQ-GHZ	DB[S21] HYB	DB[S31] HYB	ANG[S21] HYB	ANG[S31] HYB	DB[S11] HYB	DB[S22] HYB	DB[S33] HYB	DB[S44] HYB	DB[S41] HYB
8.00000	-3.164	-3.085	-14.931	-104.938	-24.144	-24.268	-24.268	-24.144	-24.703
8.05000	-3.137	-3.089	-18.236	-108.253	-25.959	-26.115	-26.115	-25.959	-26.640
8.10000	-3.116	-3.093	-21.550	-111.567	-28.243	-28.334	-28.334	-28.243	-29.064
8.15000	-3.100	-3.097	-24.871	-114.880	-31.326	-30.956	-30.956	-31.326	-32.155
8.20000	-3.088	-3.102	-28.197	-118.192	-36.082	-33.492	-33.492	-36.082	-35.592
8.25000	-3.082	-3.106	-31.528	-121.505	-46.047	-33.980	-33.980	-46.047	-36.133
8.30000	-3.081	-3.110	-34.861	-124.818	-41.568	-31.822	-31.822	-41.568	-32.907
8.35000	-3.085	-3.114	-38.196	-128.133	-34.205	-29.145	-29.145	-34.205	-29.666
8.40000	-3.093	-3.119	-41.531	-131.450	-30.203	-26.820	-26.820	-30.203	-27.113
8.45000	-3.107	-3.123	-44.865	-134.770	-27.463	-24.892	-24.892	-27.463	-25.085
8.50000	-3.126	-3.127	-48.198	-138.094	-25.378	-23.275	-23.275	-25.378	-23.425
8.55000	-3.149	-3.131	-51.527	-141.422	-23.694	-21.893	-21.893	-23.694	-22.029

Fig-8: Simulation results for hybrid coupler (snapshot from EESOF)

Freq GHz	db [S21]	db [S31]	Ang S21	Ang S31	db [S41]	db [S11]	db [S22]	db [S33]	db [S44]
8.0	-3.47	-3.9	80.9	172.6	-20.1	-15.6	-18.1	-14.9	-24.2
8.05	-3.56	-4.00	73.5	164.6	-22.0	-16.9	-19.4	-16.5	-20.6
8.1	-3.42	-4.00	66.8	157.3	-24.6	-14.2	-19.8	-16.8	-20.0
8.15	-3.42	-3.98	58.5	151.7	-22.3	-13.5	-22.7	-17.1	-21.6
8.2	-3.65	-3.90	51.2	144.1	-21.6	-16.7	-19.3	-14.6	-23.3
8.25	-3.83	-3.88	45.6	139.4	-20.1	-18.1	-16.4	-15.5	-23.4
8.3	-3.74	-3.92	38.8	131.7	-26.1	-17.5	-17.8	-15.2	-25.8
8.35	-3.85	-3.87	31.8	124.2	-27.5	-23.7	-16.4	-15.2	-31.9
8.4	-3.84	-3.80	25.6	117.8	-30.2	-32.5	-11.0	-14.4	-20.9
8.45	-3.77	-3.68	20.3	111.1	-32.8	-21.6	-10.6	-15.3	-17.8
8.5	-3.70	-3.88	13.4	102.3	-24.9	-18.0	-13.6	-17.8	-21.6
8.55	-3.61	-3.78	6.2	95.9	-23.5	-19.8	-17.3	-21.0	-23.8
8.6	-3.56	-3.67	0.4	88.9	-19.7	-16.8	-22.2	-31.4	-18.4

Fig-9: Hardware test results for hybrid coupler

FREQ-GHZ	DB[S31] CC	DB[S32] CC	ANG[S31] CC	ANG[S32] CC	DB[S11] CC	DB[S22] CC	DB[S33] CC
8.00000	-3.065	-3.065	18.476	18.476	-23.264	-23.264	-33.073
8.05000	-3.067	-3.067	15.903	15.903	-24.484	-24.484	-30.704
8.10000	-3.069	-3.069	13.330	13.330	-25.867	-25.867	-28.967
8.15000	-3.071	-3.071	10.756	10.756	-27.437	-27.437	-27.627
8.20000	-3.073	-3.073	8.182	8.182	-29.184	-29.184	-26.561
8.25000	-3.076	-3.076	5.607	5.607	-30.975	-30.975	-25.697
8.30000	-3.078	-3.078	3.029	3.029	-32.334	-32.334	-24.992
8.35000	-3.080	-3.080	0.448	0.448	-32.474	-32.474	-24.412
8.40000	-3.083	-3.083	-2.136	-2.136	-31.266	-31.266	-23.936
8.45000	-3.085	-3.085	-4.724	-4.724	-29.461	-29.461	-23.549
8.50000	-3.086	-3.086	-7.317	-7.317	-27.632	-27.632	-23.236
8.55000	-3.088	-3.088	-9.917	-9.917	-25.968	-25.968	-22.987

Fig-10: Simulation results for power combiner (snapshot from EESOF)

Freq	db [S31]	db [S32]	Ang S21	Ang S31	db [S11]	db [S22]	db [S33]
8.0	-3.8	-4.01	-107.86	-108.37	-18.9	-25.5	-14.6
8.05	-3.8	-4.0	-113.09	-113.54	-18.0	-24.4	-12.3
8.1	-3.8	-3.9	-119.74	-120.66	-19.1	-26.6	-13.5
8.15	-3.8	-3.9	-125.63	-126.76	-17.5	-22.6	-16.5
8.2	-3.8	-3.9	-129.85	-130.31	-13.7	-16.5	-15.6
8.25	-3.9	-4.0	-137.36	-138.43	-13.1	-15.9	-13.4
8.3	-3.9	-3.9	-142.33	-143.31	-15.2	-19.5	-14.6
8.35	-3.9	-3.9	-148.68	-149.95	-16.6	-21.9	-13.4
8.4	-4.0	-4.1	-153.82	-154.75	-14.7	-19.8	-10.0
8.45	-4.4	-4.37	-159.46	-160.63	-14.8	-19.7	-9.71
8.5	-4.3	-4.2	-165.88	-167.56	-19.8	-36.0	-11.3
8.55	-4.2	-4.1	-170.59	-171.56	-22.4	-35.2	-11.6
8.6	-4.28	-4.12	-175.32	-176.41	-22.1	-30.7	-13.9

Fig-11: Hardware test results for power combiner

Fig-8 shows that simulation results are tuned to a frequency around 8.2GHz to 8.4GHz. Though overall hardware results are comparable to the simulation results it is approximately tuned between 8.2GHz to 8.35GHz. Theoretically the insertion loss between the port 2 and port 3 of the hybrid coupler should be 3dB. From simulation the difference between the ports is 0.02dB around the desired frequency range. There is 0.25dB difference in hardware results around the same frequency range. The maximum phase imbalance is around ±2°. The return loss is also equally good around the desired frequency varying between 15dB to 25dB.

The difference in the hardware results in the both the designs are due to the microstrip loss, connector loss, and junction discontinuities. The units have been tested on test fixtures where perfect grounding is not possible which is very important for microstrip lines.

3.2 Layout And Test Results Of QPSK Modulator

Fig-12 shows the layout of the QPSK modulator for fabrication on the substrate. The blank spaces in rectangular shape are the space isolators to be placed at the input and output ports.

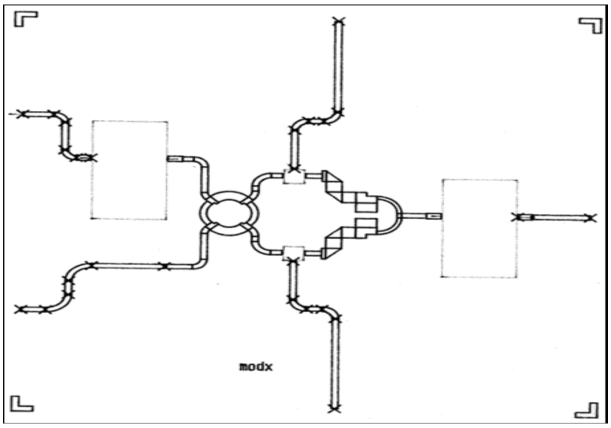

Fig-12: Layout of QPSK modulator

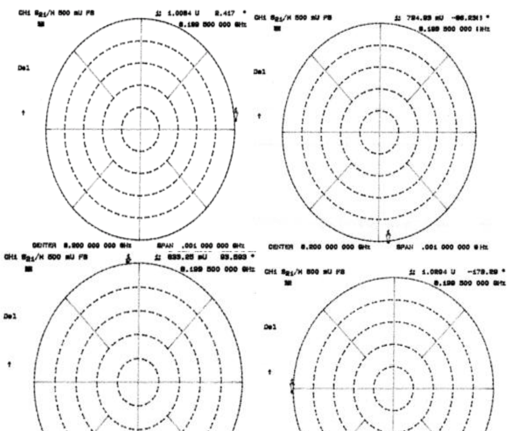

Fig-13: Phase plots of QPSK

Table-3: Phases of four states in the desired frequency band (Hardware test results)

Freq (GHz)	Phase in degrees			
	00	01	10	11
8	0	-86.5	90	179.8
8.1	-1.2	-89.2	87.3	176.9
8.2	1	-86.2	93.5	179.3
8.3	0	-94	94	177.8
8.4	1.4	-88.7	91.3	178.2

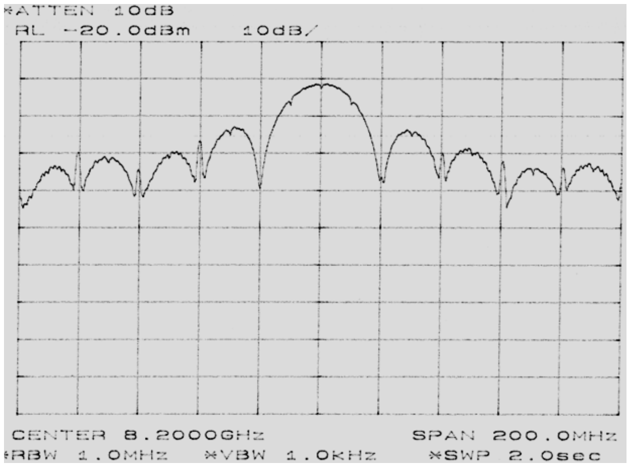

Fig-14: QPSK spectrum (from spectrum analyzer)

The dc content in the random data results in the spikes in the QPSK spectrum.

CONCLUSION AND FUTURE WORK

The modulator is designed using microstrip lines on Alumina substrate with thin film technology, for a center frequency of 8.2GHz. The simulation and test results are compared and seen to match to a large extent.

Since the bandwidth is limited at X-band, higher modulation schemes are to be explored in the future scope. As an extension of this work 8-PSK design has been taken up to converse the bandwidth at the cost of power requirements. With proper housing the modulator will be tested for environmental conditions like temperature, vibration, hot and cold tests etc. then the bandwidth achieved is not at the desired frequency. The frequency shift can be corrected by redesigning to a higher frequency so that frequency dispersion is taken care of.

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