DESIGN AND IMPLEMENTATION OF AMBA-MEMORY CONTROLLER FOR IMAGE TRANSFER APPLICATIONS

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Abstract

Real time system is dependent on its real time system interconnect architecture characteristics. It determines its performance. If system interconnect is not designed effectively it can affect communication between memory or between peripheral devices and various memory. Hence memory access time has become a bottle neck which in turn boundaries system performance. Memory controller is considered to tackle problem. Interconnection system known as AMBA is an efficient specification for management of functional blocks. This paper concentrates on effective design of a memory controller using AMBA bus protocol for memory image transfer applications. Memory controller is designed using conventional finite state machine. AMBA is implemented on Xilinx spartan6 FPGA chip

Key Words: *Advanced microcontroller bus architecture, Finite state machine, Memory controller*

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1. INTRODUCTION

Embedded system comprises of various computational elements. Various elements in an embedded system performs specific task to archive the desired result. Consider setup box of a tv as an example [1].A simple setup box performs multiple functions. Initially it splits incoming signal into various sub signals. In next phase it converts video signals to actual tv signals. Similarly audio signals are also changed. Moreover an additional job is to handle input that user gives for changing channel using a remote. These operations needs to be completed at same time .Also should be completed within a time limit. Failure in doing so will result in erroneous conditions such as blank screen. Nowadays a number of devices are integrated into same chip. A processor needs to communicate with all devices connected to it such as other processors, memories, I/O devices, in order to complete a task. Since 1983 microprocessors have improved at a rate of 61% in a year. In contrast, time to access memory has improved by less than 9%.Hence designers face a problem with performance of system. A major problem is to handle storage of data and simultaneous memory access. Usually higher volumes of datas are handled using dynamic memory. But dynamic memories is less efficient to access different locations in random and also it requires refreshing otherwise datas will be lost. In order to efficiently communicate between various blocks, memory controllers are designed. Memory controller generates signals to control read and write information's connecting memory and this memory with other parts of system. System-on-chip proposals have several different components such as external interface IP that needs to mutually communicate. In SOC design, some modules might be designed from launch; others are taken from previous available designs either can be produced from externally through vendors. Each component has an interface to the external world. Selection of pins at interface is determined by selected bus procedure for communication. In order to assimilate all components into SOC design, it is necessary to have a regular interface explanation for components. If standard is not defined the component interfaces will not be compatible with bus implementation, and function will not be executed appropriately.

To increase speed of SOC incorporation over several designs, deferent bus communication architecture criterions have been projected. Communication based on bus standards shows interface between components and bus. Numerous architecture standards give designers freedom to design bus in different ways. This paper proposes an effective design of a memory controller using AMBA bus protocol particularly for image transfer applications.

2. ARCHITECTURE OF MEMORY CONTROLLER

A memory controller is a chip on CPU die which manages data flow between memory and various devices. It can be isolated or incorporated into desired chip. Memory controllers succeed read and write operations. It selects appropriate circuit for data storage and retrieval. It acts as middle man in various operations, as it ensures that proper informations are retrieved from the right locations.

2.1 Detailed Description of Memory Controller

Advanced Microcontroller Bus Architecture (AMBA) design is a standard for on-chip communications. It is used in designing microcontrollers with extraordinary concert. AHB is a new version of AMBA bus. It is used in applications where high performance is required. Its major function is to fulfill necessities of high-performance designs.[2] AMBA controller has features necessary for

high clock following such a i) burst transfer ii) split transactions iii) Wider data bus configurations.

The system consists of mainly two modules AMBA controller, memory controller.

A) AMBA Controller

AMBA protocols are open standards. It is an interconnect specification. It is used for connecting and managing functional blocks in a SOC. AMBA controller converts incoming signal to a conventions used by memory controller, some optimizations are made to improve performance. It can be designed with synthesizable HDL for ASIC synthesis. It also supports multiple memory devices and shared path for datas between memory devices. It reduces pin number. AMBA protocols are standards for 32-bit embedded Processors. Main target of AMBA is to help designer of embedded system to meet challenges like low power consumption, to facilitate development of embedded device products with multiple CPUs or signal processors, to become technology-independent and to develop modular system. It also sees that silicon required is less; also support on-chip and off-chip communication effectively for numerous operations and testing.

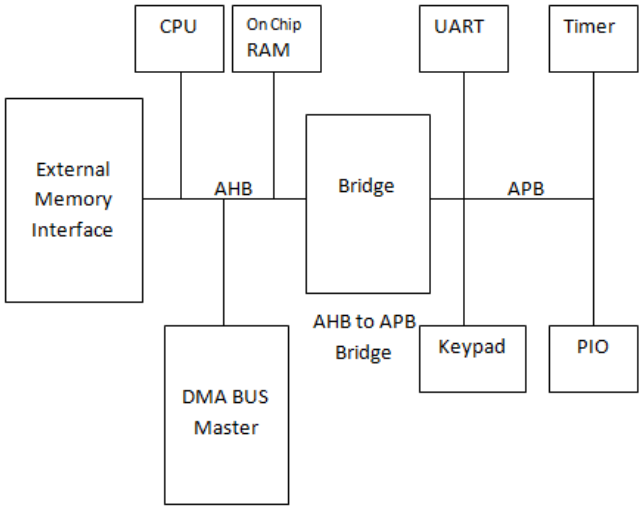

Fig -1: AMBA-architecture

AMBA architecture mainly include a master which initiates all transfers and a slave which responds to the commands issued by master.It also has a bridge which connects master and slave.Master has a complex interface..It has address generator and it also has controller.An AMBA high performance slave responds to the commands initiated by the master.

Features of AHB - controller

- Follows AMBA AHB protocol
- It has VHDL / Verilog RTL source
- Supports various memory devices
- provides test bench and required verification vectors to perform a function.
- Shared path for data between memory devices .
- Reduces pin number
- Supports AHB single beat, 4 beat and 8 beat wrapping
- supports split transaction
- Supports up to four memory banks .
- Supports Programmable and configuration registers

AMBA - Memory controller interface for image transfer application architecture is shown below:

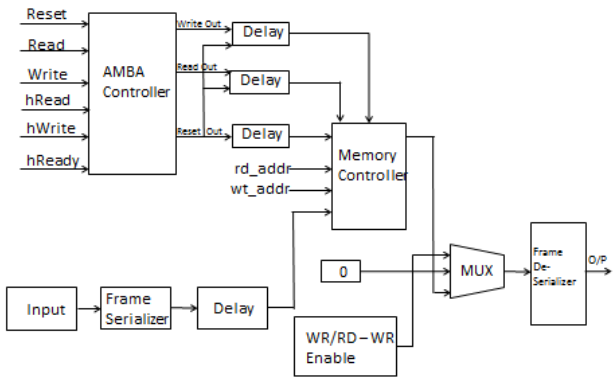

Fig -2 Architecture of AMBA-Memory controller interface

When the input is given it is passed through frame serializer which will convert the input to one dimensional format. Delay element will provide necessary synchronization. Memory controller will work as per AMBA protocol. Memory controller is designed using finite state machine.Mux is used for low power enhancement. After these functions are done output of mux is given to frame deserializer which will retrieve the original data and give it as output

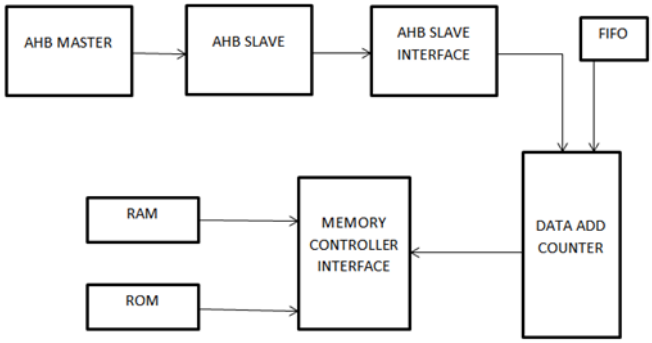

Fig -3 Top architecture of AHB memory controller

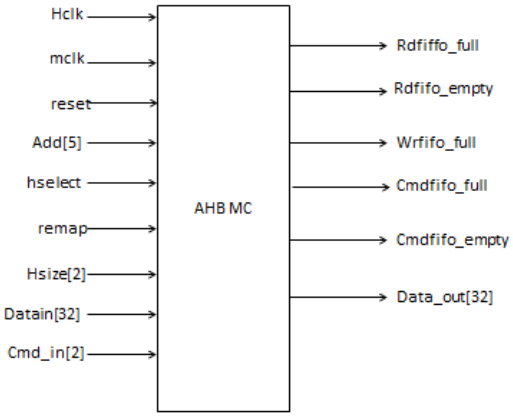

Fig -4: Overall input and output of AHB MC

B) Memory controller

A memory controller manages data flow. It is a digital circuit. It can be placed with another chip or can be separate chip. When a memory controller is integrated to a microprocessor, it reduces memory latency also it increases the system performance. Here memory controller is designed using finite state machine (FSM).memory controller has three states namely read, write and read/write. If HReady signal is active low, controller will stay in initial state; if HReady signal is high, based on signal received by the controller, it goes to read or write state. If Write signal is high, controller goes to write state only if read signal is low at that time; if Read signal is high, system enters into read state at that time write should be low. If HReady signal is low, system moves back to start state; it remains in this state till HReady signal turn into active.

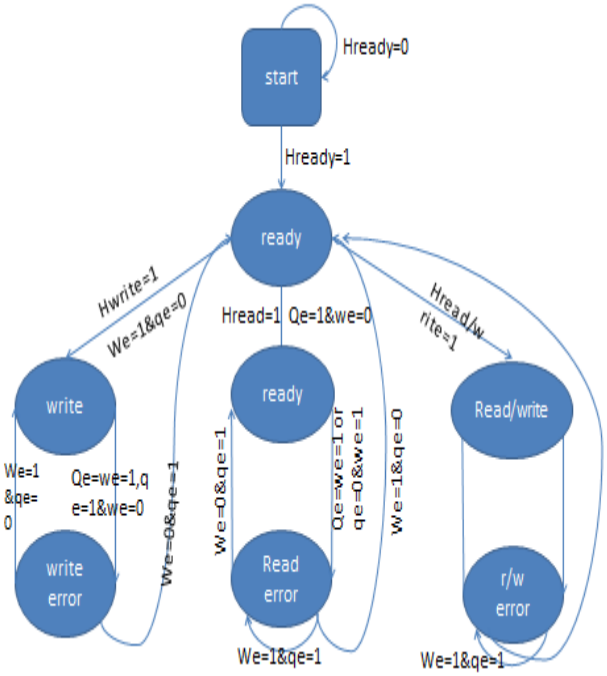

Fig -5: FSM model of Memory controller

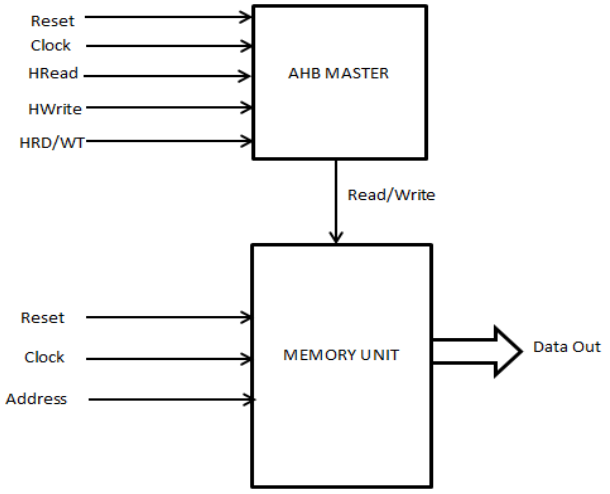

Fig -6 :AHB MC interfacing

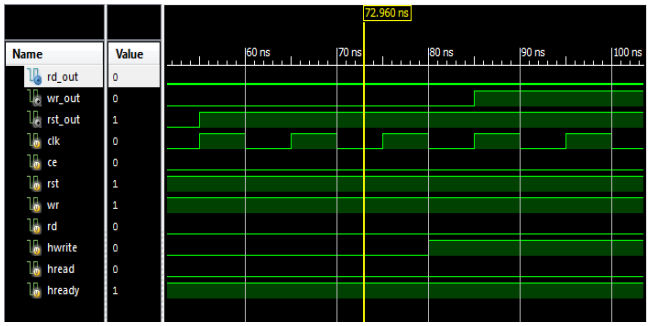

Fig -7: Simulation result of AMBA controller

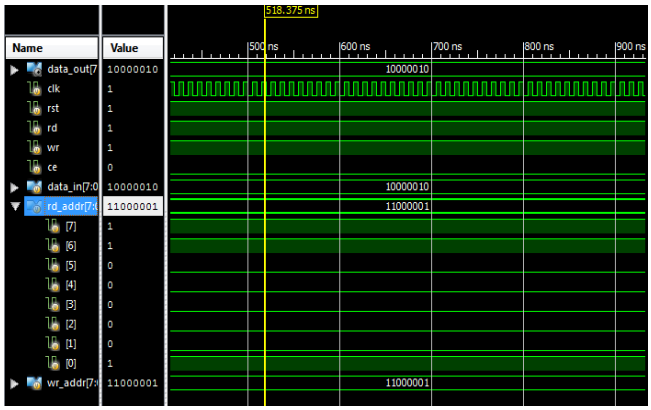

Fig -8: Simulation result of memory controller

3. CONCLUSION

The read write operations are accomplished with zero wait states. Data transfer operations will be fast due to parallel communication. Power dissipation is becoming a limiting factor due to increasing device and clock rates. This architecture optimizes power to 412mW. Design is synthesized on Xilinx 13.1 spartan3.

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BIOGRAPHIES

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