A STUDY ON VARIOUS STRUCTURES OF ADDERS AND TO SUGGEST A BEST CHOICE FOR LOW POWER APPLICATIONS

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Abstract

The basic building blocks of the arithmetic unit in a processor are adders. These adders are responsible for performing Arithmetic operations in most of the computing systems. Addition is the base for arithmetic operations such as multiplication and the basic adder cell can be modified to function as subtractor and also can be used for division. Therefore, one bit Full Adder cell is the most important and basic block of an arithmetic unit of a system. In today's modern electronics world, low power engineering has a good market starting from mobile phones to hand held devices. So, in this paper a study is carried out on different structures of adder by considering power as the constraint and a best choice is suggested for low power applications.

Keywords: *Adders, Low Power, Microwind.*

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1. INTRODUCTION

Full adder is a combinational circuit with reduced circuit complexity. A full adder adds binary numbers and accounts for values carried in as well as out. A one-bit full adder adds three one-bit numbers, often written as *A*, *B*, and *C*; *A* and *B* are the operands, and *C* is a bit carried in from the previous less significant stage. The full adder is usually a component in a cascade of adders, which add 8, 16, 32, etc. bit binary numbers. Thus it is used as the principle component in ALU block of different processor chips like signal processing, floating point processors, and in FPGAs. This Block is used to make operations like Add, subtract, Multiply etc. It can be used to construct a ripple carry counter to add an n-bit number. Besides addition, adder circuits can be used for a lot of other applications in digital electronics like address decoding, table index calculation etc.,

As the impressive advancement is witnessed by electronics industry due to portable devices, power consumption plays a vital role as these devices are battery operated. Hence there is a vital requirement to design a basic building block, an adder, which consumes less power.

The paper is organized section wise. Section 2 describes the various full adder topologies. Section 3 illustrates the simulation of the topologies which are discussed in previous section. The simulation results are analyzed and compared in Section 4. Finally, Section 5 concludes the paper.

2. VARIOUS STRUCTURES OF ADDERS

2.1 Basic Full Adder

Adder is the building block for most implementations of these operations [1–4]. Full Adder is a logic circuit that adds a pair of corresponding bits of two numbers expressed in binary form and any carry from a previous stage producing a sum and a new carry. It is also called a three input adder.

The general expression for full adder can be given as

$$Sum = A \hat{} B \hat{} C \quad (1)$$

$$Carry = A.B + B.C + C.A$$

$$= A.B + (A \hat{} B).C \quad (2)$$

The symbol ^ denotes an XOR operation. The above equations are implemented with the help of gates as shown in Fig.1

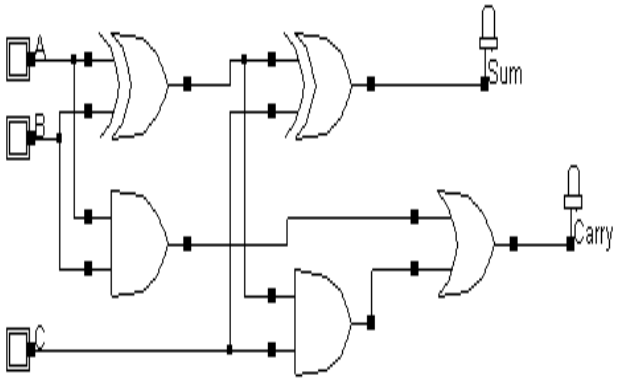

Fig.1. Basic Full Adder Circuit

The truth table for the full adder can be given as shown in Table 1.

Table 1: Truth Table of Full Adder

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

2.2 Full Adder Using XOR and Multiplexer

The full adder can also be designed using two XOR gates and a Multiplexer. This circuit will require a minimum number of transistors when compared to the basic adder. The multiplexer will output the data from the input based on the status of the select line. A 2:1 Multiplexer is used to implement the carry logic [3-4] and no change is done with respect to the sum output of a full adder.

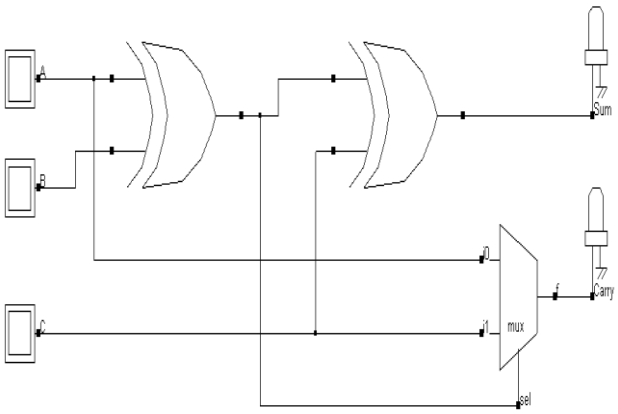

Fig.2. Full Adder using XOR and Multiplexer

2.3 Full Adder Using 6T XOR

The XOR gates in Fig2 can be replaced with 6 Transistor XOR gates. The multiplexer can be implemented with the help 2 transistors. So the two XOR in the Fig.2 requires 12 transistors [5] and the multiplexer requires 2 transistors. Hence a sum of 14 transistors are required to implement the circuit as shown below in Fig.3.

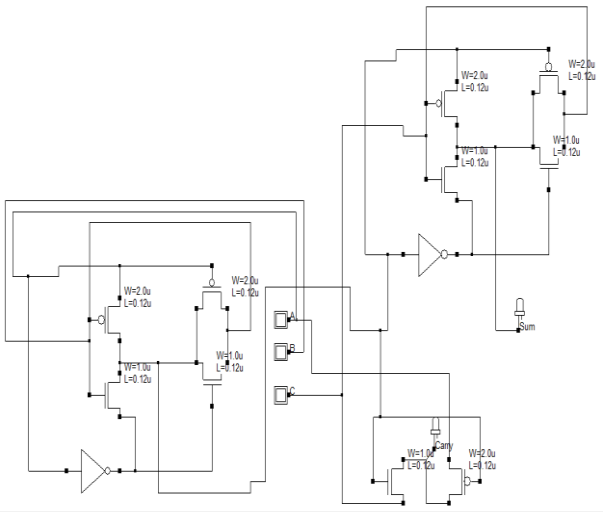

Fig.3. Full Adder using 6T XOR gate

3. SIMULATION OF ADDER STRUCTURE

3.1Full Adder

The simulation result of basic full adder using Microwind is shown in Fig. 4(a) and 4(b). The Fig. 4(a) depicts the Layout of the circuit shown in Fig. 1

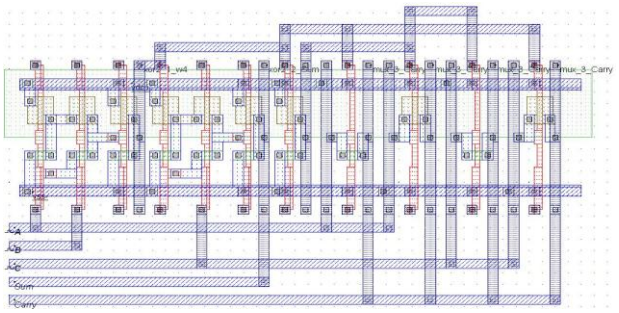

Fig. 4 (a) Layout of Basic Full Adder

The inputs are applied to this generated layout to verify the functionality. The results obtained are shown in Fig. 4(b).

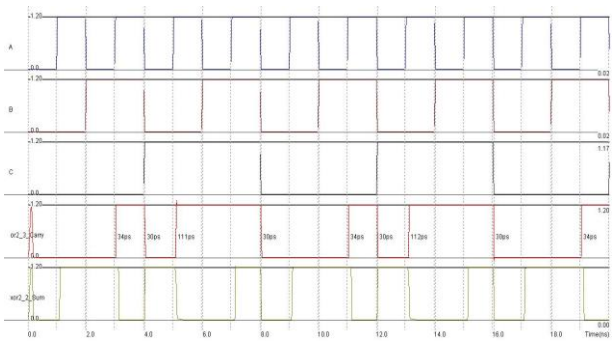

Fig.4 (b). Output Waveform of Basic Full Adder

3.2Full Adder Using XOR and Multiplexer

The Full Adder using XOR and Multiplexer as shown in Fig.2 is simulated. The layout and output waveforms are shown in Fig 5 (a) and (b) respectively.

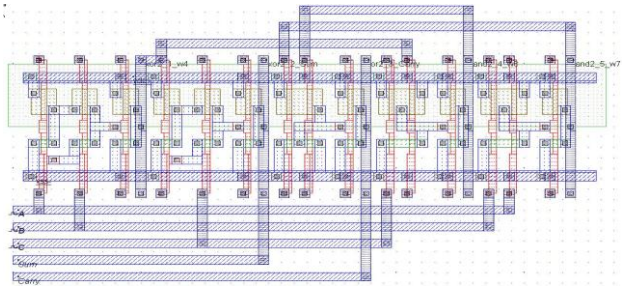

Fig.5 (a) Layout of Full Adder using XOR and Multiplexer

The Three inputs A, B and C are provided with 1.20 V and the sum and Carry outputs are recorded. The truth table shown in Table I is verified. The simulated output is shown in Fig. 5(b)

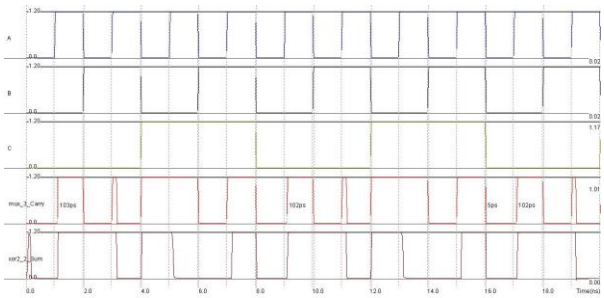

Fig.5 (b) Output Waveform of Full Adder using XOR and Multiplexer

3.3Full Adder Using 6T XOR

The Full Adder using 6 Transistor XOR gates is simulated as shown in Fig. 3. The Layout of this topology is shown in Fig. 6(a) and the output waveform obtained from this layout is shown in Fig. 6(b). All the combinations in the truth table of a full adder is successfully verified.

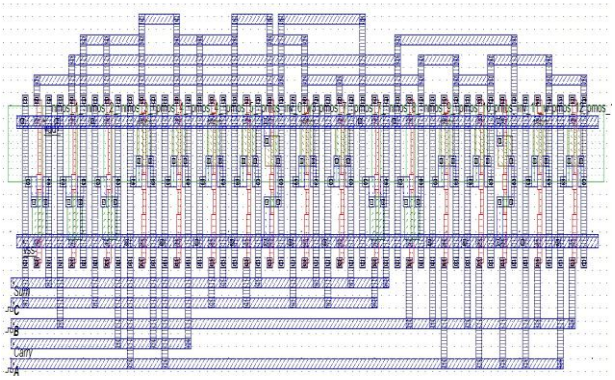

Fig 6. (a) Layout of Full Adder using 6T XOR

Fig. 6 (b) Output waveform of Full Adder using 6T XOR

4. RESULTS AND DISCUSSION

The simulated results shows that all the three topologies under discussion generate the expected outputs. As we are interested in low power applications, the comparison is made by considering the area and the power consumption of each topology. It is shown in Table 2.

Table 2. Comparison of Different Topology

Topology	Area	Power
Basic Full Adder	0.18nm	11.404 µW
Full Adder with MUX	0.168nm	9.272 µW
Full Adder with 6T XOR	0.3nm	4.184 µW

The graph below shows the area and power for different topologies

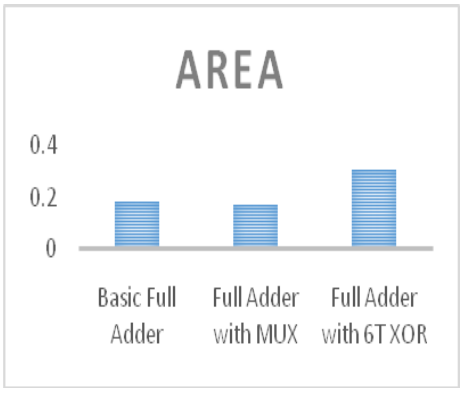

Fig. 7. Comparison of Different Topologies for Full Adder by Considering Area

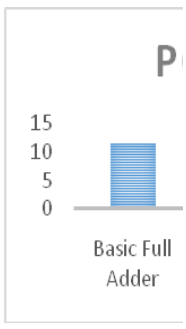

Fig. 8. Comparison of Different Topologies for Full Adder by Considering Power Consumption

5. CONCLUSION

The power consumption for three different topologies are analyzed in this paper. The result show that the Full Adder topology with 6 transistor XOR consumes less power.But the traditional Full Adder is an area efficient. Hence the full adder with 6 transistor will reduce power consumption at the cost of area.

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BIOGRAPHIES

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