

# FINFET BASED 16 BIT ALU UNITS FOR LEAKAGE REDUCTION

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## Abstract

An Arithmetic Logic Unit (ALU) acts as a heart for all microprocessors. It performs logical or arithmetic operations. It's getting smaller and more complicated in recent days to enable the progress of extra powerful however smaller design. However, there are just a few limiting reasons that slow down the growth of smaller and additional problematic chip when CMOS is used. The foremost boundaries in scaling the bulk CMOS are quick channel effects, sub-threshold leakage and gate-dielectric leakage. FinFET has an excellent control on short channel results within the sub-micron regime hence developing the probability to scale the transistor. Because of this cause, the small size transistor can have a higher intrinsic gain and less off-state current in comparison with the bulk counterpart. 16-bit ALU that performs basic logical, arithmetic, and shifting operations has been designed using FinFET constructions and leakage power has been studied and compared with the MOSFET structure.

**Keywords:** Adaptive Clustering, Contour Marking, Edge Map Extraction, GLDM.

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## 1. INTRODUCTION

In today life, the needs of portable electronic gadgets are increasing day-to-day. However issues like power consumption, dimension and capability still exist and need to be overcome in the existing designs. Power consumption is the fundamental trouble in VLSI design. As per the recent developments in technology, the number of transistors is continuously growing on a chip that increases the complexity and power consumption of a chip. The expanded power consumption results in increase in the temperature of the chips, which impacts on the circuit efficiency. Accordingly, it is very significant to care for these issues. Adders and multipliers are good recognized to be probably the most common and major unit in every digital circuit used for performing valuable computations. The recent pattern deals with scaling up to nanometre scale. With the quickly developing trends in scaling as much as nanometer scale, the arithmetic circuits need to be implemented with low power, compact size, and less propagation delay.

Accordingly, arithmetic cells which consume low-power and provide high performance are of excellent importance. Thus, any adjustment made within the arithmetic unit would affect the association as a sum total. For designing the arithmetic circuits with low power and high speed [6], it requires the incorporation of strategies on the arithmetic level, arithmetic level, circuit level and system level. There are a number of low power design methods such as dynamic voltage scaling, frequency scaling and clock gating [2] but, there are very few design procedures that gives the required extensibility with low power consumption and low area.

The latest and innovative silicon technology process strategies have led to the fast progress of modern integrated chip (IC). The development has enabled commercial IC foundry and international semiconductor enterprise to supply compact, high performance, low power, and robust

microprocessor. The core of each and every microprocessor is the crucial processing unit (CPU) where the arithmetic logic unit (ALU) is placed and forms the main building block. ALU can participate in logical operation and basic arithmetic, particularly, addition, subtraction, multiplication, and division. Almost, the aforementioned arithmetic operation can also be summed up as follows: addition, negative addition, repeated addition, and repeated negative addition. In the digital system, it's crucial to have a full adder that is low in power consumption, of high speed, power efficient, and secure [3]. Compared to conventional MOSFET technology, the brand new FinFET technology can be applied in 1-bit full adder, to prolong silicon downscaling and increase the device efficiency and power efficiency of full adder.

As nanometer process technologies have advanced, chip density and operating frequency have increased, resulting power consumption in battery-operated devices a major factor. Even for nonportable devices, power consumption is important because of the increased packaging and cooling costs as well as potential reliability problems. Thus, the main design goal for VLSI (very-large-scale integration) designers is to meet performance requirements within a power budget. Therefore, power efficiency has assumed increased importance. This paper explores how multiplier based on FinFETs (fin-type field-effect transistors), an emerging transistor technology that is likely to supplement or supplant bulk CMOS (complementary metal-oxide-semiconductor) at 20-nm technology.

## 2. RELATED WORK

Aqilah binti Abdul Tahir, Huei Chaeng Chin, Cheng Siong Lim, and Michael Loong Peng Tan [1] presented an approach on Design and Performance Analysis of 1-Bit FinFET Full Adder Cells for Subthreshold Region at 16 nm Process Technology. In this work, the FinFET structure is

implemented in 1-bit full adder transistors to investigate its performance and energy efficiency in the sub threshold region for cell designs of Complementary MOS (CMOS), Complementary Pass-Transistor Logic (CPL), Transmission Gate (TG), and Hybrid CMOS (HCMOS).

Akshay Dhenge et al [2] evaluated and compared the performance and optimized area of ALU with Static CMOS technique and GDI technique in 250nm CMOS (1P5M-1Poly 5 Metal) process technology. Simulations are performed by using Tanner EDA 13.2 tools using model file 250nm CMOS technology.

Aminul Islam, Akram, Mohd and Hasan [3] presented 1-bit full adder cell in emerging technologies like FinFET and CNFET that operates in the moderate inversion region for energy efficiency, robustness and higher performance. Merlin Jararth et al [4] In this paper, design of two different array multipliers are presented, one by using Carry Select Adder using BEC logic for addition of partial product terms and another by introducing Carry Select Adder using D-latch logic in partial product lines.

G. Lakshmi and M. Devadas [5] demonstrated and evaluated comparative performance study of low power FINFET based various designs of full adder circuits. Full adder is a most important basic building block of digital circuits employing arithmetic operation. Simran kaur, Balwinder Singh and D. K. Jain described the implementation of various adders and multipliers. The design approach proposed in the article is based on the GDI (Gate Diffusion Input) technique.

### 3. PROPOSED SYSTEM

The simplified design blocks of 16 bit ALU is as shown below, here it performs two arithmetic operations and seven logical and shifting operations depending on the select lines. Same ALU architecture was implemented using MOSFET structures, as observed that, this structure has shorter channel effects, sub-threshold and dielectric leakage is more. So we going to design the same using FinFET structure using nano-scale technology and compare the leakage power with MOSFET structure.

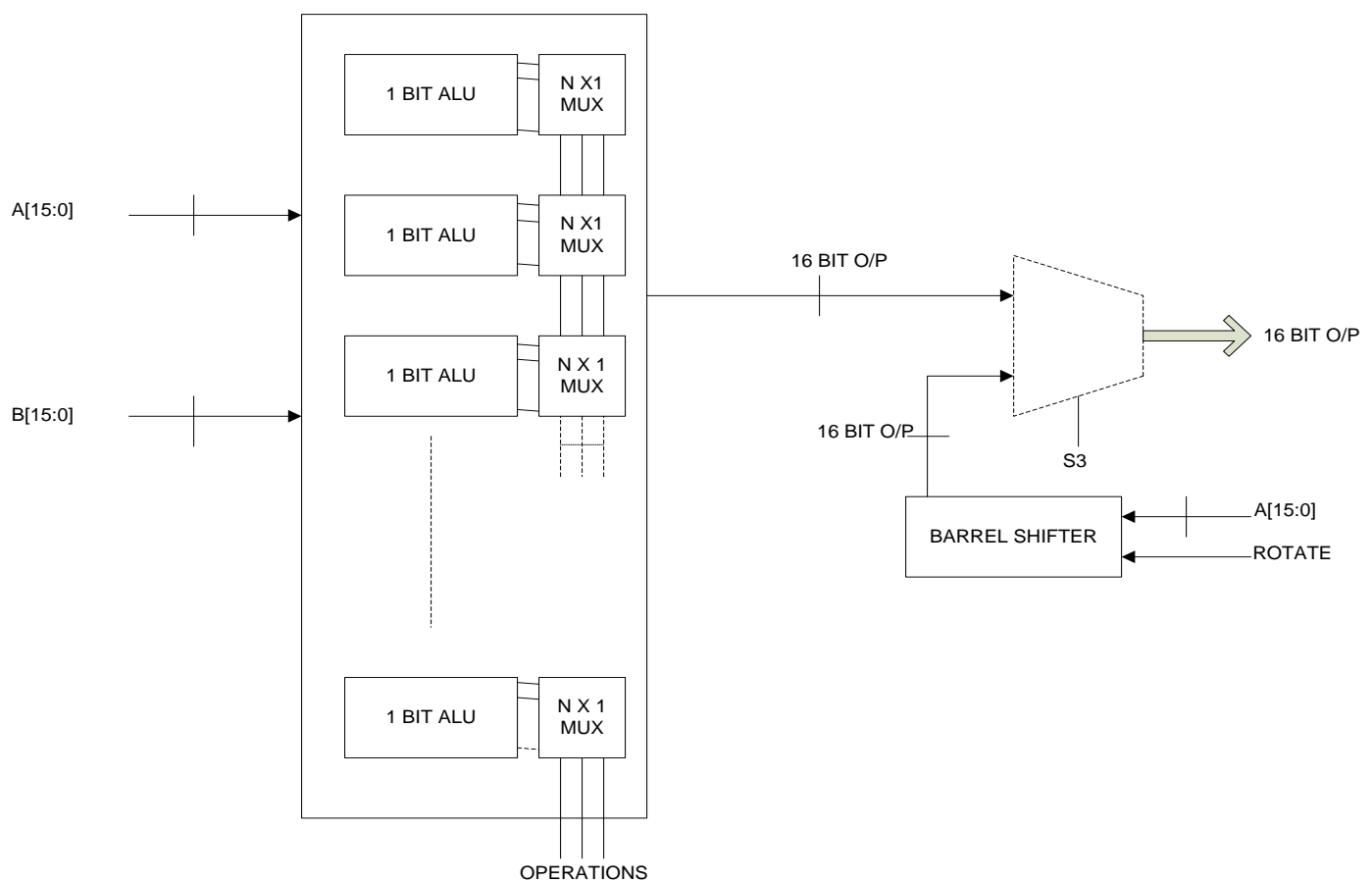
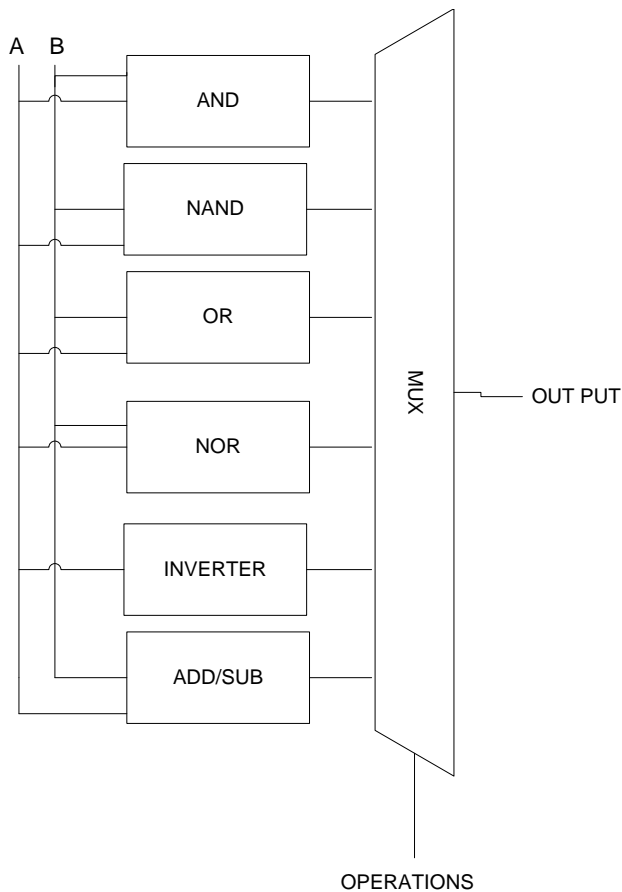


Fig -1: Proposed Architecture

Proposed parity generator has one 4:1 MUX, EXOR gate and inverter. This circuit generates even parity which can be used to notice any error if present in the received message. Because of this improvised design with respect to the traditional design, low power has been finished. Natural process has been used for the designing of multiplier which

consists of the proposed full adder and static CMOS type half of adder.



**Fig -2:** Circuit Diagram of 1 Bit ALU

Structure of ALU is depicted in the figure 5. The ALU performs the 4-bit operations on operands. The ALU contains eight 4X1 MUXs and to multiplex the outputs of these 4X1 MUXs, four 2X1 MUXs are used for the selection of the desired operation which is to be carried out. To select any one among the many eight operations, three selection traces have been used. Out of those eight operations, four are logical operations and the rest four are arithmetic operations. The MSB of select line ( ) chooses whether the operation to be performed is arithmetic type or logical type the rest 2-bits of select lines (  $S_0$  ) specifies the operation after choosing between arithmetic and logical.

#### 4. CONCLUSION

In this paper we presented an approach which uses combined segmentation and gradient vector flow to detect the boundary of an MR image. Initially we marked contour part and segment the input image using adaptive k-means clustering. GLDM features are extracted and edge of an image is obtained. Finally gradient vector flow is calculated to detect the final boundary part of an image.

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