DESIGN OF HIGH PERFORMANCE, LOW POWER MUX USING CIRCUIT LEVEL OPTIMIZATION IN CADENCE

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Abstract

This paper gives an insight into the Cadence design of a high performance, low power 8:1 MUX using 180nm technology. The paper is explained in two phases. First phase gives the simulation of a Xilinx tool generated non-optimized schematic. Second phase proposes a circuit level optimization technique using data correlation to realize the same circuit. Simulation results are compared

Keywords: *CMOS, Low Power, Power Reduction, Dynamic Power, Switching Activity, Data Correlation, Power Optimization, MUX*

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1. INTRODUCTION

High performance and low power are the two key words used by today's VLSI designers. Circuit complexity is increasing day by day. With the increasing demands for more functionality, power reduction has become a major concern faced by the designers. The various components of power dissipation are briefed below. Power optimization techniques at circuit level -data correlation, is made use of to arrive at an optimized 8:1 mux using Cadence 180nm technology.

2. COMPONENTS OF POWER DISSIPATION

The three main components of power dissipation in a CMOS VLSI circuit are listed below.

2.1 Dynamic Power Dissipation

This kind of power dissipation occurs when a [1]switching event is involved in the circuit. Switching results in charging and discharging of parasitic capacitances.

$P_{dynamic} = \alpha C_L V_{dd}^{\ 2} f$

Where α= switching activity factor, C_L=load capacitance, V_{dd}=supply voltage, f= clock freq.

2.2 Static Power Dissipation

The power dissipation that occurs when the transistors are not switching or when they are in the [2]quiescent condition. It occurs due to gate oxide leakage, subthreshold leakage and reverse biased PN junction leakage.

$P_{static} = I_{leakage} \cdot V_{dd}$

Where $I_{leakage}$ =leakage current, V_{dd} = supply voltage.

2.3 Short Circuit Power Dissipation

The existence of a direct current path between V_{dd} and ground results in short circuit power dissipation in a circuit.

$P_{short\ circuit} = I_{sc} \cdot V_{dd}$

Where I_{sc} = short circuit current, V_{dd} = supply voltage.

Hence the total power dissipation[3] in a CMOS VLSI circuit can be summed up as

$P_{total} = P_{dynamic} + P_{static} + P_{short\ circuit}$

Dynamic power dissipation contributes to a major share in the total power dissipation of any VLSI circuit. This paper aims at reducing the switching activity by data correlation and thereby reducing the dynamic power dissipation of the MUX.

3. PROCESS FLOW DIAGRAM

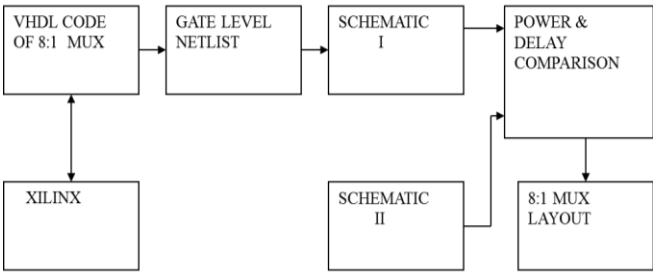

Fig -1: Process flow diagram

The above block diagram gives an idea about the flow of the paper. There are two paths as given in the diagram. First path results in a Xilinx tool generated non-optimized schematic I and the second path results in a circuit level optimized schematic II phase. Both the phases are explained below.

3.1 Non Optimized Schematic Phase I

Xilinx tool acts as a platform to generate the gate level netlist of the MUX from the VHDL source code. Transistor level schematic I of the generated gate level netlist is then simulated in Cadence. Simulation results are shown below.

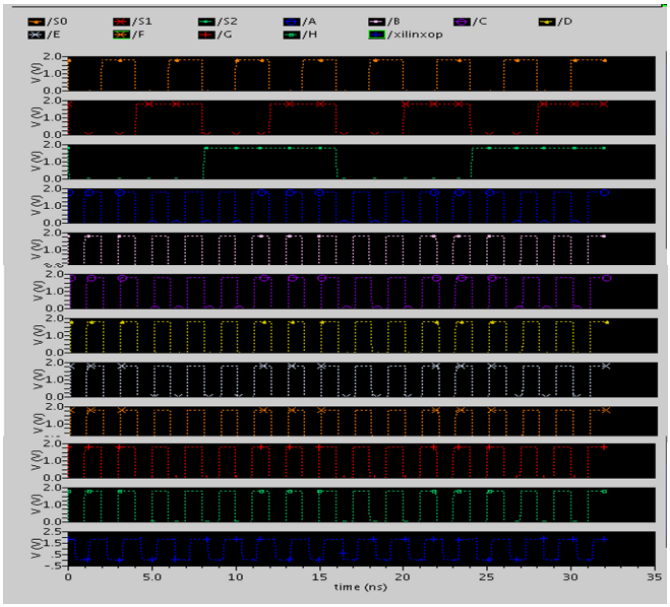

Fig -2: Simulation waveform of schematic I

3.2 Optimized Schematic Phase II

Optimization can be done at different levels of design. It can be at technology level, circuit level or algorithm level. The proposed technique in this paper performs a circuit level optimization, which aims at obtaining a high performance, low power design. Data correlation[4], which is an important attribute is made use of in this technique. Identical bits are grouped together to eliminate input redundancy, thereby reducing the switching activity [5]required to perform the functionality[6]

S2	S1	S0	I/P	O/P	
0	0	0	A	i0	i0i1 block
0	0	1	B	i1	
0	1	0	C	i2	i2i3 block
0	1	1	D	i3	
1	0	0	E	i4	i4i5 block
1	0	1	F	i5	
1	1	0	G	i6	i6i7 block
1	1	1	H	i7	

Fig -3: Optimization done in MUX truth table

The entire truth table of the 8:1 MUX is divided into four blocks, applying data correlation technique. S2 and S1 bits remaining same, only S0 is changing in each block. The block schematic of all the four blocks are given below.

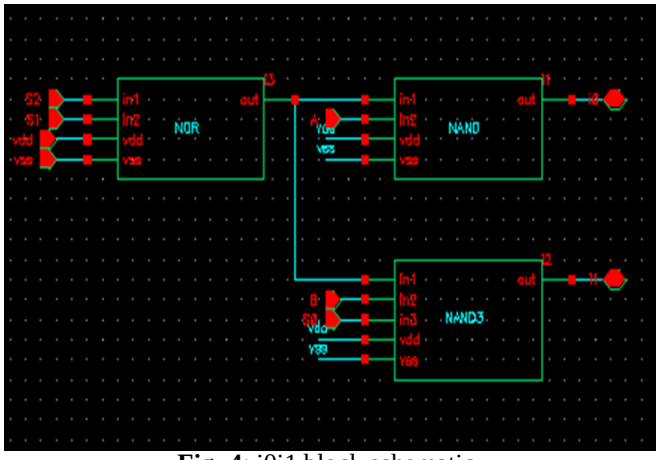

Fig -4: i0i1 block schematic

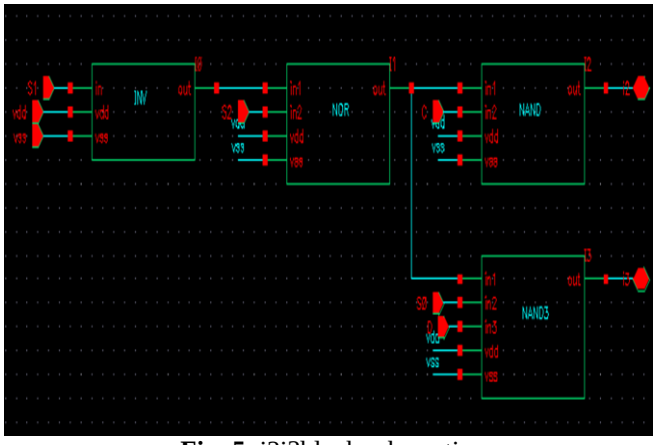

Fig -5: i2i3block schematic

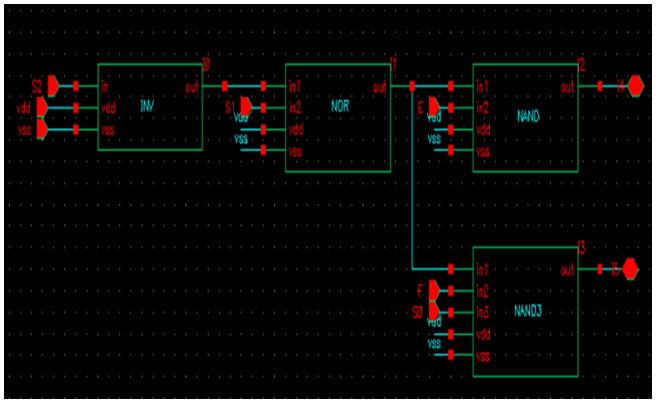

Fig -6: i4i5 block schematic

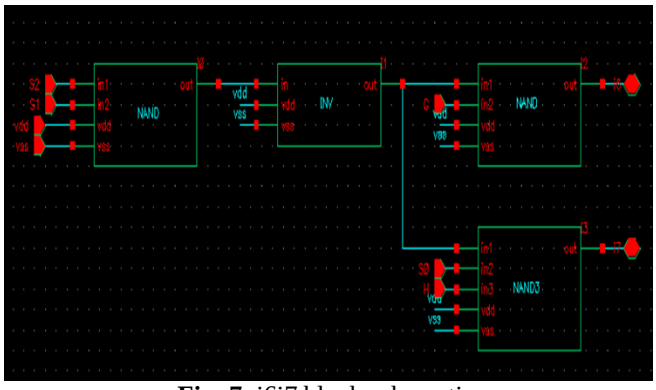

Fig -7: i6i7 block schematic

i1,i3,i5 and i7 outputs from the above four blocks results in a new block X0.i0,i2,i4 and i8 from the above explained blocks generates block X1.Block schematic of X0 and X1 are given below.

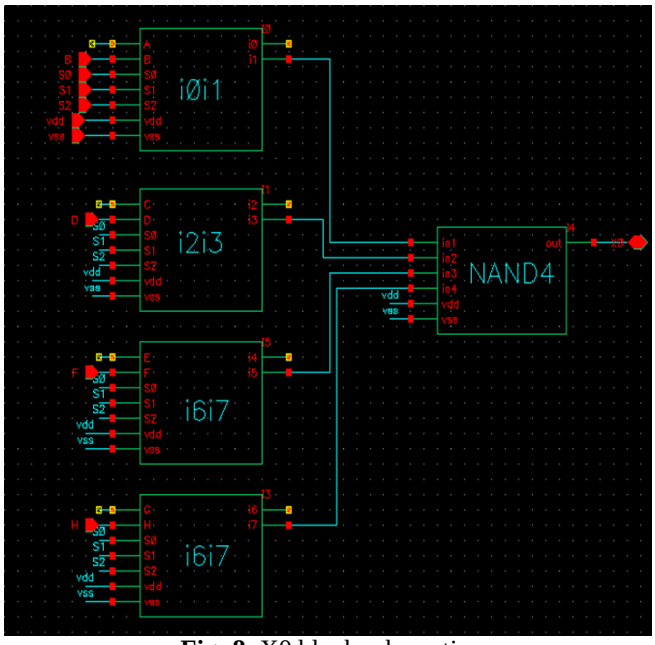

Fig -8: X0 block schematic

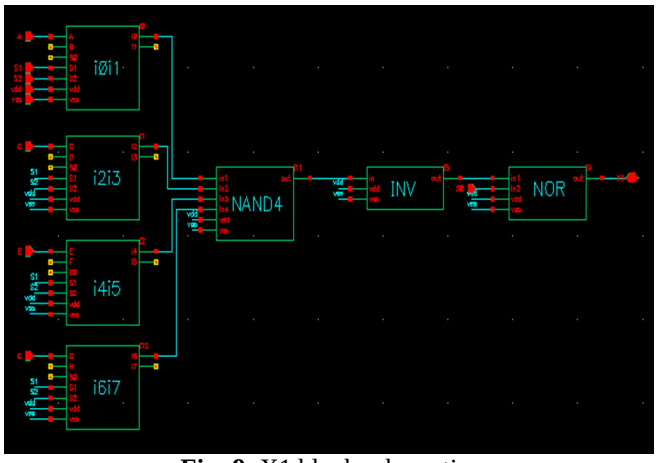

Fig -9: X1 block schematic

X0 and X1 blocks OR ed together results in the final optimized schematic II. Simulation waveform and schematics are included.

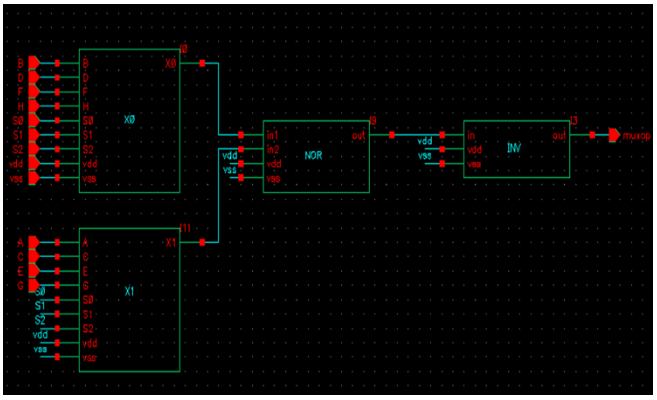

Fig -10: Optimized schematic II

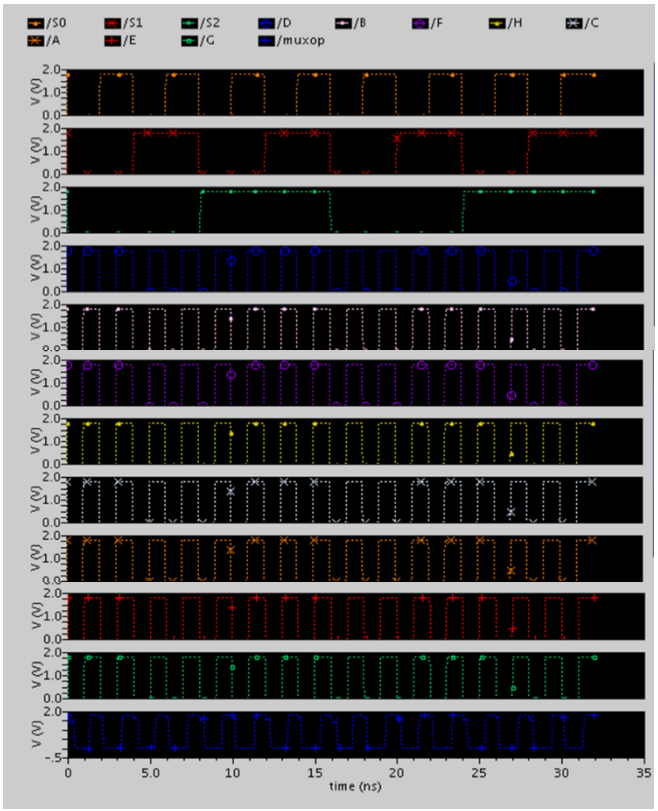

Fig -11: Simulation of optimized schematic II

4. RESULTS

4.1 Power REPORTS

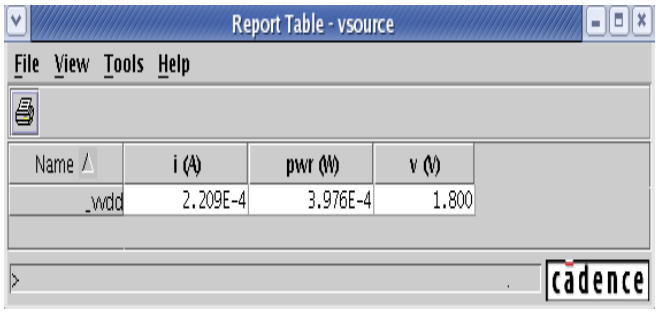

Fig -12: Schematic I power

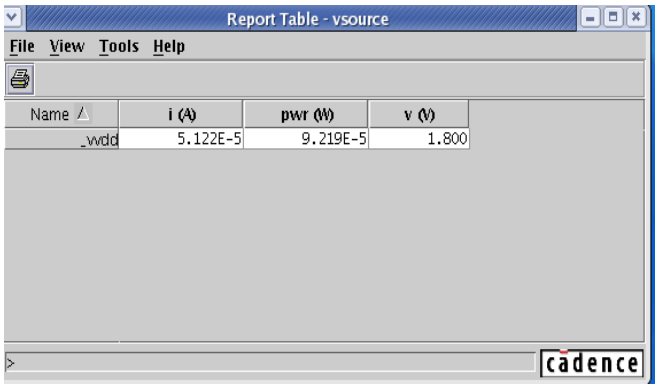

Fig -13: Schematic II power

From the power simulation results in Cadence,

$P_{schematic\ I}$-$P_{schematic\ II}$ = 305μW.

4.2 Delay Reports

τPLH(ns)	τPHL(ns)	τ = (τ PLH+ τ PHL) (ns)
0.275	0.378	0.653

Fig -14: Schematic I delay

τPLH(ns)	τPHL(ns)	τ = (τ PLH + τ PHL) (ns)
0.271	0.134	0.405

Fig -15: Schematic II delay

$Delay_{schematic\ I}$-$Delay_{schematic\ II}$ =248pS.

4.2 Transistor count

Schematic	Number of transistors
Non- optimized schematic	136
Optimized schematic	90

Fig -16: Transistor count comparison

4. CONCLUSION

The paper details the sources of power dissipation and the need for power reduction in CMOS VLSI circuit. The proposed circuit of a MUX using data correlation which is a circuit level optimization technique was successfully designed in Cadence. The optimized mux ,used as part of a huge VLSI circuit will bring down the total power dissipation by a large factor. Simulation results of the non-optimized and optimized circuits are compared.

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BIOGRAPHIES

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