DESIGN AND IMPLEMENTATION OF CARRY SKIP ADDER USING AOI AND OAI

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Abstract

Carry-skip adder (CSKA) (another name for it is called as carry-bypass adder) is an adder implementation which helps on the delay of a ripple-carry adder with less effort when it is compared with rest of other adders. The accepted or followed structure of the CSKA consist the different stages containing chain relation of full adders (FAs) (RCA block) and 2:1 multiplexer. The RCA blocks are connected one to one by 2:1 multiplexers, which we can place in further level structures. The configuration of the CSKA (i.e., the number of the FAs per stage) plays a very important role on speed in the adder. Over the period of time, several methods have been proposed to optimize the number of FAs used. Here we are presenting a method based on AND-OR-Invert (AOI) and OR-AND-Invert (OAI) compound gates logic is used to replace the MUX logic being used in traditional design. The presented methodology is about the comparison of power, energy and delay parameters with other existing adders.

Keywords: *Carry-Skip Adder, 2:1 Multiplexer, AND-OR-Invert, OR-AND-Invert (OAI).*

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1. INTRODUCTION

The adders are used as the basic blocks for arithmetic logic units (ALUs) [01]. Adder circuit is one of the vital building blocks in DSP processor also. Therefore minimizing their energy or power consumption and also decreasing their delay has a strong impact on performance of processors. For designers who design the processors for general purpose seems like a challenge.

To minimize the power consumption on digital circuits one of the efficient techniques is reducing the supply voltage of that circuit. The major leakage component in OFF devices is the sub threshold current. Through drain-induced barrier it is depended on voltage supply level [02]. The inspiration for building the circuits with characteristic of dynamic voltage and frequency scaling, is, dependence of power. To minimize energy consumption in these circuits, the voltage of the circuit may be altered by the system based on the requirement of workload [03].

Along with the supply voltage, there's always an option to select the adder among different adder structures/families to optimize their speed and power. Based on various delays, power used and space occupied many adder circuits are designed. carry skip adder (CSKA), ripple carry adder (RCA), parallel prefix adders (PPAs) and carry select adder (CSLA) are some of the example adder circuits. [01] and [04] have detailed description of each of these adders along with their respective characteristics.

Comparing all those adders, the best adder is CSKA because it requires less space and low power consumption [05]. But also space and power consumption is same as RCA, but delay path for CSKA is better and lesser when compared to RCA. Comparing to PPA, CSLA circuits the CSKA power delay product is lesser [06]. Due to CSKA is having less number of transistors will be having simplex layout and having less wiring length when compared to other like CSLA and PPA.

Mainly the paper is about concentrating on lower delay of CSKA (16 bit) structure by altering its implementation. The methodology used presently reduced delay when we having the lower power consumption and space occupied features of CSKA.

2. LITERATURE SURVEY

Milad Bhahadori et. al. have proposed a methodology of consuming the large amount of voltage with high speed and energy efficient CSKA. CSKA have high speed but not lower energy consumption when the power of proposed adder is compared to the existing adder. The concatenation and incrementation method is applied to enhance the CSKA speed rate. The proposed structure is to reduce the power consumption without effecting the speed.

B Ramkumar and Harish M Kitthur have mainly concentrated on the power and space occupied by CSLA[09]. Carry Select Adder (CSLA) is the fastest adders used for various operations like arithmetic operations. From the proposed method for CSLA , we can conclude that the proposed method decreases the ares and power consumed by CSLA. A simple gate level modification is used for a CSLA.

D. Markovic et. al. have implemented the low power adder which is operated in threshold region. The operation in the sub threshold region most often is as same as minimum energy operation. An energy modelling framework which extends over a weak, moderate and strong inversion region is developed. This work is from a need to make appropriate selection at the beginning of the design process [10].

Y Chen et. al. have mainly focused for no power and NBTI(negative bias temperature instability) occurrence in variable latency adder. Authors have designed a adder is known as variable latency and it design permit the adder to do the task by consuming low power compared with conventional one by keeping the identical throughput . NBIT effect is reduced by enhancing the variable latency adder.40% of energy is saved by using the concept of variable latency adder for carry select adder here the throughput is identical[11].

R. Zlatanovici et. al. in [12]. The authors have proposed the energy delay optimization methodology for digital circuits. Carry look ahead adder delay is minimized by using this approach below the energy constraint. Comparing the various adder design, the tree structure of carry look ahead adder and its logic style is analyzed in energy delay space.

S. Ghosh and K. Roy have designed the composed of different elements arithmetic units which is low power and high power are scaled at supply and adaptive clock stretching[13]. The main task for high speed ALU is meeting the performance and power requirement. Switching and power is reduced by supply voltage. it is based on arithmetic critical path and non critical path is operated by supply voltage at particular frequency. the delay is failure in critical path.

3. CONVENTIONAL CSKA

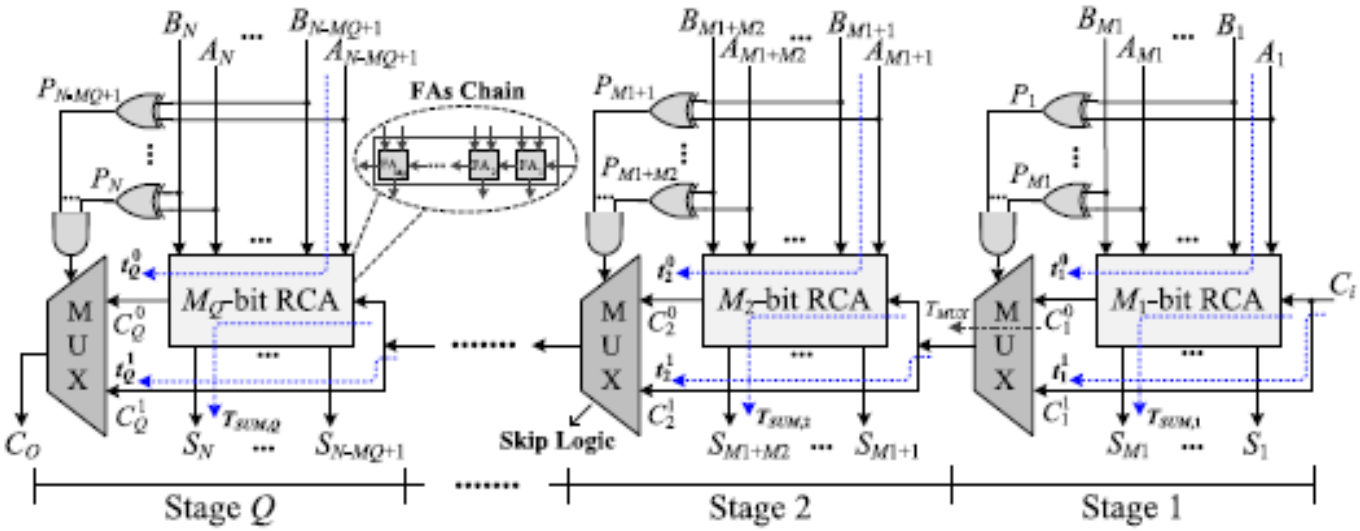

Figure 1: Conventional CSKA

Another name for carry-skip adder is carry-bypass adder. This carry skip adder, compared to other adders, improves on the delay of RCA with less effort. The conventional N-bit CSKA structure is as shown in Figure 1.

From the figure, we can see that, carry skip logic is included in each stages along with the sequence of FAs. Ripple carry adder consist of N full adders, the addition of A and B i.e two N-bit numbers. its worst propagation delay belongs to case in which each full adders in propagate mode and is related to

$$P_i = A_i \oplus B_i = 1 \quad (1)$$

for $i = 1 \ldots . N$

WhereP_i indicates the propagation signal propagation belonging to $A_i$andB_i. This implies that there is a linear relationship between N and the delay of the RCA. The carry output is same as carry input if the propagate mode consist of group of cascaded full adders. Such a situation is detected by the carry skip logic in CSKA, thus preparing the carry for the next stage here the operation of full adder is not required. As illustrated by the figure, the skip operation is executed using the multiplexer and the gates.

In CSKA N full adders is grouped in Q stages based on this description. Carry skip adder consists of RCA block with full adders and skip logic. In each stage, the inputs of the multiplexer are given as carry input for that stage and carry output of its RCA block. The selected signal of the multiplexer and propagation signals of current stage is a product term.

4. PROPOSED METHODOLOGY

In Figure 2 proposed architecture of a carry skip adder is shown. Here it uses the alternate AOI and OAI logic to implement the skip logic instead of 2:1 mux to reduce the propagation delay. The below same structure will run up to Q stages to implement the carry skip adder. The outputs of Ripple Carry Adders are passed through the incrimination blocks to give the sum output. In this proposed structure a carry is propagates through skip logic and the propagated carry becomes complemented. At even stages the skip logic output is complemented of the carry is generated.

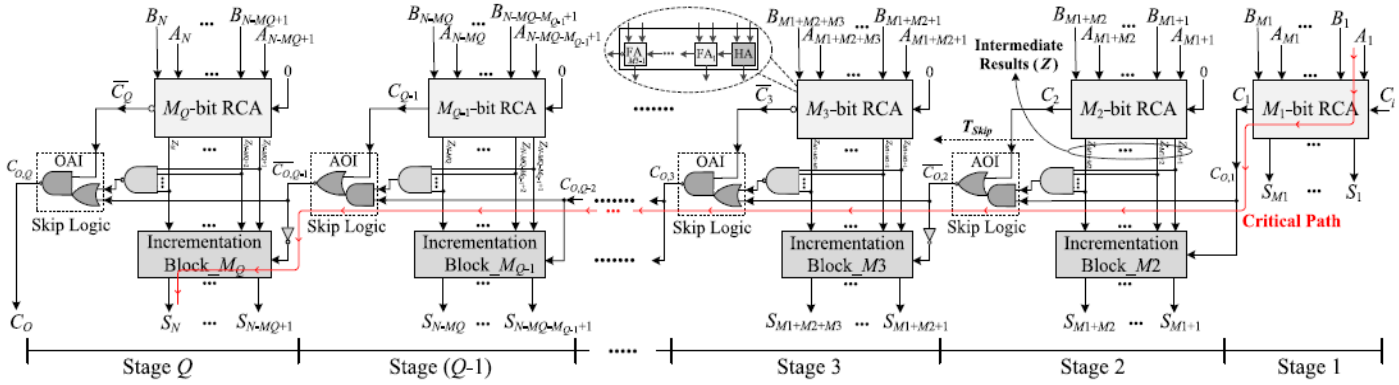

Figure 2: Proposed CSKA Structure

The incrementation block internal structure is shown in fig 3. This block consists of chain of half-adders (HAs). RCA block generates the intermediate output along with previous stage carry output are utilized by the incrementation block to process last summation of that stage.

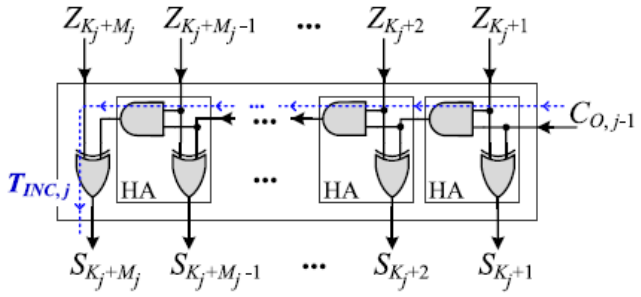

Figure 3: Incrementation Block (Internal structure)

5. EXPERIMENTAL RESULTS

This section presents the assessed path delay and area parameters. Alsothe schematic and waveform of the adder structure is presented.

The maximum combinational path delay obtained is 27.768ns. The device utilization details ARE as specified in Table 1.

Figure 4 displays the RTL schematic of CSKA. Figure 5 illustrates the waveform of ripple carry adder block of CSKA. The results presented show efficient decrease in the path delay

Table I: Device Utilization Summary

Logic Utilization	Used	Available	Utilization
Number of Slices	2	4656	0%
Number of input LUTs	4	9312	0%
Number of bonded IOBs	39	232	16%

In this paper, a static CMOS CSKA structure is presented. The presented system has relatively lower energy consumption and has improvised on the path delay, compared to the conventional one. The structure is altered to achieve enhancement in speed by making use of concatenation and incrementation procedures. Also, for the carry skip logics, AOI and OAI compound gates were employed. The presented scheme has achieved a better performance compared to the conventionl one.

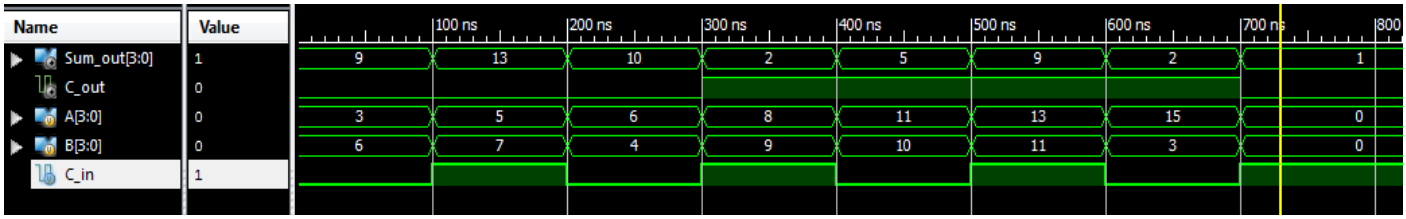

Figure 5: Ripple Carry Adder Waveform

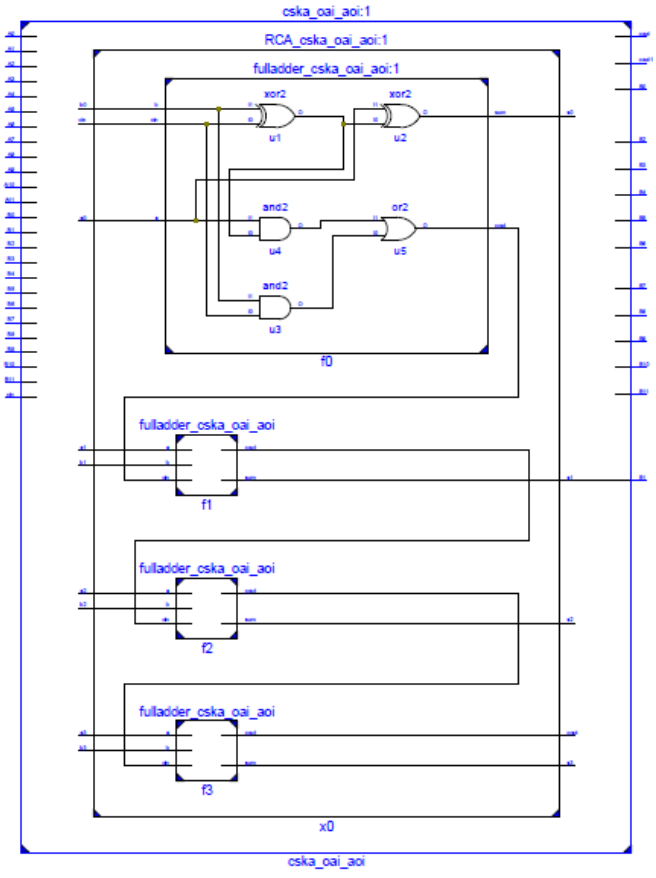

Figure 4: RTL Schematic

6. CONCLUSION

This paper is based on static CMOS CSKA structure . The presented system has relatively lower energy consumption and has improvised on the path delay, compared to the conventional one. The structure is altered to achieve enhancement in speed by making use of concatenation and incrementation procedures. Also, for the carry skip logics, compound gates of AOI and OAI were employed. The presented scheme has achieved a better performance compared to the conventional one.

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