DESIGN AND IMPLIMENTATION OF TEST PATTERN GENERATOR FOR DESIGN UNDER TEST

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Abstract

The patterns generated by LFSR for BIST as lack of correlation between the test vectors. Hence in order to improve the correlation of the test vector the patterns were generated using gray counter and decoder. In this paper we implement low power BIST for 4-bit multiplier. Main aspect of this is to implement low power BIST with increased fault coverage. This use the gray counter, decoder and accumulator as test pattern generator with changing the seed value for every 2 power m cycle, so for this purpose which use counter for monitoring the number of cycles. Hence the respective area optimization and power reduction can be achieved. Simulation outcome on multiplier circuit show a limiting of area and power than reconfigurable Johnson counter and LFSR. We implement the design using verilog HDL and Tool used for implementation is XILINX 13.2 and simulation is performed by using modelsim.

Key Words: *BIST, LFSR, Gray Counter, Decoder.*

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1. INTRODUCTION

Testing assumes to be a basic part within the field of production. The event of defect in VLSI circuit outcome in testing each chip. The defects that may occur in VLSI chips may cause design errors, material defect, malfunctioning of equipment. As the size of VLSI chips is compressing day by day the demand on power and area utilization is more hence testing is mandatory. Testing can be perform internally or externally. Outdoor testing be able to perform by utilizing Automatic Test Equipment (ATE). The test vectors are produced utilizing ATE in addition to be connected to Circuit under Test (CUT). Then the result is analyze by CAD Tool. The disadvantage of performing test utilizing ATE is longer era required for test and high cost of hardware. Consequently here is a movement from outdoor testing to the indoor testing. Indoor testing can be performing by Built in Self Test (BIST). While testing BIST reduce difficulties and complication that occurred during circuit testing. BIST can partition the device into number of levels and performs testing.

In digital systems power and energy utilization is superior in test form than in system form. At some phase in self test power utilization is more by a load since many switching node activity is caused by the random patterns. While during power saving mode a little modules are activated at the meantime. Power supply and casing of a circuit are cost concentrated part which has to be measured with peak power utilization and dissipation throughout BIST process. BIST might be reuse throughout the system era, intended for remote application. The life time of the BIST depends on life time of batteries.

Test pattern generates the fault coverage that was obtained from fault models is directly applied to the test pattern generator (TPG). For the point of pattern generation Exhaustive, Pseudo Exhaustive and Random pattern generation can be performed. In exhaustive test pattern contains 2N test vectors can be generated for every input N input combinational logic is obtained. Pseudo Random testing is most usable approach in BIST. In which the vector sequences are repeated every time hence it ensures that same set of fault is tested every time. Random test pattern is not feasible to generate all possible test vector sequences in large design because the space covered is so large to generate test vector sequence.

In conventional procedures the test vectors are formed by Linear Feedback Shift Register (LFSR) [1]. The drawback of creating test vectors is due to switch process involving the consecutive test vectors. These continuous changes will increase the power constraint. A study has been perform on internal and external testing by P.Girard in [2], A.Abu-issa and S.Quigley in [3], projected the method of interchanging bits to LFSRs. In the direction of develop the Correlation of the test vectors a reordering process is carried out.

2. EXISTING TECNIQUES

In this case linear feedback shift Register (LFSR) will acts as a pattern generator which generates a patterns. The generated patterns were sending to the scan chain. Module under Test (MUT) receives the test patterns from scan path. The scan paths serially or parallel send to the generated response from MUT to signature analysis (SA) that is captured by it. The test control units typically contain a bit counter and a pattern counter. The bit counter indicates that a system clock has been applied and sample is send into the scan path. Hence BIST completion status is indicated by pattern counters.

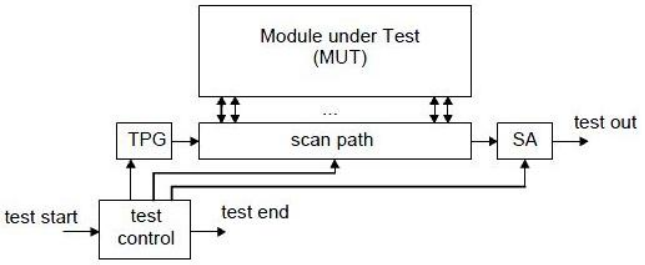

Fig 1: Test-per-scan scheme

In order to provide improvement in the respective field of test generation in BIST certain modification as to be done to overcome the fault coverage so that random and deterministic fault free patterns should be produced [4].

The aim of power decrease technique is to decrease peak power so that thermal and signal reliability issues can be reduced during while testing. Though in a few cases reduction in standard test power is favorable, because in some devices testing is done periodically hence power consumption is more. This technique will decrease the energy utilization which is main for battery power equipments.

3. PROPOSED SYSTEM

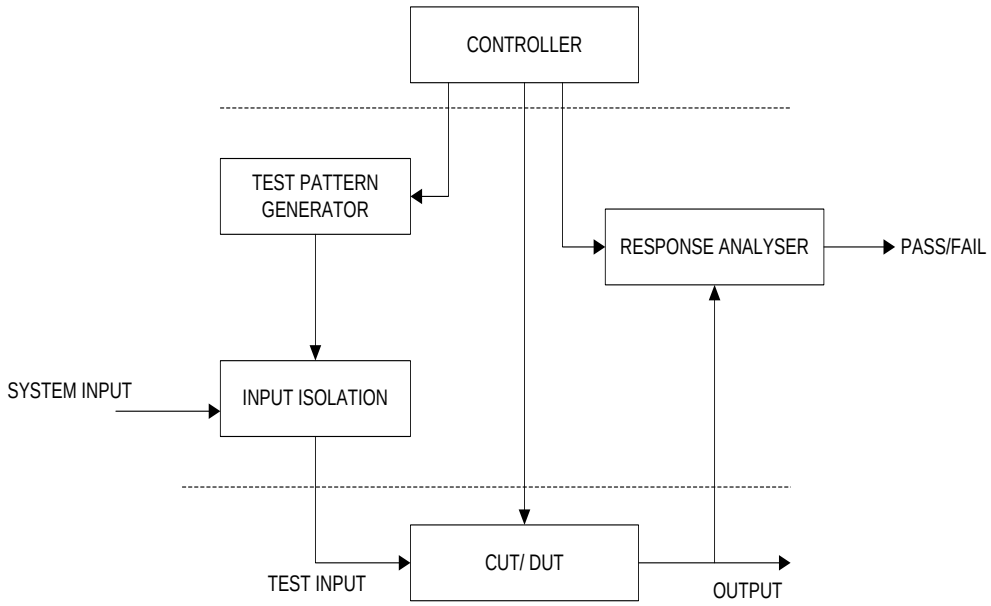

Fig 2: Block Diagram of the proposed System

The generic block diagram of a BIST is shown in Fig. 2. BIST solution consists of several blocks given below

Circuit under Test (CUT):
It is the part of the circuit tested in BIST mode. It can be combinational, sequential or a memory. During testing process on CUT an actual circuit signature is generated and then compare through the high-quality machine signature to decide whether CUT is defective.

Test pattern generator (TPG):
This is a one of the basic block of BIST circuit to be tested in which data analyzing and compressing as been done. The fault that was generated from various fault that occured is a direct function of test patterns resulted by the test pattern generator (TPG) and applied to the CUT. Here a Linear Feedback shift register usually generate patterns this patterns are generated in pseudo random fashion.

Test Controller:
It is the one of the main block in BIST system which controls the overall system for test execution. It provides signal to control all blocks. If control signal is 0 then BIST enters into test mode. If control signal is 1 then BIST enters into normal mode

Response Analyzer:
It acts as a comparator with stored responses. Compares the stored response with the tested output and shows whether the chip passes or fails the test.

3.1 Test Pattern Generator

TPG using test per clock:
Power and space enhancement is one of the fundamental perspectives that as to be fulfill the request of the consumers. In existing technique there is a there is a intricacy in power and space lessening. For this reason gray counter is used in Test pattern generator. To reduce the power and to avoid the unnecessary signal change at the key in clock pulse is active then the gray code result is connected to decoder circuit. At this point decoder result is connected to adder through Register B. At this point the Register A is utilized to store the process result in which set reset flip flop is utilized and been tested over multiplier. Then result is compared with the stored result.

The proposed system as benefit of limiting power and space utilized by the system. Then limits the intricacy of the system. By limiting power and space usage.

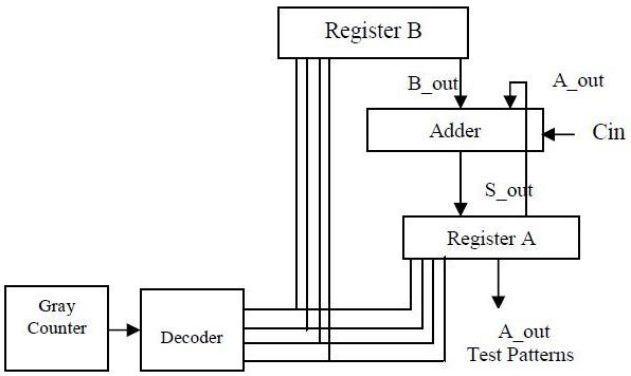

Fig. 3: TPG using gray counter

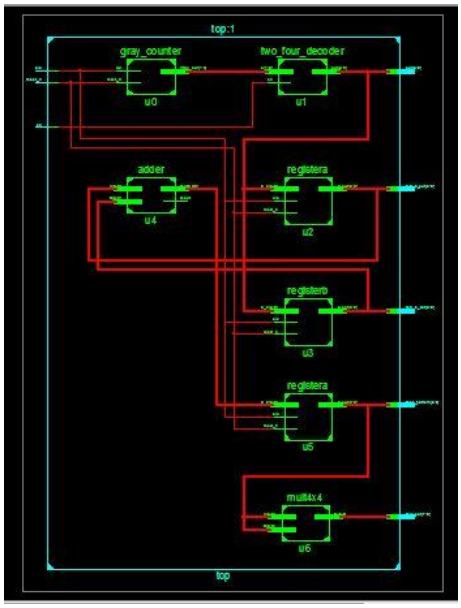

Fig. 4: RTL view of TPG using gray counter

4. RESULTS

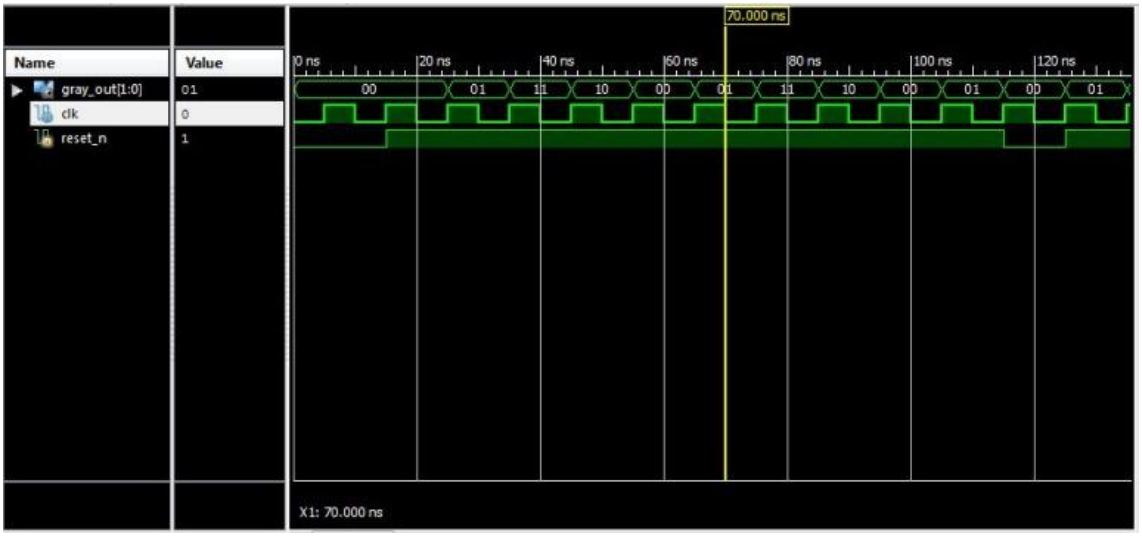

Fig. 5: Simulation Results of gray counter

Fig. 6: Simulation Results of decoder

Fig. 7: Simulation Results of Multiplier using gray counter TPG

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	8	1,536	1%	
Number of 4 input LUTs	8	1,536	1%	
Number of occupied Slices	7	768	1%	
Number of Slices containing only related logic	7	7	100%	
Number of Slices containing unrelated logic	0	7	0%	
Total Number of 4 input LUTs	9	1,536	1%	
Number used as logic	8			
Number used as a route-thru	1			
Number of bonded IOBs	27	124	21%	
IOB Flip Flops	2			
Number of BUFGMUXs	1	8	12%	
Average Fanout of Non-Clock Nets	2.63			

Fig. 8: Synthesis results of Proposed TPG

5. CONCLUSIONS

In this thesis a low power Test Pattern Generator has been incorporated in BIST developed for Vedic multiplier. The switching activities are reduced in the test pattern generation. Fault coverage is increased by the maximum number of clock cycles of the gray counter. The power consumption of different test pattern generation techniques has been found out and compared with the latest method. BIST is implemented for low power test pattern generator i.e. Vedic multiplier in the latest method. It is observed that the power consumption is reduced along with increased fault coverage when compared to other implementations.

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BIOGRAPHIES

Mr. Maseer Ahmed S N received BE Degree in Electronics and Communication Engineering from the Visvesvaraya Technological University. He is a student of M.Tech in Vlsi Design and Embedded System, VTU, Belgaum. Area of interest is in Vlsi design circuits and digital circuit design.

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