DESIGN OF A 4-BIT NON-VOLATILE SRAM USING MAGNETIC TUNNEL JUNCTION

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Abstract

In this paper, we propose a non-volatile SRAM, which presents simultaneously low power dissipation and high speed. This SRAM is based on MRAM (Magnetic RAM technology on standard CMOS. In this non-volatile SRAM design, we use Magnetic Tunnel Junctions (MTJ) as storage element. A 4-bit SRAM cell is designed and its read-write operations are described. Sense Amplifier is used in the read operation model. Two Write-Enable transistors and two inverters are used in the write operation model. The 4-bit SRAM cell has been implemented using Tanner tool. The operation of the SRAM cell is clearly understood from the output waveforms obtained after implementation. The structure and working of Magnetic Tunnel Junction is studied. The design of a Non-Volatile SRAM using Magnetic Tunnel Junction is proposed.

Keywords: *SRAM, MRAM, MTJ.*

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1. INTRODUCTION

Memory is one of the fundamental components of the modern computers used to retain digital data used for computing. Different types of memories such as SRAM, DRAM, Flash memory, MRAM etc., are used for data storage. Static Random Access Memory (SRAM) is fast, but a volatile memory. Dynamic Random Access Memory (DRAM) is cheap, but slow and volatile. Flash memory is a non-volatile memory, but slow and consumes high power. Magnetic Random Access Memory (MRAM) is also a non-volatile memory, it consumes less power and uses MTJ. Volatile memory is the one which loses the data when the memory is not powered, whereas non-volatile memory retains the stored data even after the power is off. A non-volatile SRAM, which presents simultaneously low power dissipation and high speed is proposed in this paper. This SRAM is based on MRAM (Magnetic RAM technology on standard CMOS [1]. We use MTJ to make SRAM non-volatile [2]. In our proposed model, the output of the SRAM is connected to the Sense Amplifier and the output of the Sense Amplifier is connected to the MTJ [3].

2. STUDY OF SRAM

Static Random Access Memory (SRAM) is a semi-conductor memory. There is no need to periodically refresh this memory because it uses Bi-stable Latching Circuitry to store each bit. SRAM is a volatile memory, that is, data is lost when the memory is not powered. Basically, there are two types of SRAMs namely, the 4T SRAM and the 6T SRAM.

2.1. 6T SRAM

The structure of a 6T SRAM cell consists of four NMOS transistors and two PMOS transistors as shown in Fig. 2. The transistors M5 and M6 are known as pass transistors and they are controlled by the word line (WL) when data is given through the bit lines BL and BL. Each bit in an SRAM is stored on the four transistors M1, M2, M3 and M4 that form two cross-coupled inverters [5].

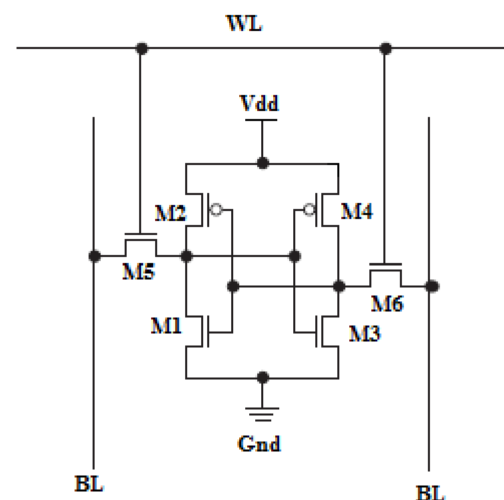

Fig -1: Structure of a 6T SRAM cell.

2.2 .Operations in SRAM

2.2.1. Procedure to write logic ‘0’ and logic ‘1’

The write cycle begins by applying the value to be written to the bit lines. To write logic ‘0’, ‘0’ has to be applied to BL and ‘1’ has to be applied to BL. WL is then asserted and the

value is to be stored is latched in. Bi-stable Latching Circuitry is used to store each bit. When BL is given logic '0', it will be fed to 'Y'. Now, the PMOS will be closed and it pulls the V_{dd} to give the output as logic'1'. The procedure for writing logic '0' is shown in Fig. 2. To write logic '1', '1' has to be applied to BL and '0' has to be applied to BL. WL is then asserted and the value is stored in using the Bi-stable latching circuitry. When BL is given logic '1', it is then fed to 'X'. Now, the NMOS will conduct and gives the output as logic '0'. The procedure for writing logic '1' is shown in Fig. 3.

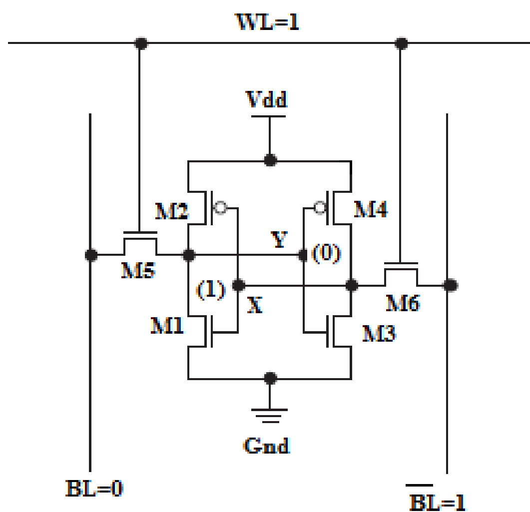

Fig -2: Procedure for writing logic '0'

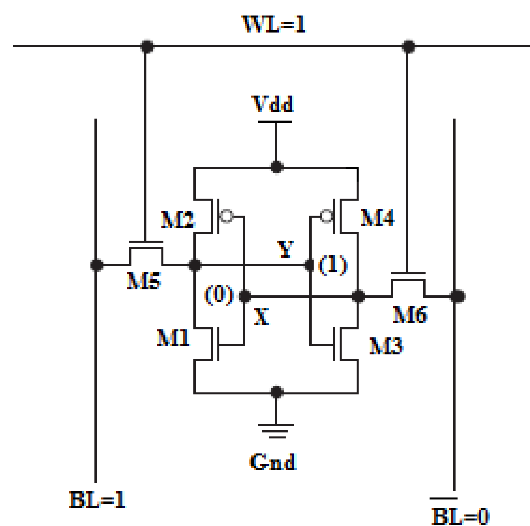

Fig -3: Procedure for writing logic '1'

2.2.2. Procedure to read logic '0' and logic '1'

The read cycle is started by precharging both the bit lines to a logical '1', then asserting the WL, enabling both the access transistors M5 and M6. The values stored in X and Y are transferred to the bit lines by leaving BL at its precharged value and discharging BL through M1 and M5 to a logical '0' and BL is pulled by M4 and M6 towards V_{dd}, a logical '1'. The procedure for reading logic '0' is shown in Fig. 4. To read logic '1', BL and BL are precharged to a logical '1'. WL is asserted and the values at 'X' and 'Y' are transferred to the bit lines by leaving BL at its precharged value and discharging BL through M3 and M6 to a logical '0' and BL is pulled by M2 and M5 towards V_{dd}, a logical '1'. The procedure for reading logic '1' is shown in Fig. 5.

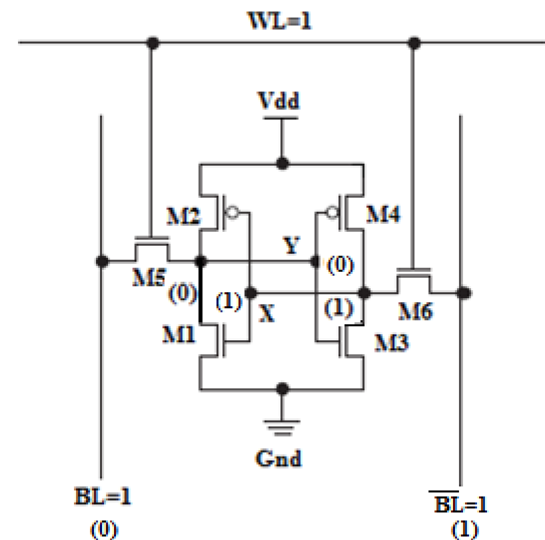

Fig -4: Procedure for reading logic '0'

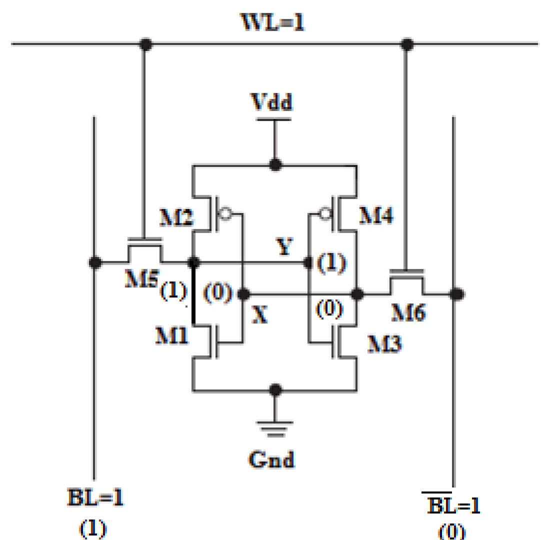

Fig -5: Procedure for reading logic '1'

2.3. Sense Amplifier

A Sense Amplifier is an essential circuit in designing memory chips. Due to large arrays of SRAM cells, the resulting signal, during Read operation, will have a much lower voltage swing. To compensate that swing, a Sense Amplifier is used to amplify voltage coming off the Bit Lines. The voltage coming out of the Sense Amplifier has a fully swing (0 - 2.5V) voltage. Sense amplifier also provides faster sensing which in turn reduces the delay time and power dissipation. Fig. 7 shows the structure of a Differential Sense Amplifier which consists of two PMOS transistors M3 and M4 and two NMOS transistors M1 and

M2. The gates of M3 and M4 are connected to the V_{GS}. The outputs of the SRAM cell are fed into the gates of M1 and M2 as X and Y respectively. The Sense Enable input (SE) is given a logical '0' or a logical '1'. When SE='1', the Sense Amplifier senses the data to be read and gives the output. When SE='0', it will be in the standby mode.

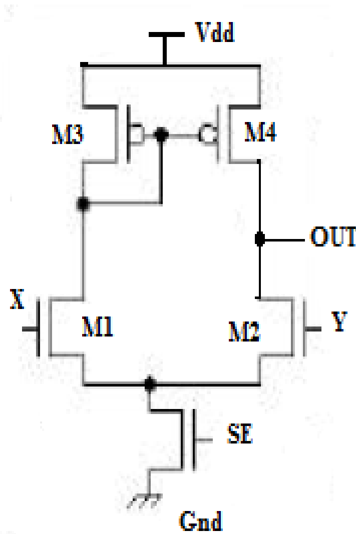

Fig -6: Sense Amplifier

X and Y – Outputs of SRAM cell fed as input to Sense Amplifier circuit.
OUT – Output of Sense Amplifier circuit.
SE=1, sense mode; SE=0, standby mode.

3. STUDY OF MTJ

3.1. MRAM

Magnetic Random Access Memory (MRAM) is a semi-conductor memory. It is a non-volatile memory which can store the data even when the power is off. It is slower than SRAM in its operation, but cheaper than SRAM. It need not be periodically refreshed. It is developed using Magnetic Tunnel Junction (MTJ).

3.2. MRAM Technologies

Three MRAM Technologies are currently being developed
– Hybrid Ferro-magnet Semiconductor Structures
– Magnetic Tunnel Junctions
– All-Metal Spin Transistors & Spin Valves

Writing data to a cell is similar for all 3 technologies. Reading a cell's data reads the direction of magnetization of a ferromagnetic element, but the method varies for each technology. The two possible magnetization states of a Ferro-magnetic element are described by a Hysteresis Loop as shown in Fig. 7.

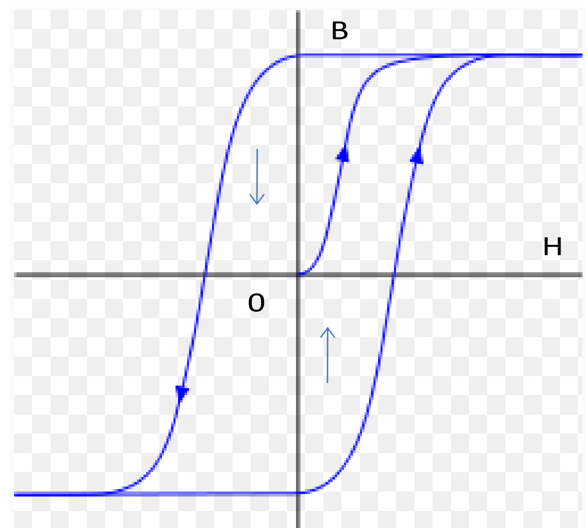

Fig -7: Hysteresis Loop

3.3. Magnetic Tunnel Junction

MTJ is the elementary storage device in MRAM. Ferro-magnet is the type of material used to create a MTJ to develop MRAM. Two ferro-magnetic films are separated by a dielectric tunnel barrier. Resistance between films depends on their magnetic states. The MTJ behaves as a resistor with two resistance characteristics such as Low Resistance corresponding to the Parallel Fields and High Resistance corresponding to the Anti-parallel Fields depending on the direction of magnetization in the two ferro-magnetic layers as shown in Fig. 8. The two resistance values represent different bit of information [4]

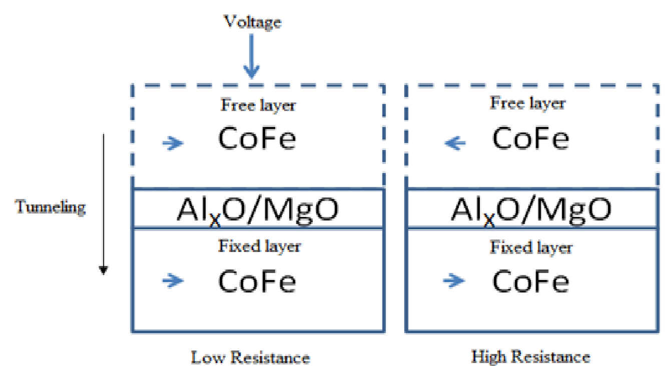

Fig -8: Low Resistance and High Resistance

3.4. Tunnel magneto Resistance

The Tunnel magneto Resistance (TMR) is a magneto-resistive effect that occurs in MTJs. It is the ratio between the anti-parallel resistance and the parallel resistance. The TMR value is 70% in an AlxO barrier MTJ and 230% in an MgO barrier MTJ. This improvement of TMR helps to read the information in MTJs more easily when the low and high resistance represent different bit of information [5]. TMR changes with the applied magnetic field.

TMR is defined in Equ. (3.1)

$$TMR= (R_{AP} – R_P) / R_P \qquad (3.1)$$

4. SIMULATION RESULTS

Simulation of the 4-bit SRAM read-write circuit was done using Tanner tool and the Circuit and the Output waveforms are shown below.

4.1. 4-bit SRAM read-write structure

In Fig.9, the Write Enable input, Word Line and the Sense Enable input are given as common, whereas the Write Data input is given separately for each cell and the Outputs are also taken out separately. WE – Write Enable; WD – Write Data; SE – Sense Enable; WL – Word Line; OUT – Output.

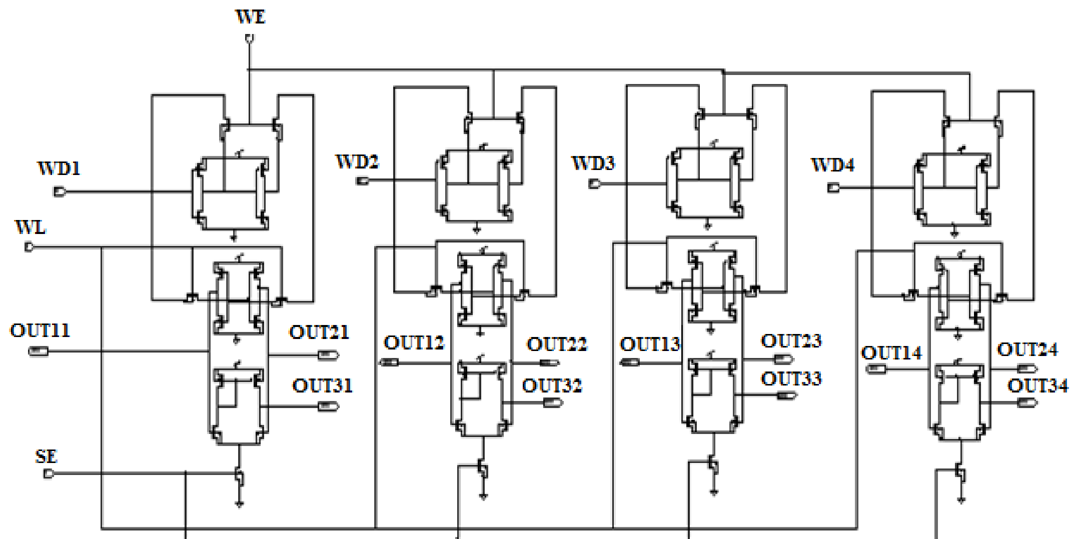

Fig -9: 4-bit SRAM read- write structure

4.2. Output Waveform for 4-bit SRAM read-write structure

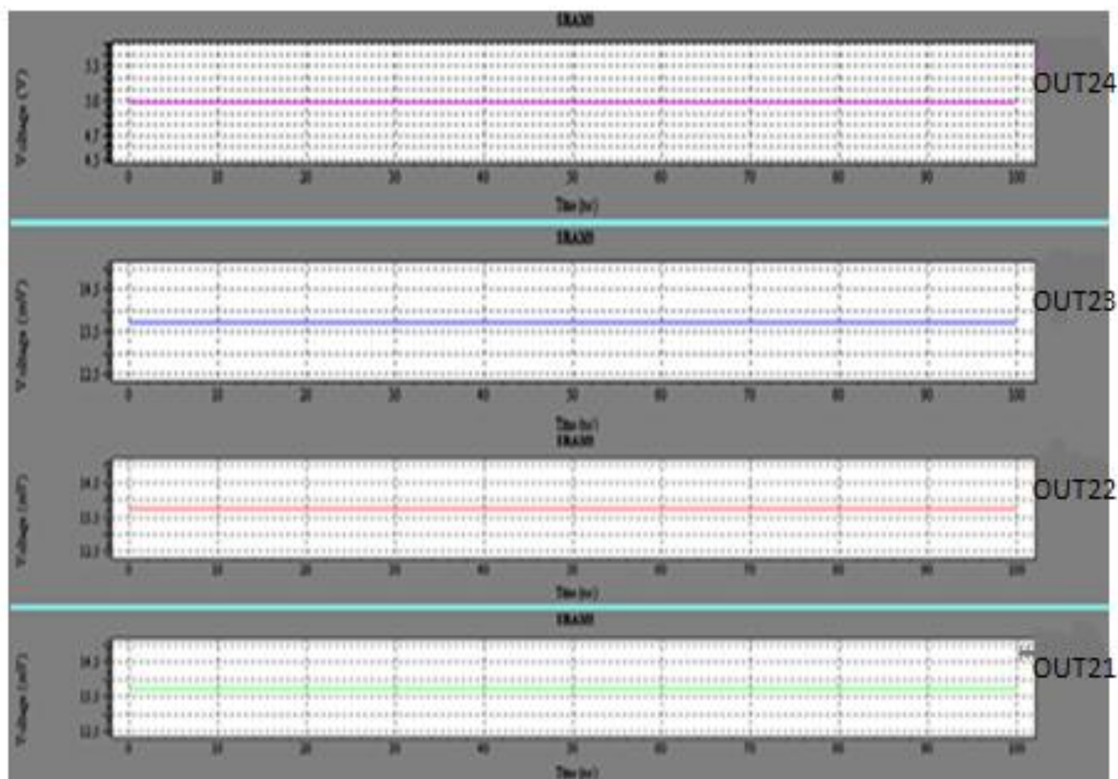

Fig -10: Output Waveform for 4-bit SRAM read-write structure

5. PROPOSED NON-VOLATILE SRAM MODEL

The Non-Volatile SRAM is designed using MTJ by connecting the MTJ to the SRAM serially [6]. The output of the SRAM cell is normally connected to its sense amplifier. The output of this sense amplifier has to be fed into the MTJ and the output has to be taken [7]. The MTJ is theoretically designed by calculating its resistance values. There are two resistances in MTJ namely high resistance and low resistance [8]. Depending on the direction of magnetization of the ferromagnetic layers, that is, same direction constitutes parallel resistance or low resistance and opposite direction constitutes anti-parallel resistance or high resistance. Both the resistance values represent different bit of information. High resistance represents logic '0' and low resistance represents logic '1'.

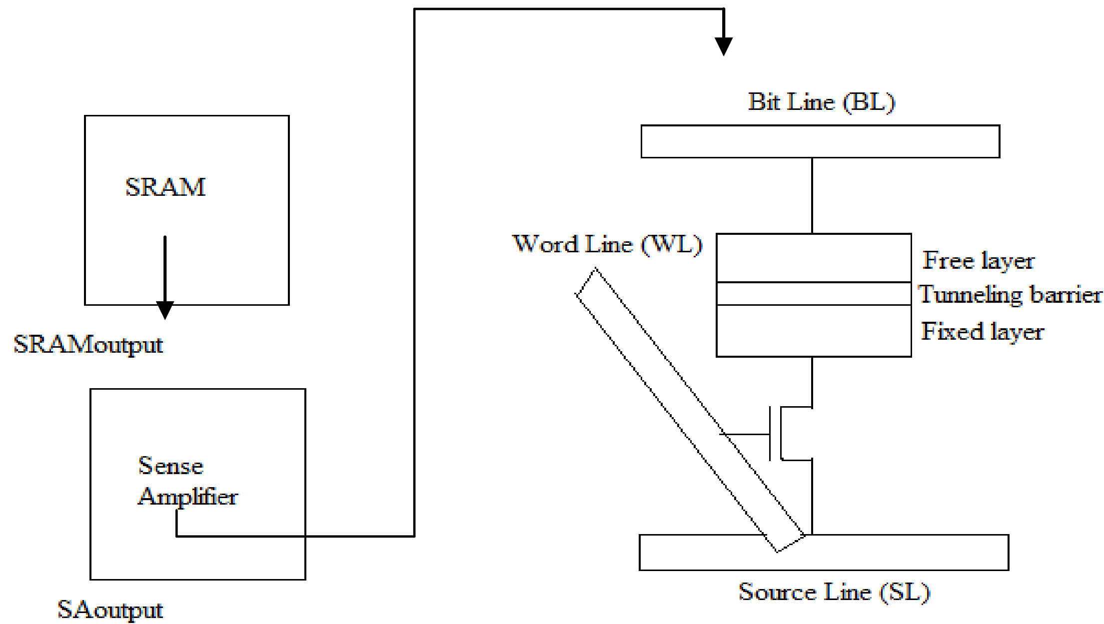

Fig -11: Proposed Non-Volatile SRAM model

6. CONCLUSION

We propose this model of non-volatile SRAM for low power dissipation and high speed. The circuits for illustrating the read and write operations in a single SRAM cell and a 4-bit SRAM cell were designed using Tanner tool and the simulation results and the output waveforms were obtained and the structure and the operation of MTJ were studied.

7. ACKNOWLEDGEMENT

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BIOGRAPHIES

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