ANALYTICAL STUDY OF STRAINED SOI MOSFET

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Abstract

In this paper, a comparison between Silicon on Insulator (SOI) and Strained Silicon on Insulator (SSOI) has been done with different technology nodes (25 nm& 32nm) .The Physical parameters for the N -channel MOSFET have been specified according to the International Technology Roadmap for Semiconductors (ITRS)[1].Simulations are done in ATLAS package of SIVACO tool. Further in this work, study of SOI Device incorporating the concept of strained channel are carried out. Simulation of different values of Drive Current (I_{on}), Leakage Current (I_{off}) and Transfer Characteristics (Id/Vg) are analyzed. All the structures are simulated for Uniaxial Strained SOI MOSFET as well as Biaxial Strained SOI MOSFET in nanometer. It has been found that Strained SOI structure shows larger Drive Current as compare to SOI structures. Hence due to its larger Drive Current it seems to better drive capability as compare to other MOS candidates. In Strained channel MOS devices electrons can move 70% faster allowing Strained Silicon transistors to switch 35% faster.

Keywords: *Strained Silicon, Uniaxially & Biaxially Strained-Silicon MOSFET.*

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1. INTRODUCTION

Silicon-on-insulator (SOI) has been the forerunner of the CMOS technology in the last decade offering superior CMOS devices with higher speed, higher density, excellent radiation hardness and reduced second order effects for submicron [12] VLSI applications. Figure 1 shows the cross-section of the bulk and SOI MOS devices[13].A lot of effort has been made to overcome the scaling problem, which seems to obey Moore's Law. Since scaling has reached its limit, Strained silicon is the latest alternative to achieve the same result as scaling down, without the need to alter the size of the electronic devices.

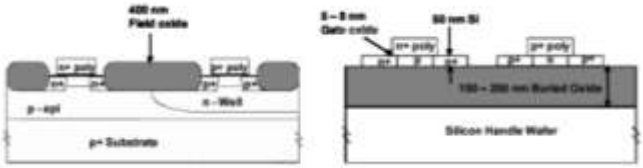

Fig.-1: Cross-sectional view of the bulk-Si (left) and SOI (right) CMOS devices [2].

MOSFET with a high mobility channel is an attractive device structure. From this viewpoint, a strained-Si channel is promising for CMOS application, because of the high mobility. Strained silicon is a layer of silicon in which the silicon atoms are stretched beyond their normal interatomic distance. This can be accomplished by putting the layer of silicon over a substrate of silicon-germanium(SiGe).As the atoms in the silicon layer align with the atoms of the underlying silicon germanium layer (which are arranged a little farther apart, with respect to those of a bulk silicon crystal), the links between the silicon atoms become stretched - thereby leading to strained silicon. Moving these silicon atoms farther apart reduces the atomic forces that interfere with the movement of electrons through the transistors and thus better mobility, resulting in better chip performance and lower energy consumption. These electrons can move 70% faster allowing strained silicon transistors to switch 35% faster. The mobility enhancement obtained by applying appropriate strain provides higher carrier velocity in MOS channels. Under a fixed supply voltage and gate oxide thickness, this will result in a higher drive current.Fig.2 shows structure ofStrained-SOI MOSFETs[14]. The advantage of strained silicon lies in its electrical properties. A general term for Si1-xGex is SiGe, which is widely used in the semiconductor technology to be matched with silicon and produced strained silicon. Since the fundamental scaling has its own limitation caused by the short channel effect, SiGe extends the chance of improving the performance of MOSFETs. The 4.2% lattice mismatch between Si and SiGe layer is used to create strained layer to enhance the carrier transport in the MOSFET's channel[5].Several advantages have been found by introducing strained silicon in MOSFET-

- Carrier Mobility Enhancement[10][11].
- Lower the resistance and power consumption.
- New gate stack material needs delay[8]

The advantages of strained silicon is indeed should not be taken lightly, since it is the new hope of improving MOSFETs for better performance.

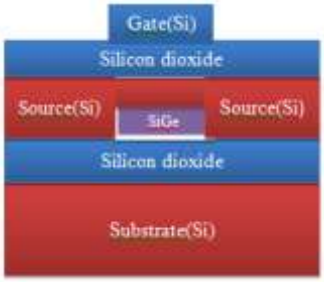

Fig-2: Structure of Strained SOI

1.1 Straining the Si-Channel

Strain in silicon channel can be introduced either during processing known as process induced strain or from the bottom by growing silicon on top of a crystalline template typically silicon with20% or more germanium content, known as substrate induced strain. Figure 3 shows the Strained silicon after being matched with Silicon Germanium.

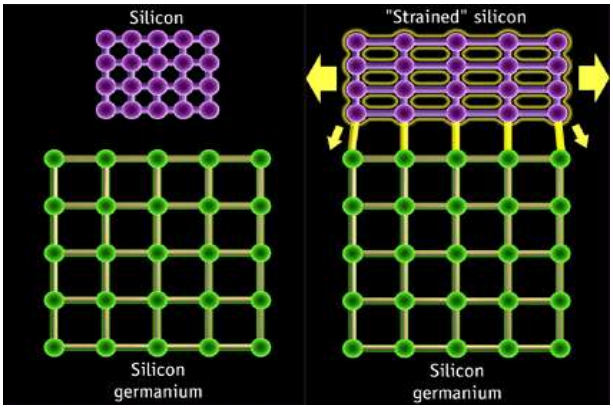

Fig 3-: (Left) Pure silicon and Silicon Germanium (Right) Strained silicon after being matched with Silicon Germanium[9].

1.2 Methods to Implement the Strain

1.2.1 Uniaxial Strained Silicon MOSFET (Process-Induced Strain)

Uniaxial local strain is realized locally,in the transistor channel,either by using srtained compressive or tensile contact etch stop layers for pMOS and nMOS devices,respectively,or by the integration of silicon-germanium(SiGe)in the source and drain regions of the pMOS transistors.

Uniaxial stress could provide a low channel direction in plane conductivity mass, large out-of-plane in confinement mass, and high in-plane density of states (DOS) to the ground hole subband[6].

1.2.2 Biaxial Strained Silicon MOSFET (Substrate-Induced Strain)

Biaxial strain in the lattice structure of a crystalline Silicon is induced when an epitaxial of a thin Silicon film is grown on top of a relaxed Silicon Germanium (SiGe) substrate[7]. Strained silicon is introduced at the region between the source and the drain region, and a relaxed SiGe layer is placed at the top of the bulk, right under the strained silicon layer. The bottom part of the device will be the silicon substrate layer. Bulk silicon and bulk germanium have different lattice constants, 5.43A and 5.65A respectively. The lattice constant in the alloy Si-Ge is between that of Si and Ge and varies with Ge concentration. If a thin silicon film is grown on top of Si-Ge, up to a critical thickness, Si lattice follows the lattice of underlying substrate and gets stretched (or strained) in the plane of the interface. Figure 4 shows Uniaxial & Biaxial Strained SOI.

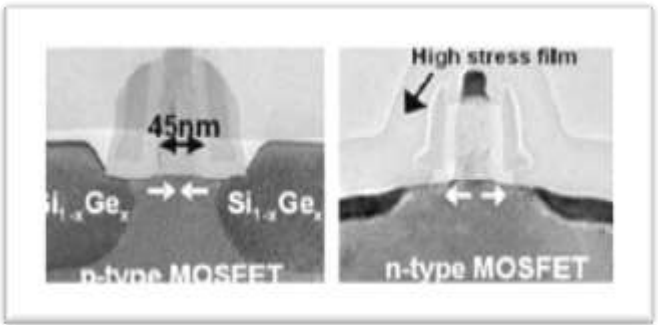

Fig.4-: Uniaxial and Biaxial Stained SOI[3]

1.3 Uniaxialversus Biaxial

Unlike, process induced strain which is uniaxial, biaxial tensile strain enhances both electron and hole mobility's.This is a major reason for commercialization of wafers based on strained silicon on top of Si-Ge layer despite process complexities and huge cost. This is opposed to process induced strain where both electron and hole mobility's respond oppositely to uniaxial tensile strain[4].

2. RESULTS AND DISCUSSIONS

The physical parameters of N-Channel SOI-MOSFET at 32nm and 25 nm in Table 1.The designs are made in the ATLAS framework of SILVACO TCAD tool .Device simulation is an important tool as it provides us quick feedback.

Table-1: Physical Parameters of SOI-MOSFET at 32nm

PHYSICAL PARAMETER	VALUE
Technology node	32nm
Gate oxide thickness	2nm
T_{si}thickness	5nm
Source/Drain doping	9.5e16cm-3
Box thickness	50nm
Channel doping	3.5e11cm-3
Substrate doping	1e10cm-3
Substrate thickness	70nm

Figure 5, Figure 6(a) & Figure 6(b) shows simple Silicon on Insulator(SOI) simulation,Silicon on Insulator(SOI) at 32nm and SOI at 25nm respectively on Silvaco tool .

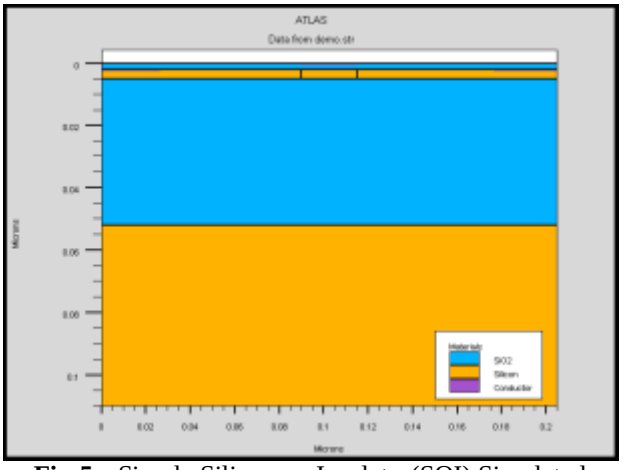

Fig-5-: Simple Silicon on Insulator(SOI) Simulated Structure

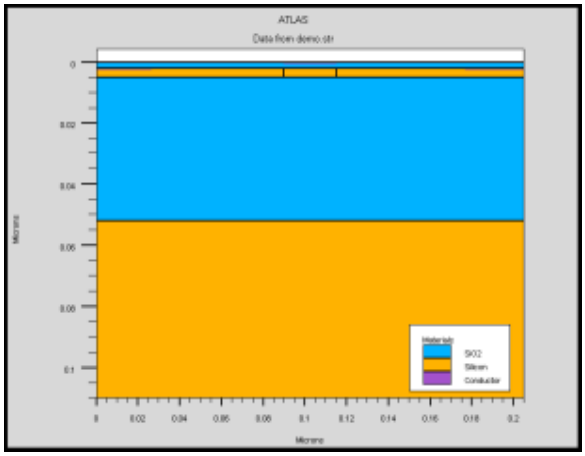

Fig-6(a):-Silicon on Insulator Simulated Structure(SOI) at 32nm

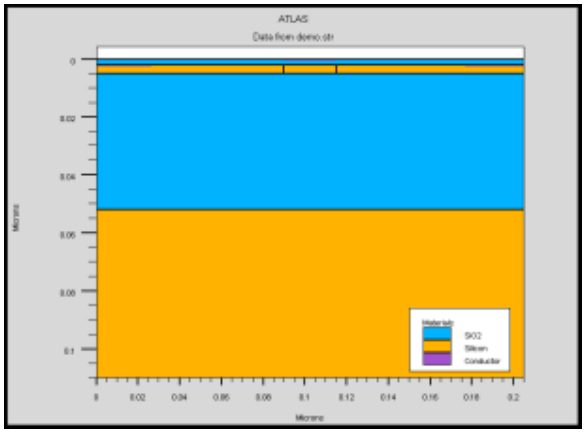

Fig-6(b):-Silicon on Insulator(SOI) simulated structure at 25nm

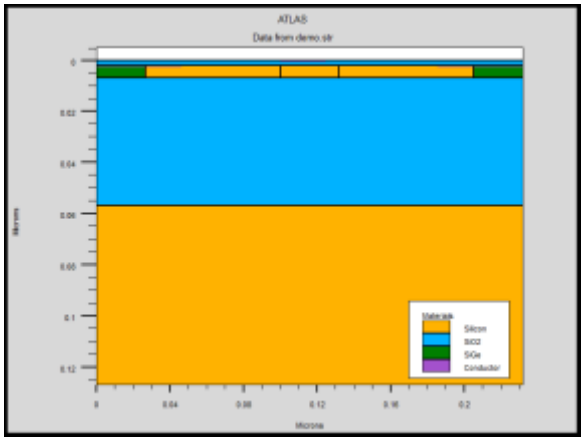

Fig-7(a):-UniaxialStrained Silicon on Insulator (SSOI) structure at 32nm

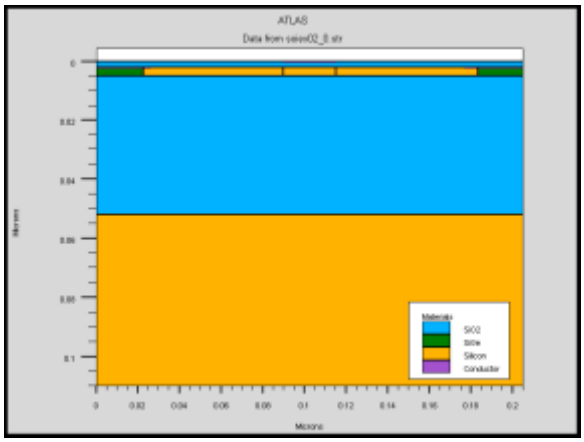

Fig-7(b):-Uniaxial Strained Silicon on Insulator(SSOI) structure at 25nm

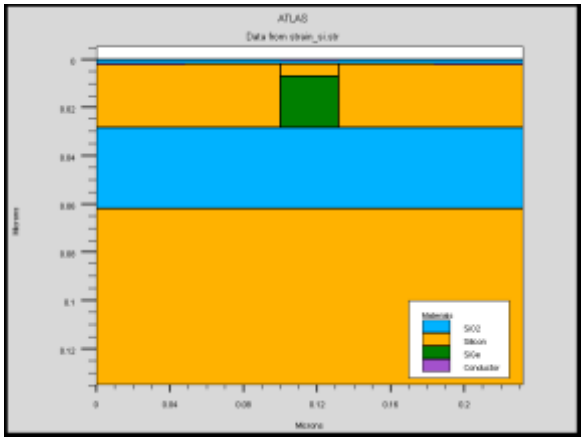

Fig-8(a):-BiaxialStrained Silicon on Insulator(SSOI) structure at 32nm

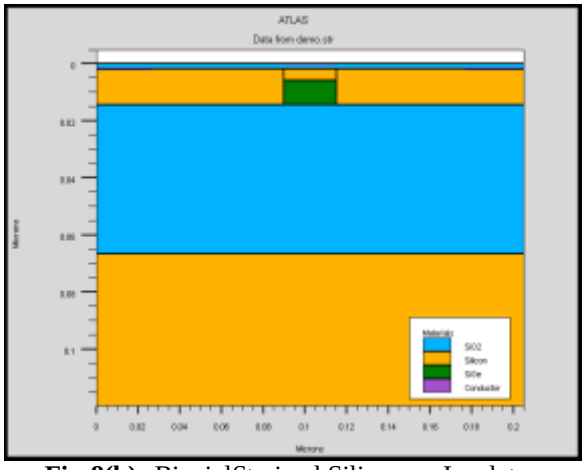

Fig-8(b):-BiaxialStrained Silicon on Insulator (SSOI) structure at 25nm

Figure 7(a) & Figure 7(b) shows the Simulated strucure of Uniaxial Strained Silicon on Insulator(SSOI) at 32nm & 25nm respectively.

Likewise, Figure 8(a) & 8(b) shows the Simulated structure of Biaxial Strained Silicon on Insulator(SSOI) at 32nm & 25nm respectively.

Figure 9(a) shows the Transfer Characteristics of Silicon on Insulator(SOI) at 32nm &Figure 9(b) shows combined characteristics of Silicon on Insulator(SOI) at 32nm &25nm respectively and it has been found that Drain current increases as we decrease the technology node because Drain current of SOI at 32nmis 0.043mA and at 25nm it becomes 3.0522mA.

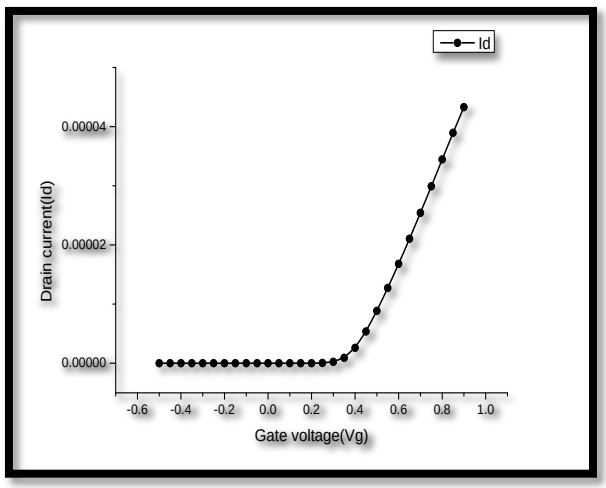

Fig-9(a) Id-Vg characteristics of Silicon on Insulator(SOI) at 32nm

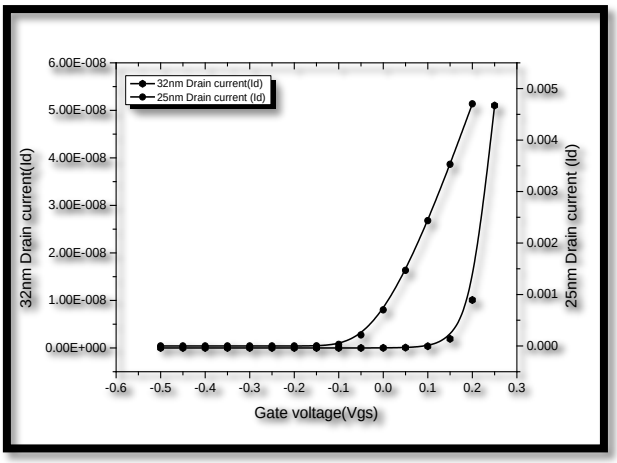

Fig-9(b) CombinedI_d versus V_g characteristics of Silicon on Insulator(SOI) at 32nm and 25nm.

Figure 10(a) shows the Transfer Characteristics of Uniaxial Strained Silicon on Insulator(SSOI) at 32nm & Figure 10(b) shows combined characteristics of Uniaxial Strained Silicon on Insulator(SSOI) at 32nm&25nm respectively and it has been found that Drain current increases as we decrease the technology node because Drain current of SOI at 32nm is 0.1105mA and at 25nm it becomes 4.7031mA.

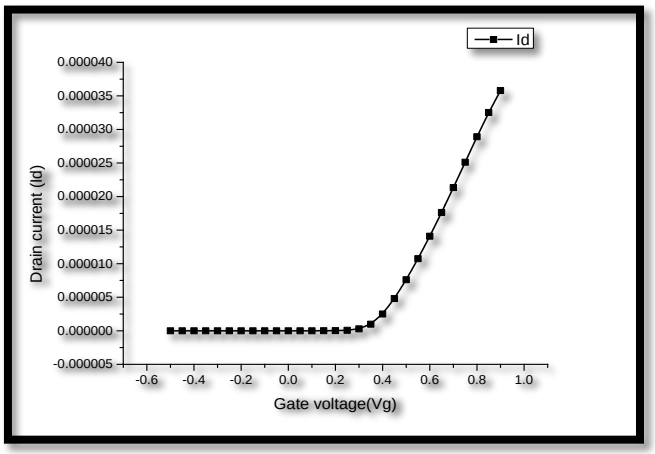

Fig-10(a)-: Id-Vg characteristics of Uniaxial Strained Silicon on Insulator(SSOI) at 32nm

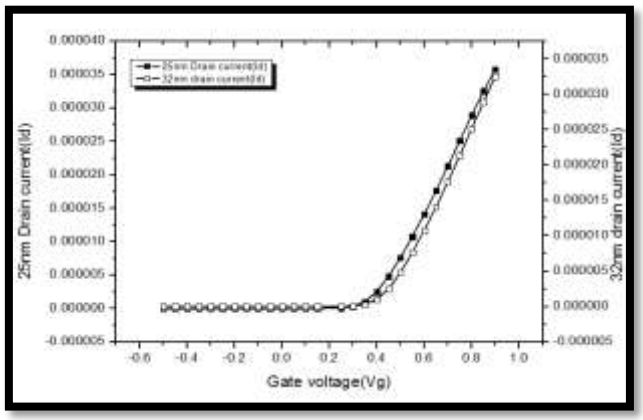

Fig-10(b)-: Combined $I_d$versus V_g characteristics of Uniaxial Strained Silicon on Insulator(SSOI) at 32nm and 25nm

Figure 11(a) shows the Transfer Characteristics of Biaxial Strained Silicon on Insulator(SSOI) at 32nm & Figure 11(b) shows combined characteristics of Biaxial Strained Silicon on Insulator(SSOI) at 32nm&25nm respectively and it has been found that Drain current increases as we decrease the technology node because Drain current of SOI at 32nm is 0.273mA and at 25nm it becomes 6.12mA.

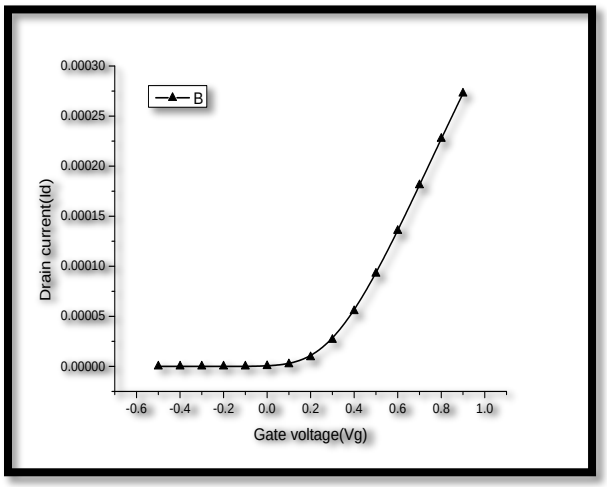

Fig-11(a)-: Id-Vg characteristics of Biaxial Strained Silicon on Insulator(SSOI) at 32nm

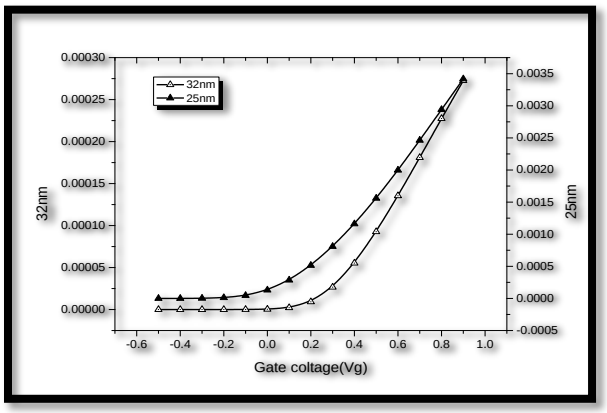

Fig-11(b)-: Combined I_d versus V_g characteristics of Biaxial Strained Silicon on Insulator(SSOI) at 32nm and 25nm

Figure 15(a) & 15(b)shows the comparison between SOI & Strained Silicon at 32nm & 25nm respectively. As shown in Figure 12(a) Drain Current for SOI is very small shown by rectangular boxes and drain current slightly increases for Uniaxial as shown by triangular boxes and drain current again increases at Biaxial shown by circles.The values of Drain current for different structures at 32nm technology node is shown in Table 3.

Likewise,in Figure 12(b)Drain Current for SOI is small shown by circles and drain current slightly increases for Uniaxial as shown by rectangular boxes and drain current again increases at Biaxial shown by triangular boxes .The values of Drain current for different structures at 25nm technology node is shown in Table 4.

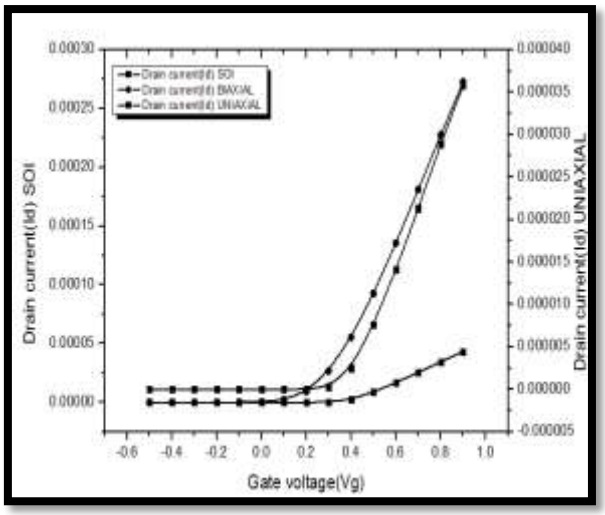

Fig-12(a)-: Comparison Characteristics of Strained SOI & SOI at 32nm

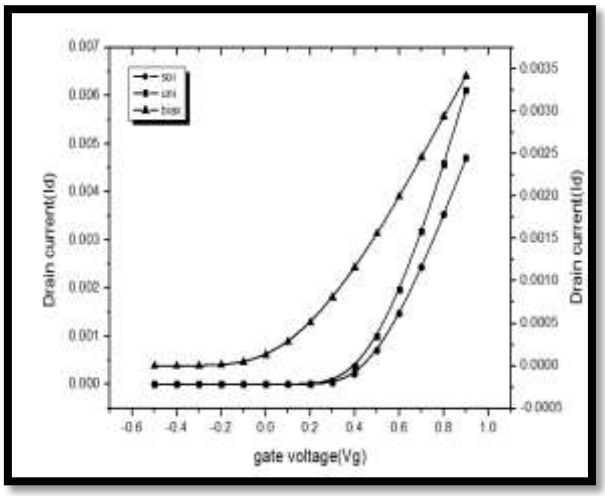

Fig-12(b)-: Comparison Characteristics of Strained SOI & SOI at 25nm

Table- 3 shows the simulated results of Drive current(On-current) and Leakage current(Off-current) of SOI , Biaxial strain and Uniaxial Strain at 32nm.Table-4 shows the simulated results of On-current and Off-current of SOI , Biaxial Strain and Uniaxial Strain at 25nm.

Table-3: Drive current & Leakage current values at 32nm

Structures	Ion(mA)	Ioff(μA)
SOI	**0.043075**	**0.5775**
BIAXIAL STRAIN	**0.273**	**9.5**
UNIAXIAL STRAIN	**0.1105**	**4.625**

Table-4: Drive Current & Leakage Current values at 25nm

STRUCTURES	Ion(mA)	Ioff(µA)
SOI	3.0522	12.5
BIAXIAL STRAIN	6.12	22.84
UNIAXIAL STRAIN	4.7031	22.45

3. CONCLUSION & FUTURE SCOPE

It can be concluded that Strained Silicon CMOS is the alternative for improving a conventional CMOS rather than scaling down the current technology of conventional CMOS. By growing a Strained Silicon layer on top of the relaxed SiGe layer at the channel, this technology allows the enhancement of the carrier mobility, thus delaying the need for the new gate stack materials and improving the overall performance of the device.

It has been Clear that Biaxial (Substrate Induced strain) Strained SOI is better than the Uniaxial(process Induced)Strained SOI because Drive current increases in Biaxial as compare to Uniaxial Strained SOI and this is the need of the device when drive current increases device can be work faster. On the other hand, one of the most important advantages of globally strained SSOI is the scalability to thinner device and insulator layers. Also there are some challenges and drawbacks which must be overcome to fully utilize the improvements of strained silicon technology.To continue the Moore's law and to improve I_{ON}/I_{OFF}, new nontraditional structures like FINFET, DGFET, TGFET and multi gate FET etc. can be investigate at less than 25nm technology node.

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