A NEW APPROACH FOR EFFICIENT SOFT-SWITCHING TECHNIQUE TO INCREASE POWER CONVERSION

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Abstract

Increasing power conversion efficiency is the optimization problem considered in this paper which focuses on soft-switching techniques in order to solve it. Fuel cell (FC) systems with full-bridge topology are considered for the empirical study. Minimizing conduction losses is the aim of the work. In order to focus on it right-aligned modulation sequence is built. At the same time soft-switching techniques are used in the well known MOSFETs. As conventional series conductors are not practically feasible, this paper focuses on combination of techniques to have various benefits such as reduction of stress in switches, minimizing transformer ringing, and minimizing reverse-recovery losses. Different loading conditions are explored and the results observed. Simulation study of the proposed soft-switching techniques is made using Simulink to demonstrate the proof of the concept. The reference topology employed is phase-shift zero-voltage switching to show the mechanisms. Empirical results revealed that the proposed simulation model was able to show soft-switching transitions, modulation benefits, besides validating efficiency gains.

Keywords: *Power Electronics, Fuel Cell (FC), Soft-Switching Techniques, Modulation, Power Conversion*

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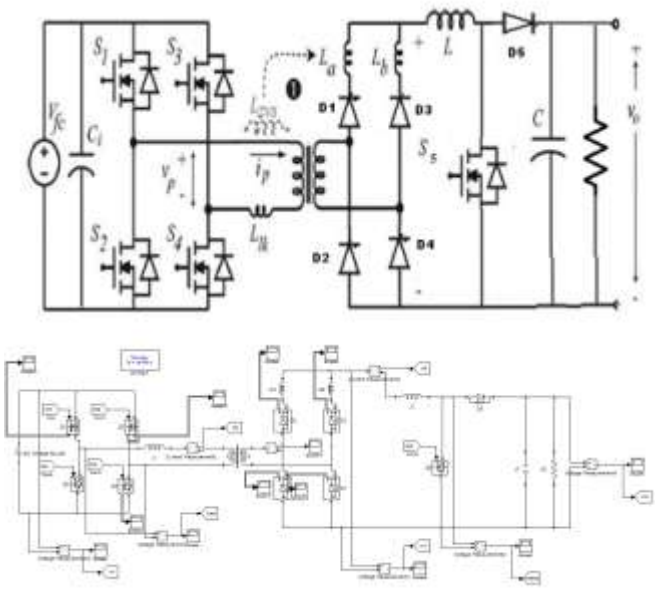
1. INTRODUCTION

Power electronics plays a role in controlling the conversion of electric power and deals with and control of electronic systems. With respect to fuel cells, power electronics provides an interface between loads and fuel cells. Converters in power electronics ensure that power is reliably delivered in the required formats such as AC or DC. In fact fuel cells are power sources that are meant for converting energy from electrochemical format to electrical energy format with low emissions and high efficiency. Unregulated voltage can be produced by a proton exchange membrane. When number of cells is connected, it forms a fuel cell stack. When many cells are stacked, there are mechanical challenges as they can run continuously based on the feeding of reactant. With respect to fuel cell power sources, there are many approaches for power conversion. They are based on different topologies such as current-fed, push-pull, and full bridge.

Many researchers contributed towards the fuel cell power conversion technologies. Recently a three-phase version of full-bridge converter is proposed as explored in [10]. It is based on a clamp circuit and transformer connection. Δ-Y. Other researches include full-bridge forward dc-dc converter along with rectifier [9], push-pull topology with high voltage-conversion ratio [8], push-pull topology with grid connected inverter system [7] and a modular architecture based on push-pull topology for reliable and scalable service. Other contributions include a family of phase-shift ZVS with auxiliary circuits [11], three-phase converters, and inventions on other topologies such as output-voltage doubler and input-voltage doubler for efficient voltage conversion ratio. With respect to high-input-voltage converters switching losses are minimized. However, FC power conversion involves low input voltage, high input current and poor regulation. Generally achieving ZVS with low voltage does not result in significant efficiency gains. As FC is known for high-current and low-voltage power source, there are technical challenges. For instance conduction losses are more than switching losses. Therefore it is essential to ensure reduction in conduction losses besides, realizing high-current inductors, minimizing reverse-recovery losses, reducing transformer oscillations, and achieving high efficiency. In order to overcome the aforementioned issues, this paper focuses on proposing a novel approach for soft-switching technique using full-bridge forward topology.



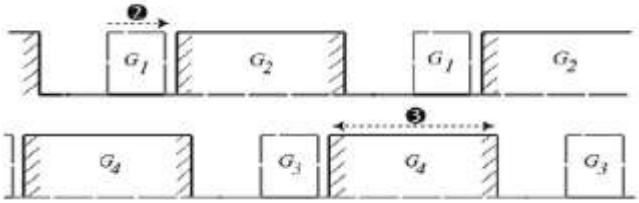


Figure 1: Conceptual schematic and gate waveforms of proposed topology

As shown in Figure 1, there are changes made to FC power conversion process for high efficiency in different loading conditions. Many researchers contributed towards FC power conversion and other related researchers. This is found in the literature [1]-[6] and [12]-[20]. In this paper we introduced soft-switching techniques for efficient power conversion. The remainder of the paper is structured as follows. Section 2 covers preliminaries. Section 3 presents proposed right-aligned modulation with full-bridge topology. Section 4 focuses on loss reduction effects vs. operation intervals. Section 5 presents empirical results while section 6 concludes the paper besides providing directions for future work.

2. PRELIMINARIES

A. Voltage Regulation Process in FC

Under different operating conditions, polymer-electrolyte FC had different regulation characteristics. Thus it helps in the good design of power conditioning stages. This topology is associated with both Direct Methanol FC (DMFC) and PEMFC. Fuel is the main contributor to output voltage in case of DMFC. Output voltage is affected by output current significantly. In the same fashion output power is influenced. With respect to DMFC the factors that influence output voltage are operating temperature, oxygen flow rate, fuel flow rate and fuel. At the same time output current also influences output power and output voltage. In order to illustrate this, set of experiments are made with Simulink. The observations are interesting. DMFC's output voltage is affected by output current and operating temperature. Therefore it is clearly understood that modification of operating conditions can improve the results. Another observation is that the transition rate from a polarization curve to another is slow when operating conditions are changed. The rationale behind this is that heat capacity of the cell is high besides slow mass transport process. Nevertheless, when there is change in the output current, there is fast dynamic response under fixed operating conditions. Thus it became important to have empirical study under low-voltage, high current and poor voltage regulation.

3. PROPOSSED MODULATION IN FULL-BRIDGE TOPOLOGY

This section provides details of full-bridge forward converter with respect to FC power conversion besides other relevant information.

A. Full-Bridge Input Stage

While making simulations on the full-bridge topology importance is given to getting rid of conduction losses and high current bulky inductor in MOSFETs. It is achieved by removing traditional inductor and focusing on the right-aligned sequence of pulses. It can be observed in Figure 1. And Figure 2 presents MOSFET with conduction losses.

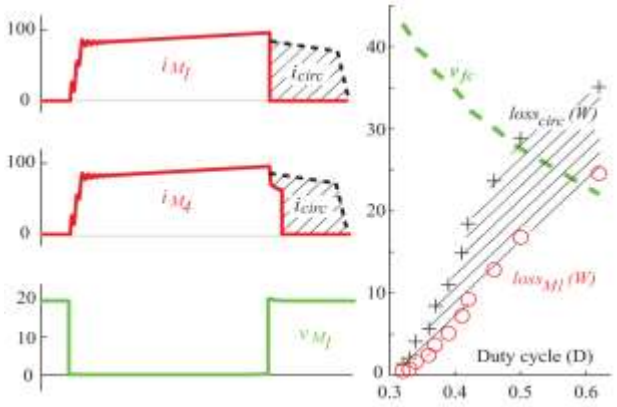


Figure 2: Circulating current causing conduction losses of MOSFET

As shown in Figure 2, the conduction losses are significantly high. The losses are computed in terms of rms value of the current passes through M1 and MOSFET. It is computed as follows.

$$P_{loss_{con}} = R_{ds_{on}} iM1^2$$

With respect to switching losses, the power device is same and it shows less than 6.5 W due to its capacitance. It is shown in the following computation.

$$P_{loss_{coss}} = \frac{1}{2} C_{oss} F_{sw} v f c^2$$

Thus it is understood that with respect to high-current and low-voltage application, the gain achieved with soft-switching is significantly more than the switching losses in heavy load conditions. Interestingly, this is more feasible with respect to lower switches such as M2 and M4 in terms of conduction losses and ZVS. This is due to the changes made to modulation appropriately. The effect of this is the reduction of copper losses found in the windings of transformer and thus finally leads to increased power transfer and low leakage inductance.

B. Output Rectifier Stage

In power electronics, it is well known that the reverse recovery and conduction cause power loss in output rectifiers. As output voltage is high, it causes reverse-recovery losses. The reverse-recovery charge is the function which considers operating temperature of the device, rate of change of current and forward conduction current. The estimation of reverse-recovery losses can be made by using reverse applied voltage (VR), switching frequency (Fsw), and recovery charge. It also makes use of peak ringing value as follows.

$P\text{loss} = Q\text{rr}VRF\text{sw}$

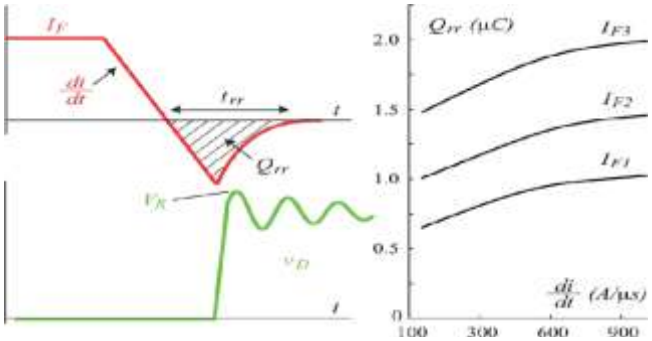


Figure 3 – Relationship between reverse-recovery charge, initial forward current and rate of change current

As shown in Figure 3, it is evident that there is conceptual relationship shown among different aspects such as reverse-recovery charge, initial forward current and rate of change current. By controlling the rate of change of current it is possible to reduce reverse-recovery losses. This is the reason for reflection of Lzvs placed at rectifier D5 and D7 in connection with modulation changes. The process is limited to diodes D5 and D7 and the lower diodes such as D6 and D8 reflect elimination of reverse recovery and prevent transformer oscillations. Moreover, the technique is able to avoid simultaneous conduction of D5, D6, D7 and D8 besides reducing unnecessary ringing. It also eliminates the possible electromagnetic interference (EMI).

4. STUDY OF LOSS-REDUCTION EFFECTS AND OPERATION INTERVALS

The proposed soft-switching techniques along with duty cycle changes in lower switches, right-aligned gate signals in upper switches, and Lzvs inductor reflection are studied. In Figure 4, the technique under study can be seen with switching sequence for MOSFETs M1, M2, M3 and M4. For clarity, transition intervals are exaggerated. Figure 5 shows structured needed by power converter. Many intervals from T1-T12 are considered for observations in switching sequence results. Upper and lower output rectifiers are considered with upper and lower MOSFETs.

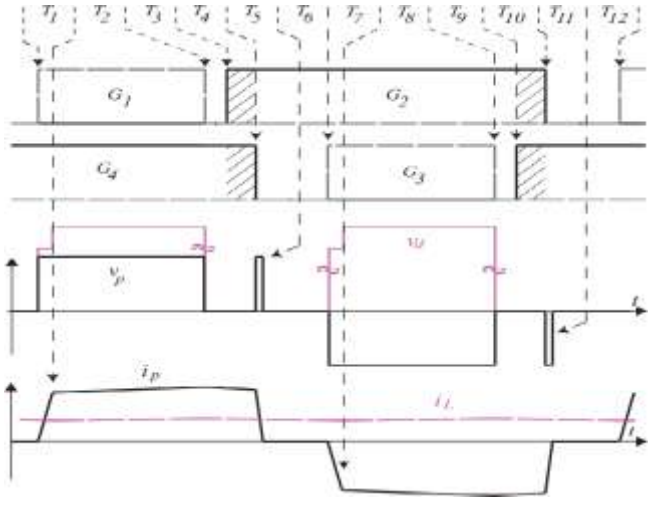
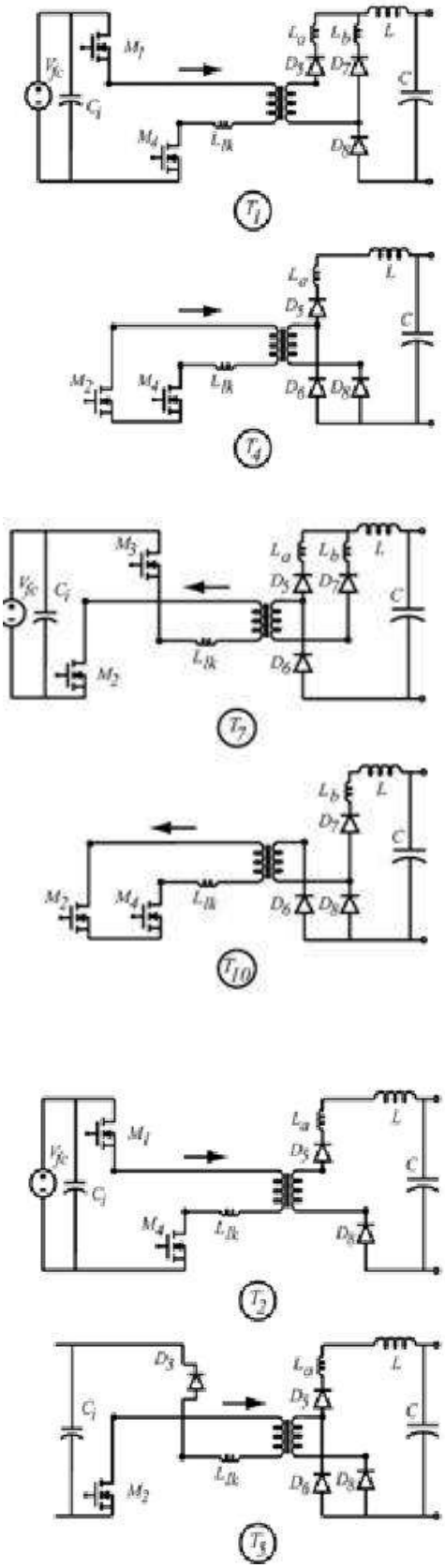


Figure 4: Illustrates switching sequence for MOSFETs M1, M2, M3 and M4

As shown in Figure 4, it is evident that the switching sequence for MOSFETs M1, M2, M3 and M4 with corresponding waveforms is presented.



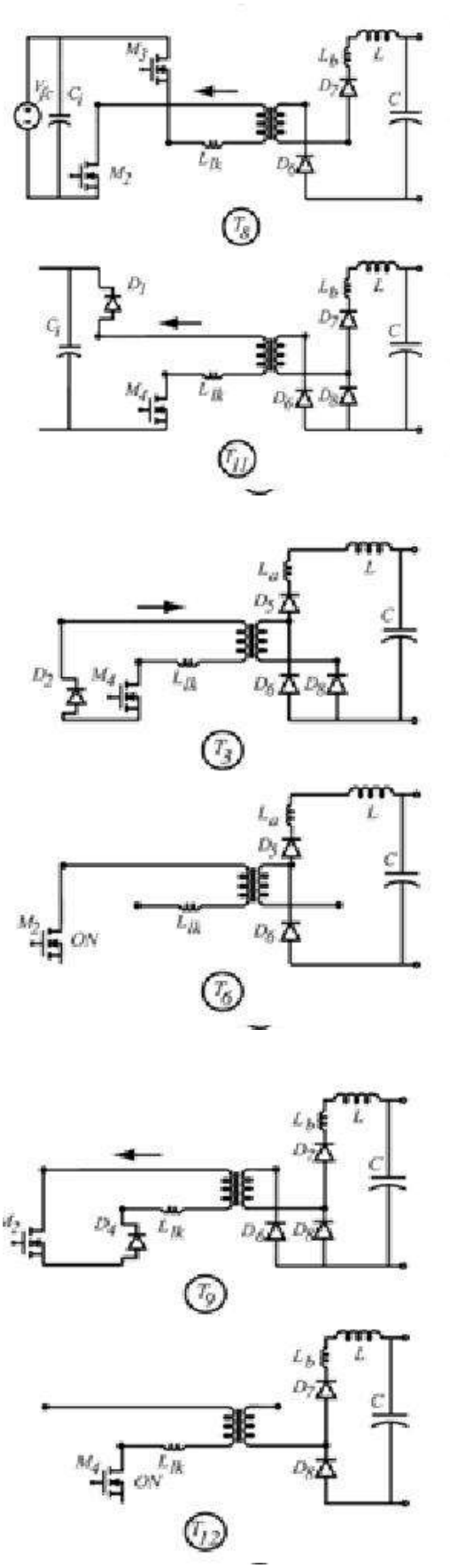


Figure 5: Illustrates power converter structures with intervals T1-T12

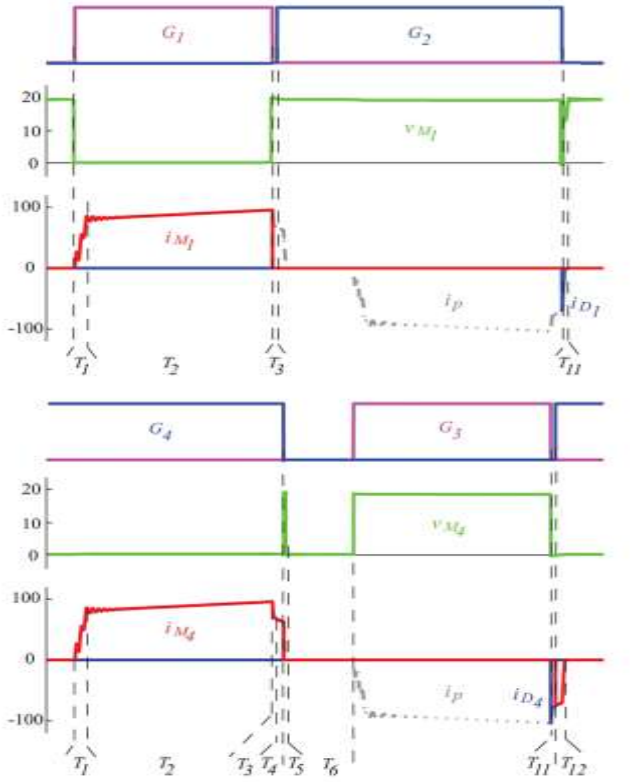


Figure 6: Illustrates M1, M4 waveforms, G1-G4 signal gates and D1, D4 diode waveforms

As shown in Figure 6, wave forms are shown for M1 and M4 and diodes D1 and D4. It does not show waveforms for M2 and M3 and corresponding diodes such as D2 and D3. With respect to interval T1, the right-alignment modulation starts here. It causes no circulating current in the primary. Then M1 turns on and the current path is from M1 through M4. M1 is with ZCS. During T1 primary current rate of change is limited by inductors La and Llk. In interval T2, MOSFETs M1 and M4 are on and continue as power is transformed from input to output. The interval T3 starts when M1 is turned off due to drop of G1. At the same time D2 starts conduction. This interval reflects the dead time between switches M1 and M2. In the same fashion, M2, D2, M4, D4 show their functionality in the next switching cycle.

With respect to interval T4, M2 switch turns on with ZVS. It is a brief time interval which ends with drop of signal of G4. G4 is extended slightly to ensure ZVS present on both lower switches. In interval 5, the energy available with the leakage inductance L1k is returned to capacitors. It is done through body diode D3. As traditional Lzvs is reflected in the secondary, it is possible to minimize inductance in the primary L1k. At the same it the primary current of the transformer is reset to zero. In the interval 6, the circulating current is eliminated in the primary and converted into efficiency gains which are an important feature of FC power

conversion dynamics. Same behaviour is repeated by other intervals from T7-T12 for M2 and M3 with D2 and D3 diodes. The proposed soft-switching techniques eliminate unnecessary circulating current MOSFETs and transformer. This is very important in case of high-current and low-voltage applications in order to reduce conduction losses that are always more than the losses due to switching frequencies. The gains are further enhanced due to optimizations in output rectifiers.

A. Output Rectifier Waveforms

This sub section provides analysis of efficiency gains and waveforms with respect to output rectifier. Figure 7 shows voltage waveforms for diodes D7 and D8.

As shown in Figure 7, reverse-recovery and conduction losses are presented in terms of different intervals. In time interval 1, the recovery process is initiated by D7 and it is limited by Lb. However, there is interleaving action found in La and Lb which causes to have only three forward-biased diodes. Thus it could prevent zero-state in the transformer secondary. Unlike traditional full-bridge converters, this change led to reduction in ringing in T2.

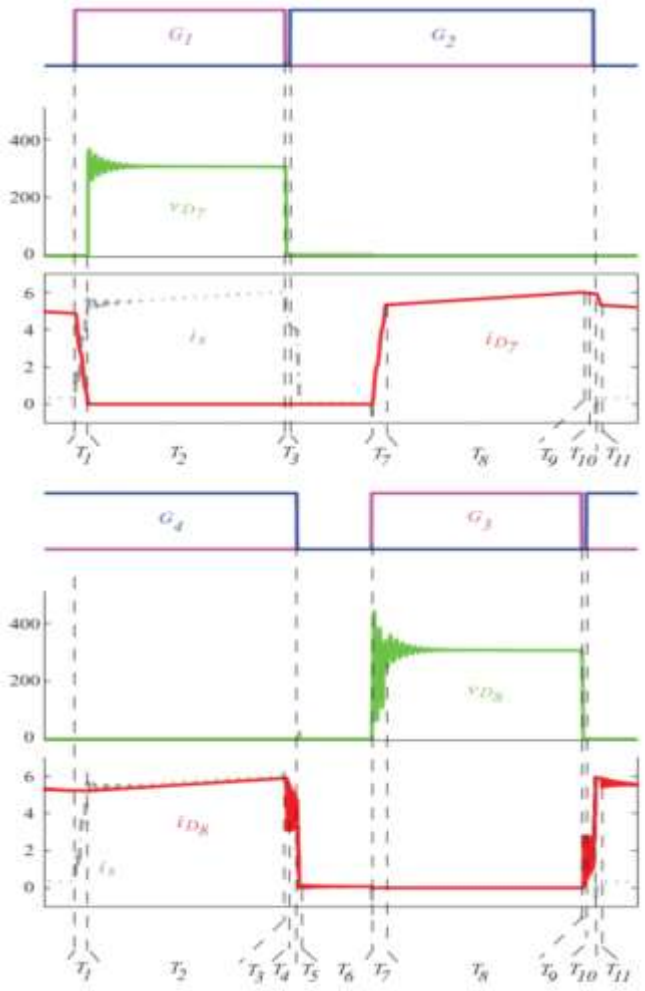


Figure 7: Output rectifiers D7 and D8 with current and voltage waveforms

Once D5 is at the current level, T2 starts. Soft transitions are exhibited by D7 and shows reduced blocking voltage resulting reduced recovery losses. This is achieved by eliminating zero voltage condition in the secondary of the transformer. It prevents an abrupt voltage step. It also eliminates snubber which is required by traditional full-bridge ZVS. T3 exhibits conduction interval of D7. The reverse recovery process is initiated by T4 and T5. In T6, interleaving effect of La and Lb are observed. Due to this, reverse voltage is not experienced by D8. This results in significant efficiency gains diodes such as D6 and D8. It is reflected in waveforms presented in Figure 7. With the proposed soft-switching techniques the following are the improvements observed.

Total recover recovery power losses are controlled effectively La and Lb inductors with respect to D5 and D7.

The diodes D6 and D8 experience reverse-recovery losses which are negligible. This is an improved form over traditional phase-shift ZVS.

Oscillations are reduced due to the presence of La and Lb with regard to D6 and D8. Thus undesirable effects and EMI are minimized. These are the advantages of FC power conversion with the proposed soft-switching techniques.

B. Dynamic Behaviour vs. Frequency Response

With respect to full-bridge topology the frequency response is related to control-to-output feature. It is nothing but a buck-derived topology. Conductor operates in phase-shift ZVS. Generating soft transitions in switches is required along with series inductance to limit rate of change. Thus it can affect control-to-output feature. An artificial dumping effect is found as a result due to series inductance which makes the control-to-output to be flexible. In this study, multiple measurements were employed with appropriate outer voltage and inner current loops. In the modified modulation both control loops are employed to have an efficient power conversion with FC.

5. EXPERIMENTAL RESULTS

A prototype power converter is designed to demonstrate the proof of concept of the proposed soft-switching technique. Measurements are performed by experimenting with resistive loads. The parameters provided in Table 1 are used to build converter. The topology employed was phase-shift ZVS.

Table 1: Parameters used to build converter

Parameter	Value port of proposed topology	Value port of existing topology
v_{fc}	300	300
v_0	68.76	102.6
P_{OROM}	1KW	1KW
Q_1 Q_2 Q_3 Q_4 Q_5	IRFB4110	IRFB4110
D_1 D_2 D_3 D_4	DSEI2x30	DSEI2x30
L	310e-6	310e-6
L_a L_b	310e-6, 310e-6	310e-6, 310e-6
C	4760e-6	4760e-6
C_i	1e-06	1e-06
F_{sw}	40-100KHZ	40-100KHZ
Transf.core	1e3 33.3e3	1e3 33.3e3
Transf.primary turns	1	1
Transf.secondary turns	1	1

With respect to ZVS operation, changes made include removal of La and Lb besides inclusion of Lzvt. The proposed changes are also tested with La and Lb while removing Lzvt. DSP control and modulation are used to with current trends while implementing converter. In other words, the right-aligned modulation is generated. In the same fashion, the drivers of upper MOSFETs are used to generate pulse width modulation for flexibility unlike the approach used in phase-shift ZVS counterpart.

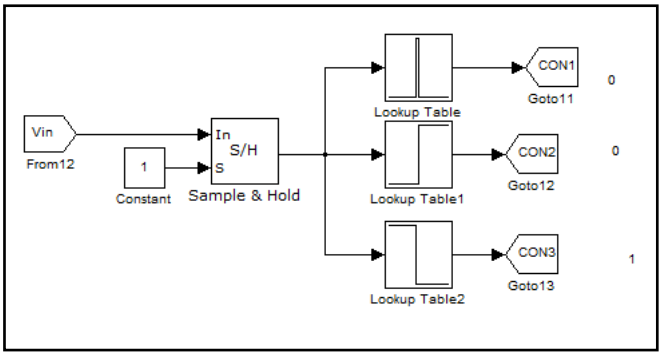


Figure 8: Sample and hold circuit generating voltages at different load conditions

A. Verifying Load at Different Conditions

Input voltages such as v0, 0, con3 are considered for giving to three input switch. When con3 is evaluated to true, the first input is passed to adder 1 through switch.

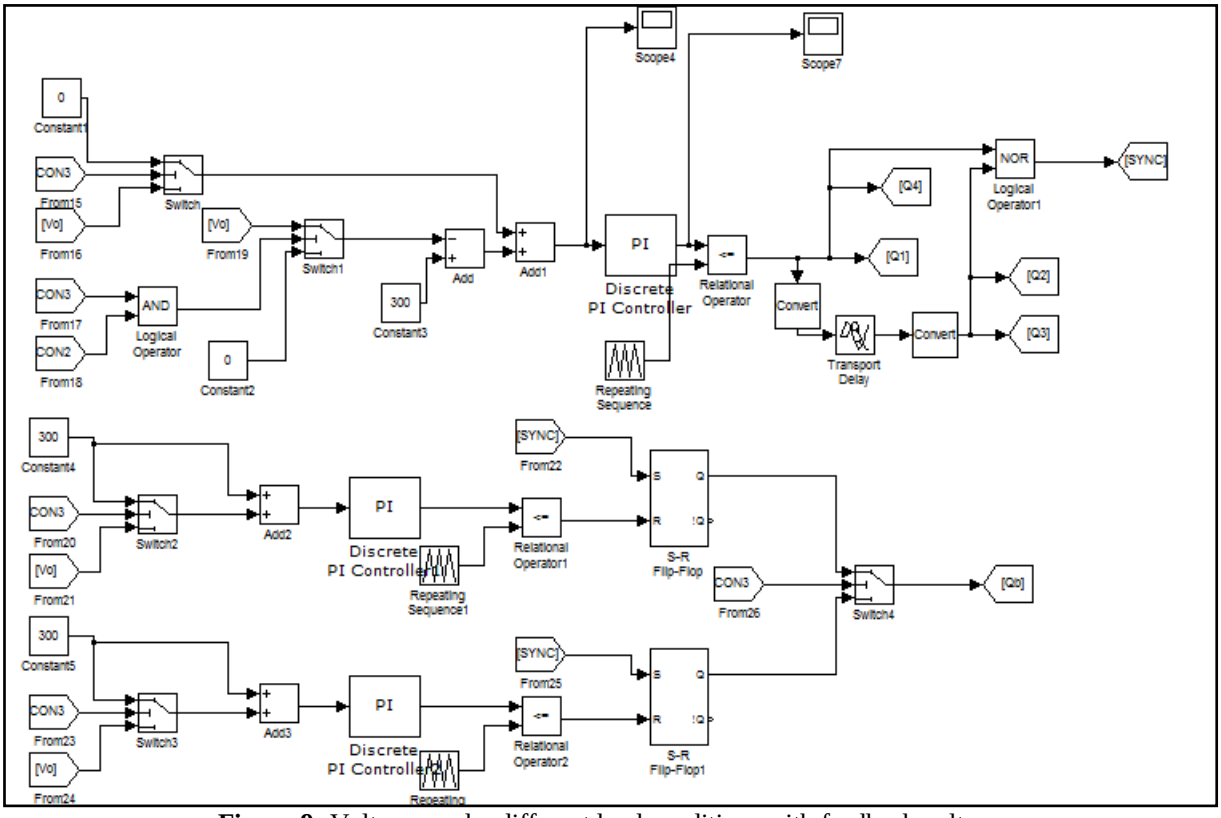


Figure 9: Voltages under different load conditions with feedback voltage

For AND gate, con1 and con2 are given as input while v0 and 0 are given to three input switch to adder. Then the combined output of the two adders is given to controller. Controller output and feedback are given to relational operator or comparator. Combining four switches output is also done and given to sync. By considering two SR flip-flops, sync output and comparator output are given to SR-flip-flop. Finally expected results are obtained under different load conditions.

B. Results

Measuring of a complete switching cycle is made in M1, M4, D7 and D8. This is done to validate medium loading conditions and waveforms. The switching frequency was set to 40 kHz for visualization.

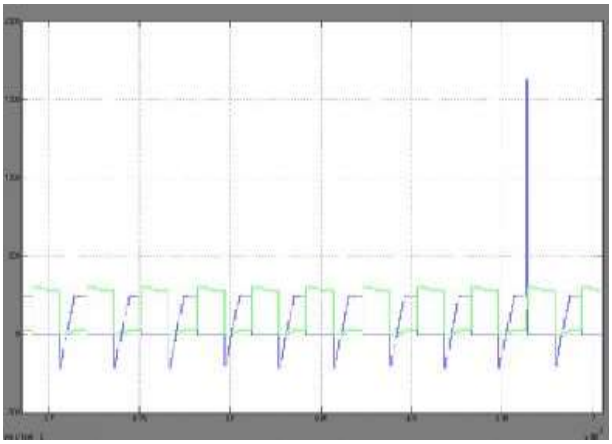


Figure 10: Upper side MOSFET *M*1 waveforms in the proposed modified topology under medium loading condition

As shown in Figure 11, it is evident that waveforms of MOSFET M1 are presented. The waveforms include of secondary transformer current, and gate and drain-to-source voltages. MOSFET current started at zero in the beginning of T1 AND reaches current level of the output-filter slowly at the beginning of T2. During T3, MOSFET is turned off which can limit the conduction interval from T1 to T2. In T11, conduction interval of body diode can be seen.

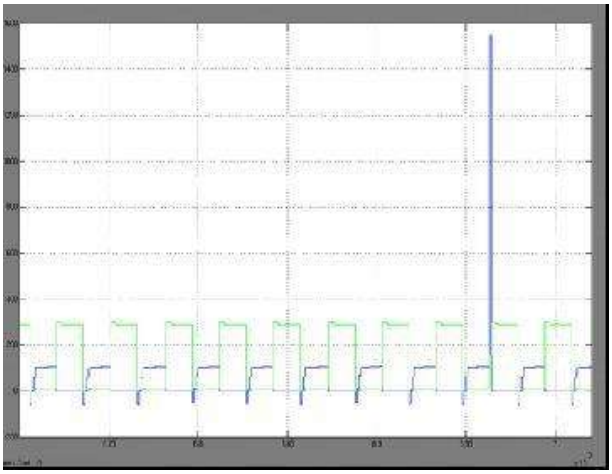


Figure 11: Upper side diode M1 waveforms in the existing topology under medium loading condition

This results in returning the energy of the leakage inductance with regard to input dc bus. Thus it can avoid circulating current in the primary. The input capacitors of the converter can absorb and clamp small energy in the leakage.

In Figure 13, lower MOSFET M4 waveforms are presented. With respect to conduction interval it is similar to that of M1. It shows reduction in conduction losses. Figure 12 and 14 shows the existing MOSFET M1 and M4 graphs while the Figure 11 and 14 show the results of the proposed approach. Conduction losses are reduced with the help of MOSFET switch in secondary side.

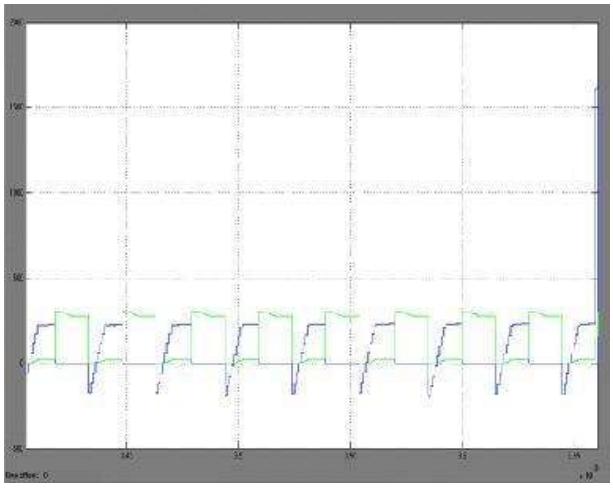


Figure 12: Upper side MOSFET *M*4 waveforms in the proposed modified topology under medium loading condition

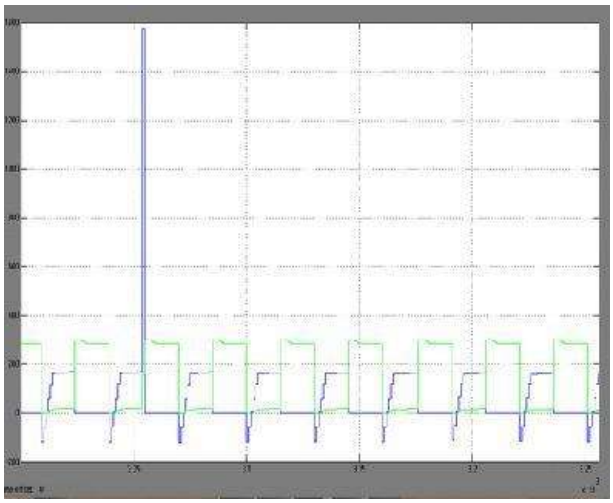


Figure 13: Upper side diode *M4* waveforms in the existing topology under medium loading condition

Fig. 11 shows the waveforms of MOS- FET M 1, including gate and drain-to-source voltages, and the secondary transformer current. It can be seen that the MOSFET current starts at zero (ZCS) at the beginning of T 1 and slowly ramps up until it reaches the current level of the output-filter inductor at the beginning of T 2. The MOSFET turns off during T3, limiting the conduction interval to T1 –T2. The body diode D 1 conduction interval can be seen in T 11,

which returns the energy of the leakage inductance to the input dc bus and avoids circulating current in the primary. The small energy in the leakage is absorbed and clamped by the input capacitors of the converter. The lower MOSFET M 4 waveforms are shown in Fig. 13 .The conduction interval in M 4 is similar to that of M 1, showing reduced conduction losses.

Compare this existing MOSFET M1, M4 graphs with proposed graphs of Fig 10, 12. With the help of MOSFET switch in secondary side we reduce conduction losses.

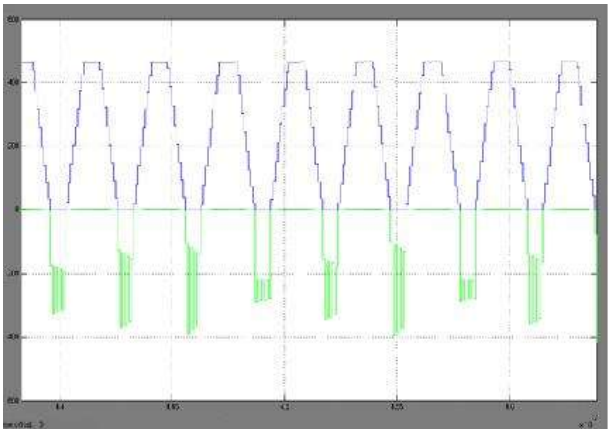


Figure 14: Upper side diode *D8 waveforms* in the proposed modified topology under medium loading condition

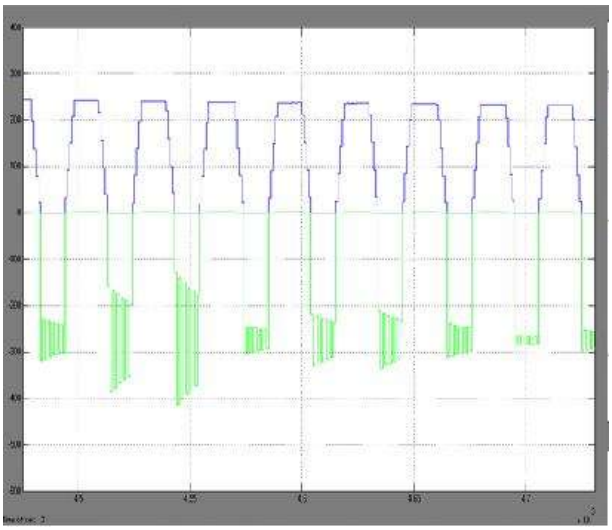


Figure 15: Upper side diode *D8* waveforms in the existing topology under medium loading condition

As shown in Figure 15, the result of interleaving effect of La and Lb during T3-T5 interval, fast transition is experienced by diode D8. The transition is from high conduction current to near-zero current. It is observed that at the beginning of T7, there is partial reflection of converter input voltage to the secondary. This blocks D8 with a transition which results in reverse-recovery losses in D8 which are negligible. The blocking transition results in the moderate ringing at the beginning of T7. At the same time, the upper diode current iD7 increases. The conduction losses are reduced when compared to existing system.

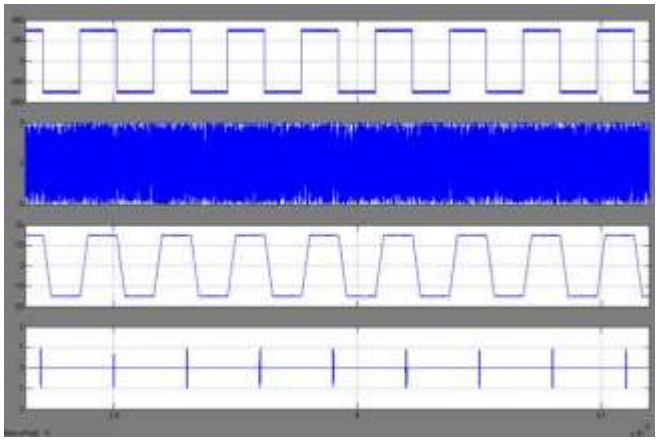


Figure 16: Voltage-Current characteristics of existing system

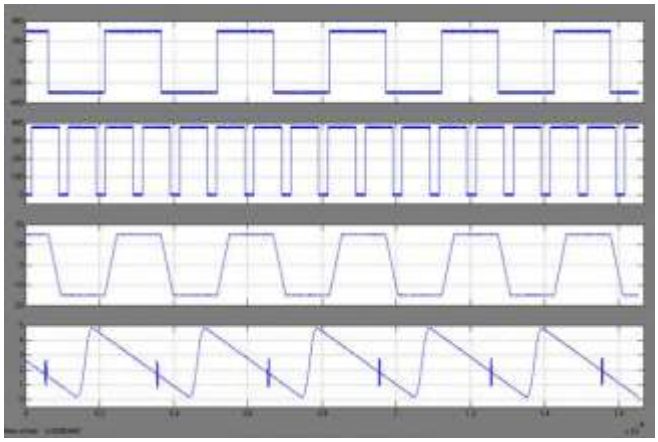


Figure 17: Voltage-Current characteristics of proposed system

As shown in Figure 16, it is evident that voltage and current waveforms are not properly reflected. Unwanted fluctuations are observed. The proposed topology is able to recover such fluctuations as shown in Figure 17.

6. CONCLUSIONS AND FUTURE WORK

In this paper we studied the fuel cell (FC) systems with full-bridge topology for increasing power conversion efficiency. We considered improvement of power conversion in FC systems as an optimization problem. Soft-switching techniques are introduced in order to ensure efficiency gains of FC systems with full-bridge topology. Minimizing conduction losses is the aim of the work. In order to focus on it right-aligned modulation sequence is built. Series of MOSFETs are used in the empirical study along with diodes and gates. As conventional series conductors are not practically feasible, this paper focuses on combination of techniques to have various benefits such as reduction of stress in switches, minimizing transformer ringing, and minimizing reverse-recovery losses. Different loading conditions are explored and the results observed. A simulation study is made using Simulink to demonstrate the proof of the concept. The proposed soft-switching techniques revealed significant performance gains with respect to FC systems using full-bridge topology in terms of efficient power conversion. Empirical results revealed that

the proposed simulation model was able to show soft-switching transitions, modulation benefits, besides validating efficiency gains. In future we intend to investigate on the role of soft-switching techniques further in efficient power conversion.

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