

A GaAs/AlGaAs/InGaAs PSEUDOMORPHIC HEMT STRUCTURE FOR HIGH SPEED DIGITAL CIRCUITS

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Abstract

A double heterojunction GaAs/AlGaAs/InGaAs pseudomorphic depletion mode HEMT has been developed at the gate length of 80nm. The device properties are tested for different biasing potentials at the input and output side. The device is found to exhibit a cut off frequency of 80Ghz. Further, the logic suitability of the device is supported by developing the basic gates used for digital communication i.e., Inverter, Nand and Nor. Thus, enhancement in digital communication can be obtained with the use of HEMTs which provide high speed, low noise applications. Furthermore, with the implementation of universal gates using HEMTs, any digital circuit can be easily implemented. The paper reports a complete method from developing of the structure in Visual TCAD (VTCAD) to further implementing a circuit using the developed structure.

Keywords: HEMT, TCAD, Pseudomorphic, Logic Gates, Digital Applications

1. INTRODUCTION

The emergence of III-V compound semiconductors has given a promising choice for channel material of future. These devices rely on the use of heterojunctions for their operation and high electron mobility transistors (HEMTs) are one of the most mature ones of the new generation of the III-V semiconductor transistors. The heterojunctions in these devices are formed between semiconductors of different compositions and bandgaps, e.g. GaAs/AlGaAs and InGaAs/InP. These novel devices offer potential advantages in microwave, millimeter-wave, and high speed digital integrated circuit (IC) applications over the homojunction devices. With heterojunctions, device designers can vary the band structure (and hence the electric field) as well as the doping level and thus obtain significant improvements in charge transport properties. In the HEMT, the epitaxial layer structure is designed so that free electrons in the channel are physically separated from the ionized donors, and electron mobility is enhanced by reducing ionized scattering [1].

1.1 Heterostructures

A heterostructure or heterojunctions occurs when contact is made between two semiconductor materials with different band-gap energies. Heterojunction FETs have shown great promise for high speed devices where the conventional MOSFET technology is reaching its limit due to various short channel effects and velocity saturation effects. The band-gap in the III-V semiconductors can be engineered by varying the mole fraction of the constituents and hence the device properties can also be tailored [2].

Heterojunction devices present difficult challenges to both device fabrication and device modeling engineers. The

fabrication process requires doping density, layer thickness and material composition to be altered abruptly during the growth of the device structure. Extremely thin heterostructures are required in modern HEMT devices. Doping layer thickness and composition must all be very tightly controlled to produce a useful device. Fabrication of heterostructures also requires consideration of material lattice constants, thermal expansion coefficients and interface states [3].

Fig. 1 shows the band diagram for a p-n heterojunction. The p-type material (GaAs) has a smaller band-gap than the n-type material (AlGaAs).

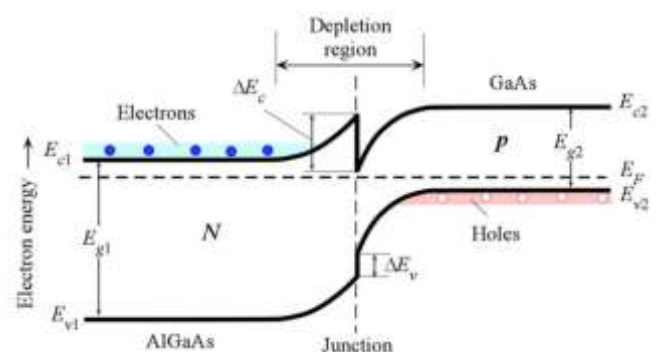


Fig 1: Energy band diagram for a p-n heterojunction

The band discontinuities exist in both the conduction band and valence band. In Fig.1 these discontinuities are labeled as “ ΔE_c ” and “ ΔE_v ”. The amount of conduction and valence band discontinuity for two materials forming a heterojunction is determined by a number of factors, including the band-gap energies and electron affinities of each of the materials [3].

Fig. 2 presents the band diagram for a Schottky barrier placed on a semiconductor heterostructure typically exploited for HEMT fabrication. The wide band-gap material is doped n-type, but is depleted of free carriers by the reverse or zero-biased Schottky contact.

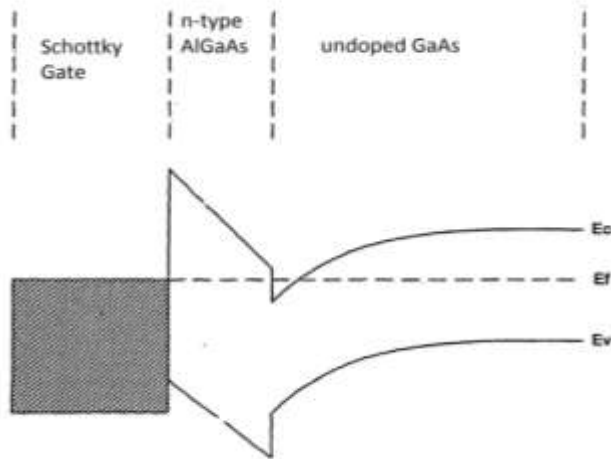


Fig 2: Energy Band diagram for a Schottky contact made to a heterostructure

The narrow band-gap material is lightly doped p-type. The most important feature of the band diagram related to HEMT operation occurs at the heterojunction interface between the two materials. At this boundary, the band-gap discontinuities cause the conduction band of the narrow band-gap material to dip below the Fermi level. The free carrier concentration is very high where the dip occurs. This region of high carrier concentration is very extremely thin and is the primary property of the heterostructure exploited in the fabrication of HEMTs [3].

2. DEVICE STRUCTURE

Introduced in 1981, the conventional AlGaAs/GaAs high electron mobility transistor has offered both high speed and excellent gain, noise performance at microwave and millimeter-wave frequencies [3]. The HEMT represents an evolutionary improvement in the GaAs MESFET and has been used extensively in both hybrid and monolithic circuits. The HEMT has two ohmic contacts (source and drain) and a Schottky gate which modulates the flow of current in the channel between the two contacts.

As shown in Fig.2, because of the conduction band discontinuity, ΔE_c , between the high band-gap AlGaAs and the undoped GaAs, electrons are localized to a thin ($\sim 80\text{\AA}$) two-dimensional electron gas layer on the GaAs side of the AlGaAs/GaAs heterojunction interface. Because there are no donor atoms intentionally present in the undoped GaAs layer, electrons in the 2-DEG channel do not undergo impurity scattering and hence exhibit high mobility and velocity. This structure scheme gives the HEMT not only superior electron transport properties in the channel but also much higher sheet charge density for high frequency operation [1].

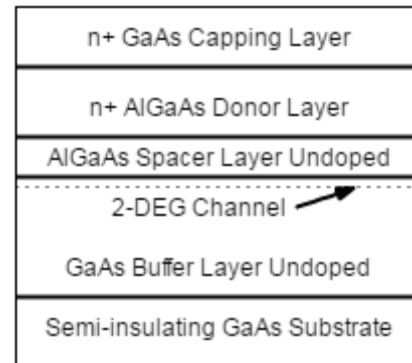


Fig 3: GaAs based conventional HEMT

As shown in Fig.3, the conventional AlGaAs/GaAs HEMT structure is typically composed of (a) n+ GaAs capping layer, (b) n+ AlGaAs donor or gate-barrier layer, (c) undoped AlGaAs spacer layer, (d) undoped GaAs channel, (e) undoped GaAs buffer, and (f) GaAs semi-insulating substrate.

One way of improving the HEMT performance is to use InGaAs as the two-dimensional electron gas material instead of GaAs as shown on Fig.4. The benefits of using a thin InGaAs layer as the pseudomorphic channel in a HEMT include the enhanced electron transport in InGaAs as compared to GaAs, improved confinement of carriers in the quantum well channel, and larger conduction band discontinuity at the AlGaAs/InGaAs hetero-interface which allows even higher current density and transconductance than possible with a AlGaAs/GaAs conventional HEMT.

2.1 GaAs based Pseudomorphic HEMT layer design

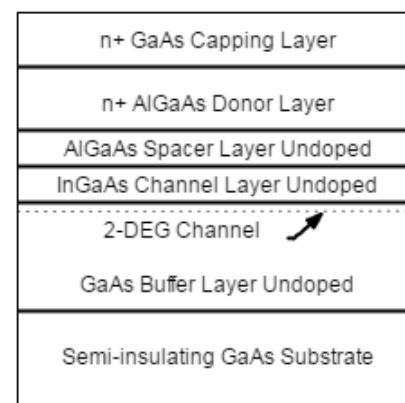


Figure 4: GaAs based pseudomorphic HEMT

The following sub-sections describe each layer and its importance for the HEMT structure.

i. Capping Layer:

The GaAs capping layer, typically heavily doped with Si at approximately $10^{18}/\text{cm}^3$, provides good ohmic contact to the HEMT, reduces the device resistance, and also protects the AlGaAs donor layer from surface oxidation and depletion.

ii. AlGaAs Donor Layer:

The AlGaAs donor layer should be depleted from both the AlGaAs/GaAs heterojunction interface and the Schottky gate to eliminate the parallel conduction of the AlGaAs in a HEMT. The donor layer is typically uniformly doped with Si at a very high doping level of approximately $10^{18}/\text{cm}^3$. An important parameter in the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ donor layer is the AlAs mole fraction x . The conduction band discontinuity, ΔE_c , at the $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ heterojunction interface at room temperature is related to x by

$$\Delta E_c = 0.806x(x < 0.47) \quad (1)$$

iii. Spacer Thickness:

In a HEMT, even though the electrons and donors are separated spatially, their close proximity allows an electrostatic interaction called Coulomb scattering. By setting the donors away from the interface, Coulomb scattering by the positive charge of donor atoms can be reduced. This is done by inserting a thin spacer layer of undoped AlGaAs with a typical thickness of 20-50 Å between the AlGaAs donor layer and GaAs channel of a HEMT to separate the negative charged 2-DEG from the ionized dopant atoms.

iv. Pseudomorphic Channel:

GaAs-based pseudomorphic HEMT differs from the conventional AlGaAs/GaAs HEMT in that a thin (typically 20-500 Å) layer of $\text{In}_x\text{Ga}_{1-x}\text{As}$ ($x=0.15-0.35$) is inserted between the doped AlGaAs barrier layer and GaAs buffer layer. The benefits of using this layer includes enhanced electron transport in InGaAs as compared to GaAs, improved confinement of carriers in the quantum well channel, and the larger band discontinuity at the AlGaAs/InGaAs hetero interface which allows higher sheet charge density and hence higher current density and transconductance than possible with AlGaAs/GaAs conventional HEMT.

3. DEVICE DETAILS AND SIMULATION

Fig.5 shows the structure of AlGaAs/InGaAs/GaAs pseudomorphic double heterojunction device simulated with GaAs substrate of thickness 130nm, AlGaAs layer of thickness 8nm, InGaAs channel of thickness 4nm, AlGaAs barrier layer of thickness 10nm and GaAs capping layer of thickness 10nm. Total length of the device is set to 160nm. The capping layer is doped with the donor concentration of 10^{18} and the two AlGaAs layers are doped with 10^{18} and 10^{16} respectively. The mole fraction for InGaAs and AlGaAs is set to 0.3. In the device simulation, Cogenda Visual TCAD is used.

The pseudomorphic GaAs/InGaAs/AlGaAs double heterojunction as simulated in Visual TCAD's GUI interface is shown in Fig. 6. Similar structure can be implemented using the programming reference as well. Both of which provide similar results. In double heterojunction, carriers are introduced into the InGaAs pseudomorphic channel by

doping the AlGaAs on both sides of the InGaAs. The result is high current density and high power-handling capability.

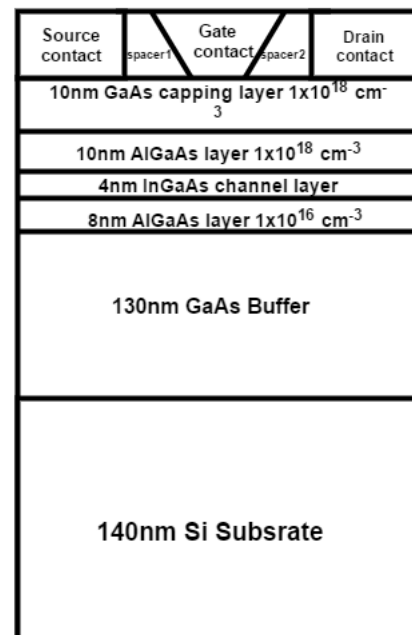


Fig 3: Device structure

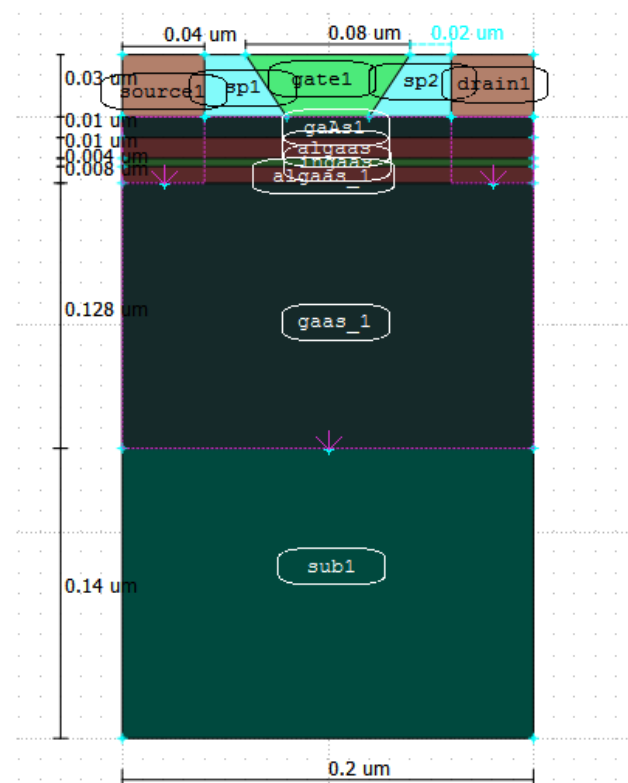


Fig 4: Device structure simulated in Visual TCAD

4. RESULTS AND DISCUSSION

The device structure shown in Fig. 6 is initially simulated for its DC response and the current-voltage characteristics of the device are plotted. A sharp dip in the conduction edge occurs in the HEMT at the AlGaAs/InGaAs boundary. This results in a high carrier concentration in a narrow region along the GaAs side of the heterojunction. The free-electron

concentration occurs over such a thin region that it is described as a two-dimensional electron gas (2-DEG). Electrons travelling in this region do not encounter ionized donor atoms because the GaAs is undoped.

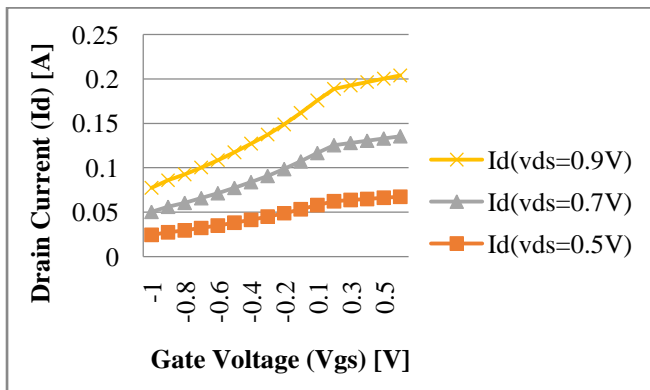


Fig 5: Input characteristics for HEMT

Fig. 7 shows the results of simulating the device for DC parameters and plotting curves for the input voltage (V_{gs}) ranging from -1V to +0.5V in steps of 0.2V with $V_{ds}=0.5V$, 0.7V and 0.9V respectively and output current (I_{ds}) for different values of output voltage (V_{ds}).

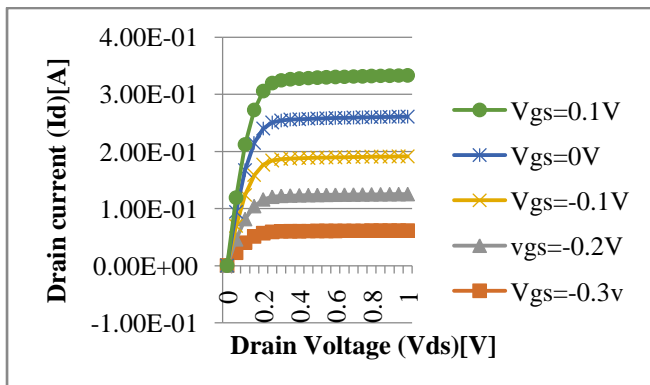


Fig 6: Output characteristics for HEMT

The output curves of HEMT plotted for output voltage (V_{ds}) ranging from 0V to 1V with $V_{gs}=0.1V$, 0V, -0.1V, -0.2V and -0.3V and output current (I_{ds}) are shown in Fig. 8.

As evident from Fig. 7 and Fig. 8, the device behaves in depletion mode and current flows through the device in the absence of the applied gate bias as well. This flow of current is proportional to the applied drain-source voltage. As drain-source bias levels are increased, electron velocity and the current levels saturate. The saturated current level is determined primarily by the sheet carrier density of 2-DEG that forms in the structure.

The current gain of HEMT is given by

$$\text{Gain} = \frac{\Delta I_d}{\Delta I_g} \quad (2)$$

Fig. 9 signifies that the device's gain reduces below 1, after 80GHz after which no further amplification can be obtained.

Thus, the device can be used for high frequency operations up to 80GHz.

Furthermore, the higher g_m and f_T of the pseudomorphic device make them extremely attractive for high speed and low power digital applications. Also HEMTs exhibit promising logic characteristics such as gate delay (CV/I), subthreshold slope (S), drain induced barrier lowering (DIBL) and I_{on}/I_{off} which are considered as figures of merit for logic applications [5]. HEMTs are also very sensitive to optical illumination and find application in OMIMC's [6].

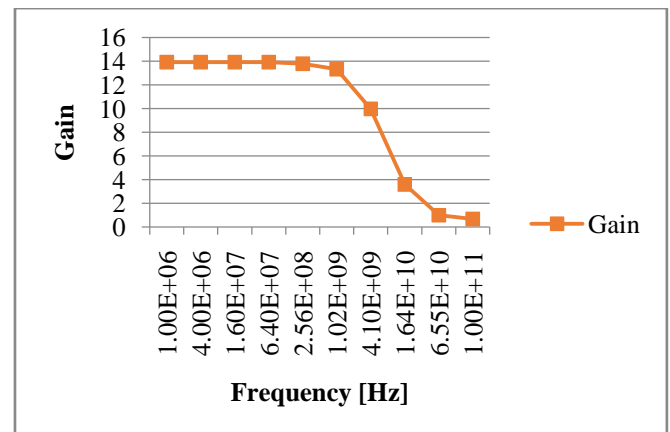


Fig 7: Frequency versus Current gain

Considering the above advantages, the pseudomorphic HEMT is simulated for the implementing the basic building blocks of digital applications i.e. the logic gates.

Following are the steps to be followed in VTCAD to implement logic gates' circuits.

1. The device is first designed and developed in either the GUI or programming reference of VTCAD (Fig. 6).
2. Appropriate meshing of the device is done to obtain the desired response.

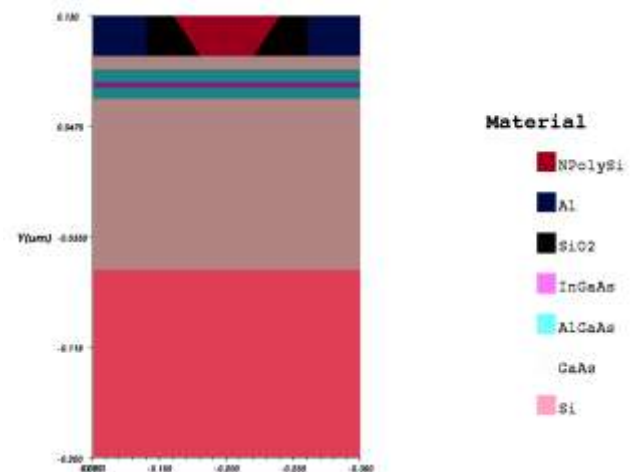


Fig 8: Device file generated after meshing

3. The performance parameters of the device are determined and verified to meet the standard requirements in the device simulation part of the software (Fig. 11).

4. If all the characteristics of the device are found to be appropriate as shown in Fig. 7 and Fig. 8, a circuit symbol is prepared with appropriate contacts and interconnections.

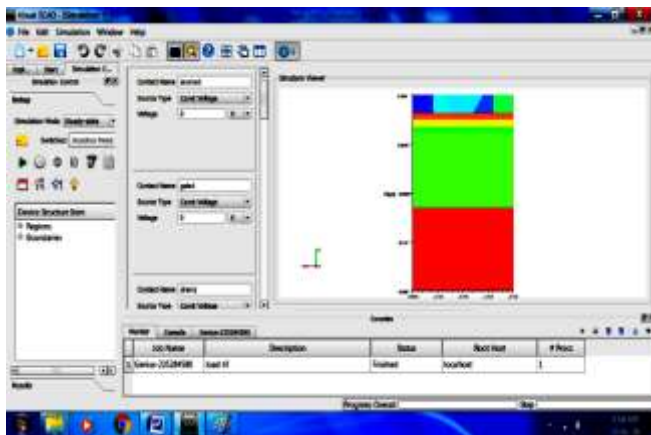


Fig 9: Simulation file in VTCAD

As shown in Fig.11, the desired input biases can be given on the contacts and the results can be observed.

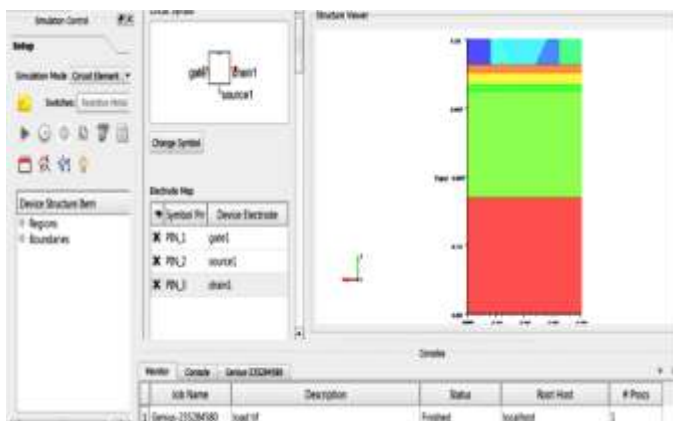


Fig 10: Circuit element in VTCAD

5. If two or more devices have to be used, they should be first merged with an insulator in between and then implemented.

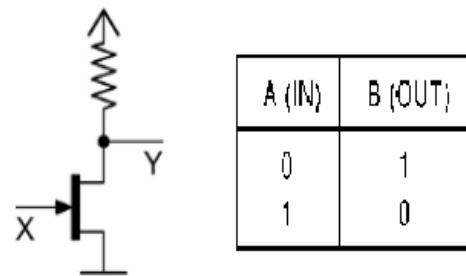


Fig 11: Merged devices in GUI of VTCAD

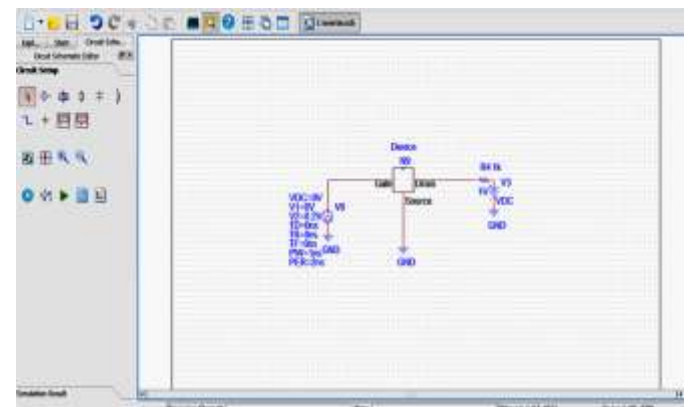
7. The desired circuit is implemented and tested.

Following the above procedure, three circuits, namely Inverter, Nand and Nor have been implemented in the circuit schematic of VTCAD considering HEMT to operate as a N-channel depletion mode device. The outputs for these circuits are observed by applying appropriate pulse inputs at the gate terminals and obtaining the desired response at the drain terminals.

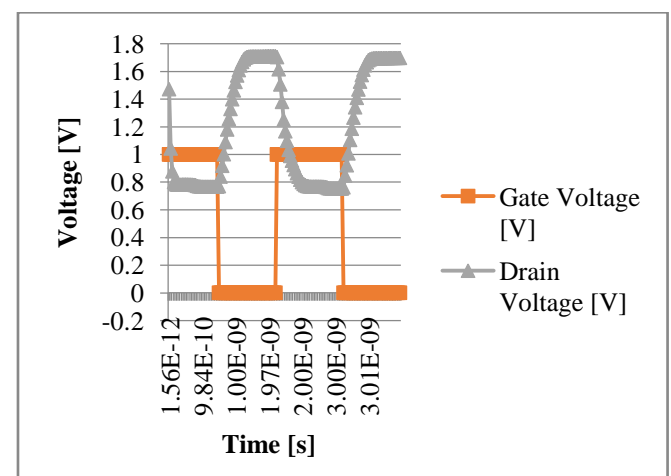
4.1 Inverter



(a)



(b)

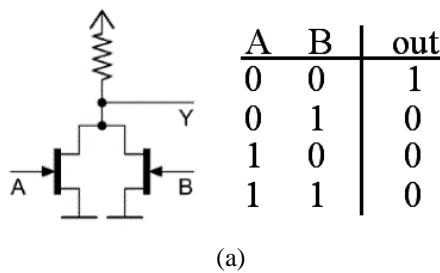


(c)

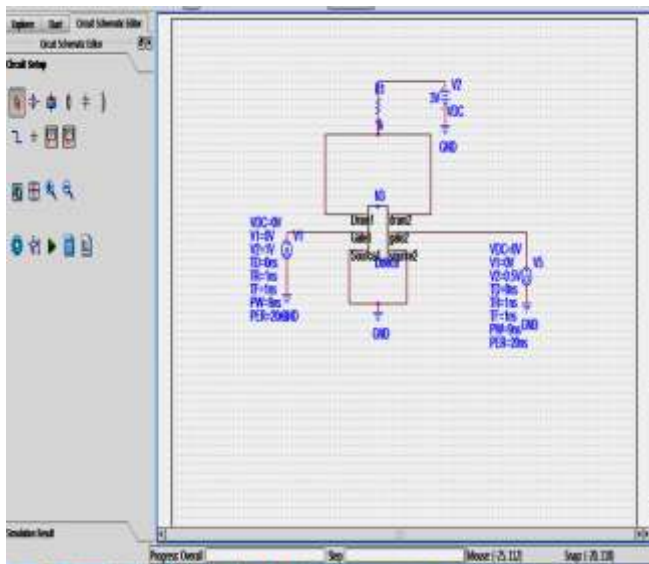
Fig 12: (a) Inverter Circuit schematic and Truth Table, (b) Inverter Circuit Implementation, (c) Output waveforms at 500 MHz

6. Further, this circuit symbol is used as the numerical device in circuit schematic of the software.

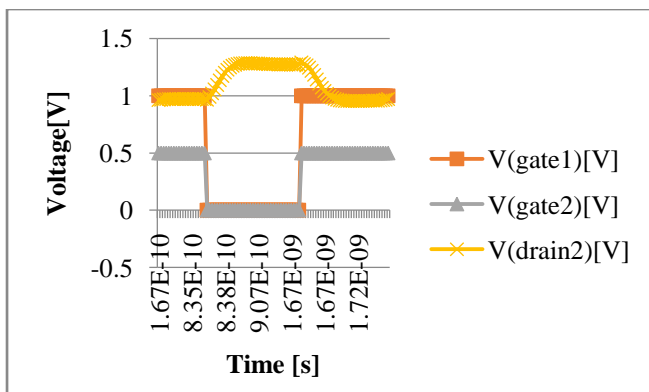
4.2 Nor Gate



(a)



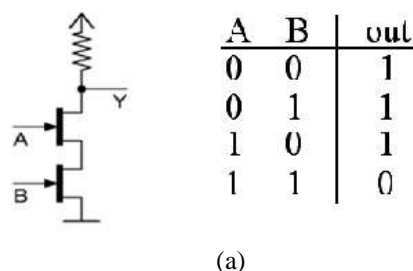
(b)



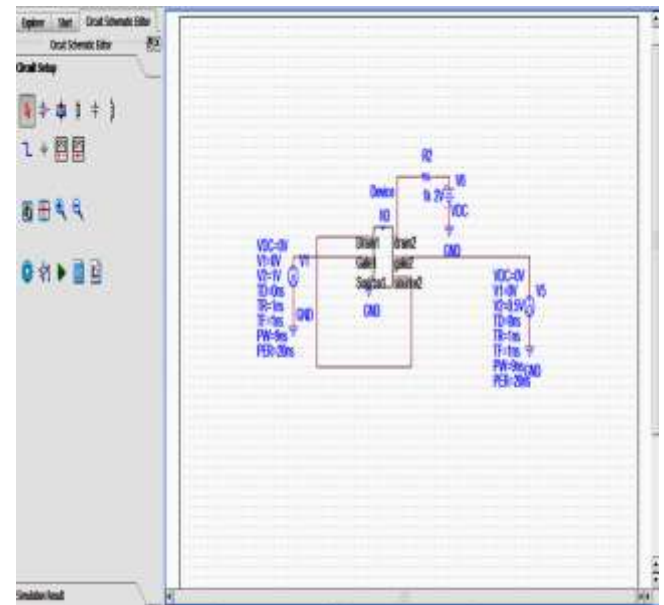
(c)

Fig 13: (a) Nor gate circuit schematic, (b) Nor gate circuit implementation, (c) Output waveforms at 500 MHz

4.3 Nand Gate

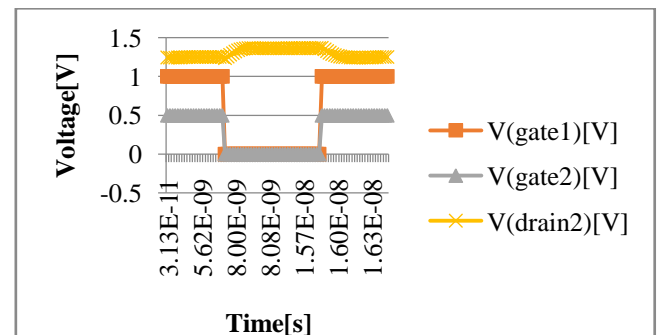


(a)



(b)

Nand gates and Nor gates being universal gates can be used for the implementation of any logic circuit in digital applications. The speed of communication is enhanced and also the noise is reduced. Fig. 15 and Fig. 16 show the implementation of the Nand and Nor gates using the developed HEMT structure.



(c)

Fig 14: (a) Nand gate circuit schematic, (b) Nand gate circuit implementation, (c) Output waveforms at 500 MHz

From Fig. 14(c), 15(c) and 16(c), it is observed that, when two or more devices are connected in series, or parallel the difference between level 0 and level 1 reduces which for a series combination is further reduced as compared to the parallel combination.

5. FUTURE SCOPE

We have found that the InGaAs HEMTs exhibit very promising logic characteristics. However, realizing the logic potential of InGaAs HEMTs will require a new device design with better electrostatic integrity. With further device optimization in the form of scaled insulator thickness, positive V_T and a self-aligned gate design, InGaAs HEMTs could well be the technology of choice when the CMOS roadmap comes to an end [7],[8].

6. CONCLUSION

In summary, we have developed a pseudomorphic HEMT structure for the implementation of logic gates which are the basic building blocks of the digital communication. The research supports the logic suitability of HEMT by using it in logic circuits. An attempt to take the digital communication to a complete new level in terms of speed and noise is made in this research. As we look forward, HEMTs are uniquely positioned to expand the reach of electronics in communications, signal processing, electrical power management and imaging.

REFERENCES

- [1] Fazal, Ali, *HEMTs and HBTs: Device, Fabrication and Circuit*, Artech House, pp. 1-6, 1991.
- [2] N.V. Uma Reddy, M.V. Chaitanya Kumar, "InGaAs/GaAs HEMT for High Frequency Applications", *International Journal of Soft Computing and Engineering (IJSCE)*, vol. 3, issue 1, Mar 2013.
- [3] Golio, John, *Microwave MESFETs and HEMTs*, Artech House, pp.24-70, 1991.
- [4] B.K.Mishra, Lochan Jolly, S.C.Patil, "In_{1-x}Ga_xAs a next generation material for photodetectors," *Cyber journal, JSAM*, pp.9-16, April 2011.
- [5] D.-H. Kim and J. A. del Alamo, "Beyond CMOS: Logic suitability of In_{0.7}Ga_{0.3}As HEMT," in *Proc. CS Mantech*, pp. 251-254, 2006.
- [6] B K Mishra, Lochan Jolly, Sonia Behra, "Submicron Model for illuminated gallium nitride HEMT", *International Conference and Workshop on Emerging Trends in Technology*, pp. 7-12, 2011.
- [7] Niamh Waldron, Dae-Hyun Kim, Jesús A. del Alamo, "A Self-Aligned InGaAs HEMT Architecture for Logic Applications", *IEEE Transactions on Electron Devices*, vol.57, no.1, pp.297-304, Jan 2010.
- [8] J.A. Del Alamo, "The High Electron Mobility Transistor at 30: Impressive Accomplishments and Exciting Prospects," *CS Mantech Proc.*, pp. 17-22, 2011.

BIOGRAPHIES



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