SCAN SEGMENTED STUMPS ARCHITECTURE FOR LOW POWER

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Abstract

Built-In-Self-Test is one of the technique for test power reduction that uses a scan segmented chains in a CUT the goal of this technique is to minimize the power consumption during test mode. One of the DFT technique is to design a circuit so that the circuit can test itself is called BIST which eliminates the need for external ATE. BIST architectures may results in increased test power and reduced fault coverage. This paper proposes a new test power reduction technique for BIST. The idea is to reduce the number of shift cycles required to test the CUT by dividing the scan chain into number of segments and only two segments will be triggered at a time. The BIST environment is implemented by taking S15850 benchmark circuit as CUT and it achieved 21% reduction in test power.

Keywords- *TPG, CUT, ORA, ROM, MISR, STUMPS*

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1. INTRODUCTION

In today's VLSI industry power reduction, area reduction and test time reduction are one of the main challenges. Because complexity of ICs had reached billions of transistors [1][2], this results in increase in complexity as well as functionality involved in testing process of a circuit. Because of this testing of today's ICs has become more time consuming, challenging and costlier. BIST is a one of the testing approach which reduces the complexity of VLSI circuit. The STUMPS based BIST is widely used architecture to test logic blocks of circuits. The basic BIST method consists of LFSR as a TPG, CUT, ORA and ROM used to store golden values. An external LFSR is used to load the data to the scan inputs of STUMPS BIST. In this paper we propose a new BIST architecture which reduces the number of test cycles and reduces the test power.

The rest of paper is divided as follows, STUMPS BIST architecture in section II. The proposed BIST architecture in Section III. In Section IV, setup and analysis of the BIST. Conclusion of paper is given Section V.

2. STUMPS BIST ARCHITECTURE

The basic architecture of STUMPS BIST [4][5] is shown in fig 1, this complete architecture works in two modes BIST mode and functional mode. These two modes are controlled by test mode signal. The basic architecture includes CUT, TPG, Compactor, ROM and ORA [6][7]. Here external LFSR is used to generate pseudo random test pattern as TPG. The output response of the CUT is compared with the golden values and result whether the chip good or bad.

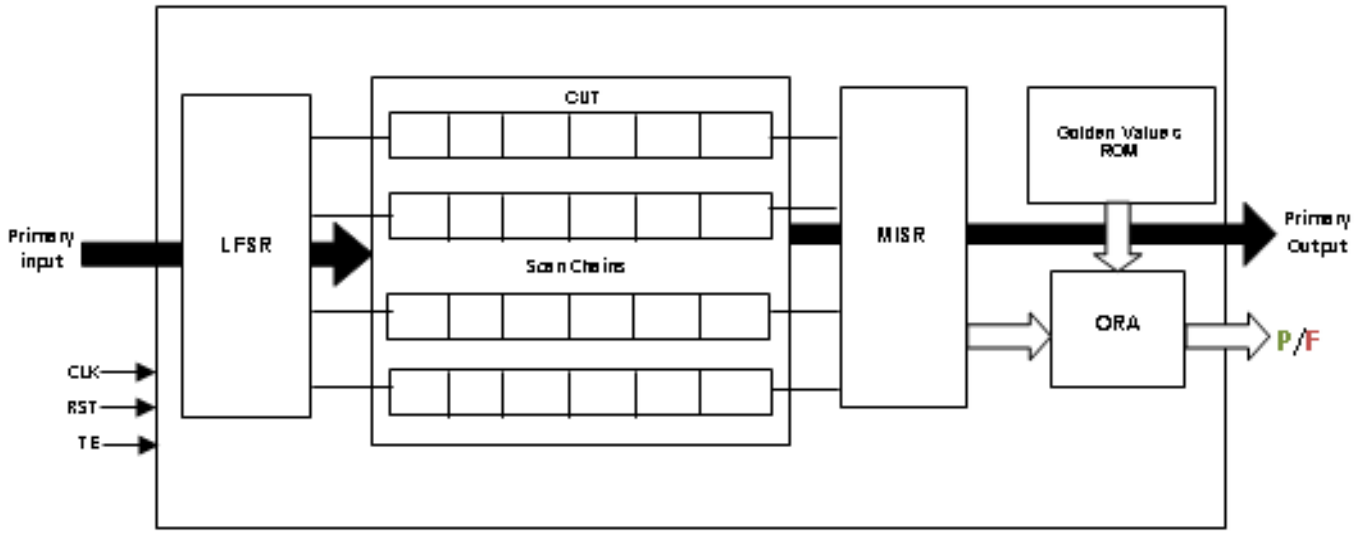

Fig 1. Basic STUMPS BIST

The steps involved in STUMPS BIST testing process are,

- The test patterns generated by LFSR are applied to the CUT, when test mode is enabled.
- The data is loaded to scan chains from LFSR by making scan enable signal high. The scan enable is made low for one clock cycle for capturing the combo logic response.
- The CUT response is given as input to compactor [8], to compact the CUT output response.
- The compacted test response are compared with golden response if both values matches means result will be logic '1' which indicates chip is good else result will be logic '0' indicate chip is bad.

In STUMPS BIST [4][8] the data is serially loaded into the scan chains so it requires n number of clock cycles where n is the number of flip flops present in longest scan chains. This results increase in the test power. The architecture proposed in section III reduces the test power in STUMPS by making the scan chain into number of segments.

3. PROPOSED BIST ARCHITECTURE

In basic STUMPS design, the test power and test time is depends on the length of scan chains and the number of shift cycles. In this section we propose a new scan segment based STUMPS architecture for low power where the total power of the architecture is reduced by using scan segment technique. In order to reduce test power for a STUMPS architecture we are dividing each scan chain into a number of segments and values are loading parallely into each segment. At a time maximum three scan segments can be triggered by using gated clock technique. The block diagram of single segmented scan chain is shown in Fig.2(a) and proposed parallel load STUMPS architecture is shown in Fig.2 (b).

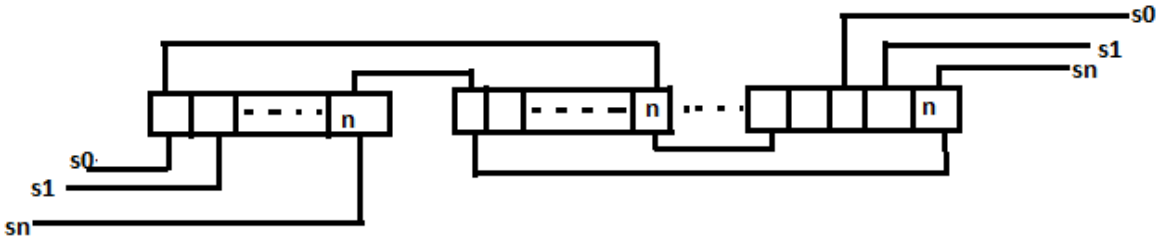

Fig.2(a) segmented scan chain

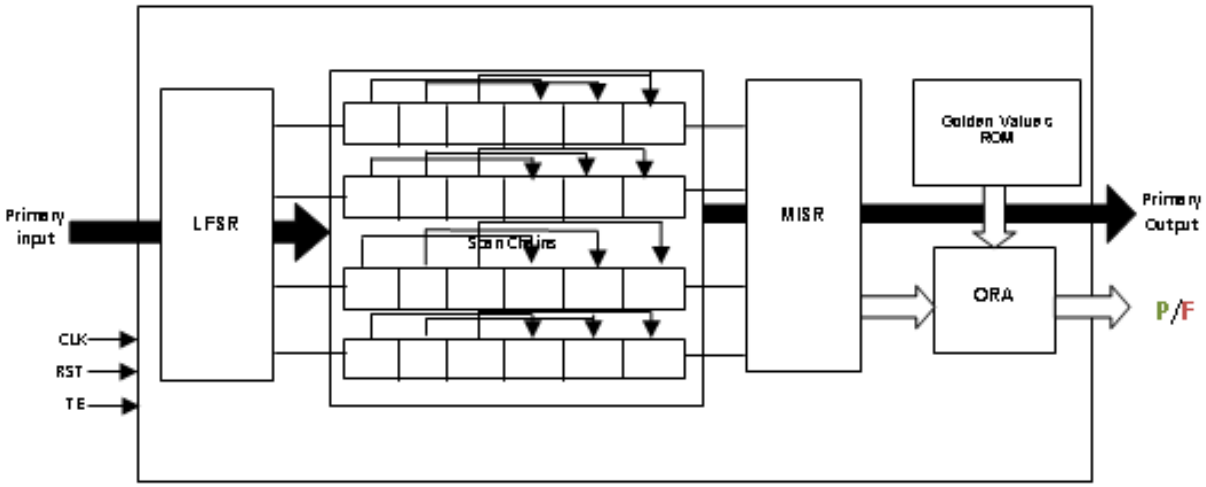

Fig.2(b) Parallel load STUMPS BIST

The steps involved in scan segment based STUMPS BIST are,

- S15850 benchmark is taken as a CUT. Scan chains are inserted into the CUT.
- Each scan chains are broken into number of segments
- Both flush test and logic test will be performed.
- Input values are loading parallel into the each 1st segment from an external LFSR. A parallel path is provided between adjacent segments.
- The design is simulated using NCSIM and Synthesized using Cadence RC.
- Using Cadence RC Power, Area, Test power and Timing reports are generated.

4. RESULTS AND ANALYSIS

4.1 Experimental Setup

The proposed architectures in section III and basic STUMPS architectures both are built for S15850 ISCAS standard benchmark circuit. For this benchmarks 8 scan chains are created with the available flops. For proposed architecture each scan chains are divided into number of segments by editing the netlist. An n-bit TPG is used to generate test patterns. Where n is number of flops present in first segment of each scan chains. Cadence RC is used for scan insertion, power estimation with 90nm TSMC technological library, TCF file is used for calculating test power.

4.2 Analysis

The experimental test power results for the proposed and basic STUMPS BIST is shown in table 1. From the table 1, the proposed BIST architecture reduces the test power of 21% for S15850 ISCAS benchmark circuit. In the proposed BIST architecture each scan chains are divided into number of segments. The data will be loaded paralley to these segments through LFSR. Load 1st segment of all scan chains for 1st clock cycle and remaining segments will be off. For 2nd clock cycle 1st and 2nd segments of all scan chains will be active, 2nd segment will take data parallely from the output of 1st segment. This will be continue for all segments and only maximum 3 segments will be on at a time. Here we are comparing test power for both architectures by taking 1000ns run time for tcf file.

Table 1. Test power results for basic BIST and proposed BIST architecture

Architectures	Test Power(nW)
Basic STUMPS BIST	1162313.926
Scan Segmented STUMPS BIST	919623.901

4.3 Simulation Results

The simulation waveform result of basic STUMPS BIST is shown in Fig.3 (a) and scan segmented STUMPS BIST is shown in Fig.3 (b).

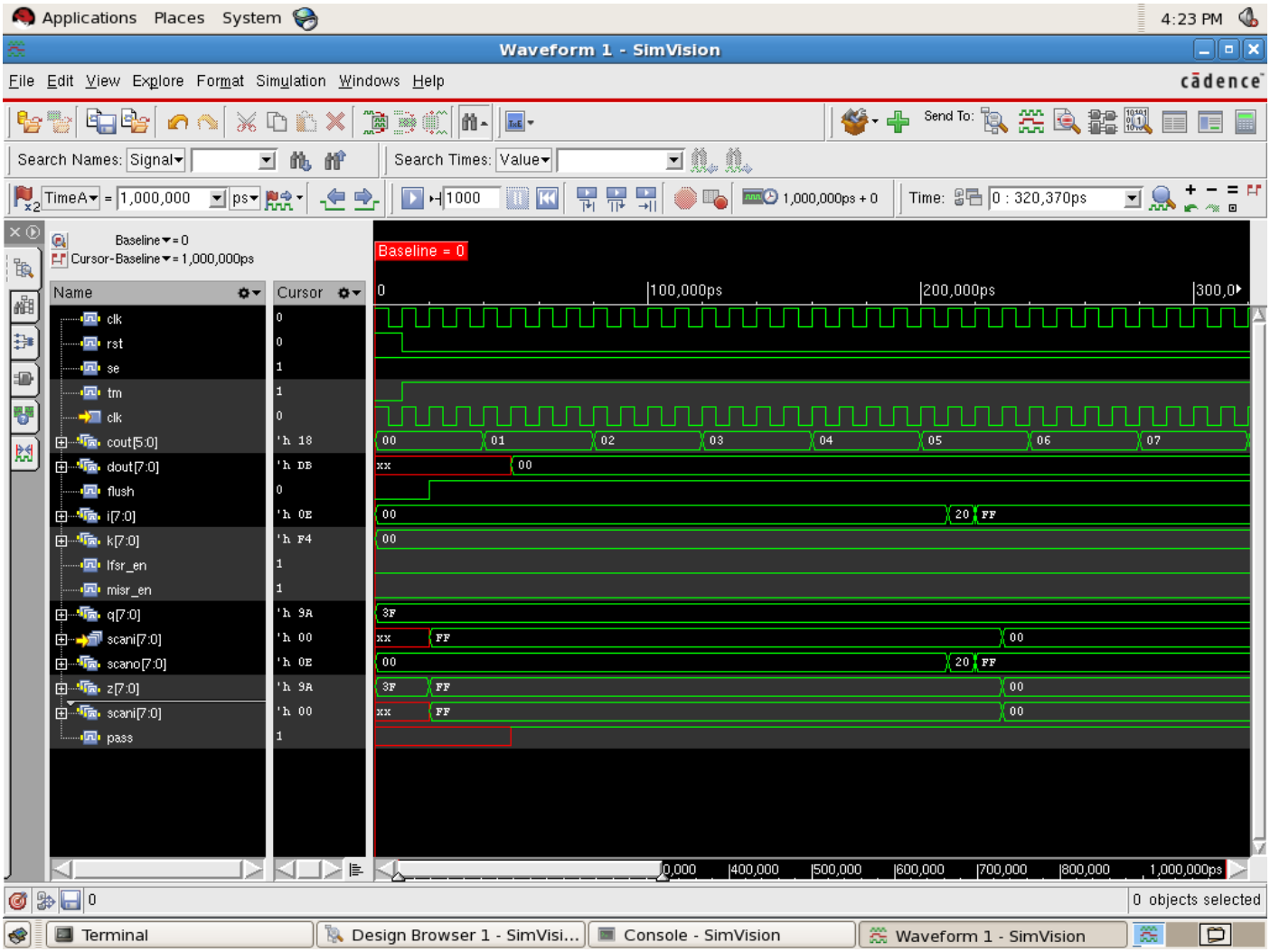

Fig.3(a)Simulation waveform for basic STUMPS

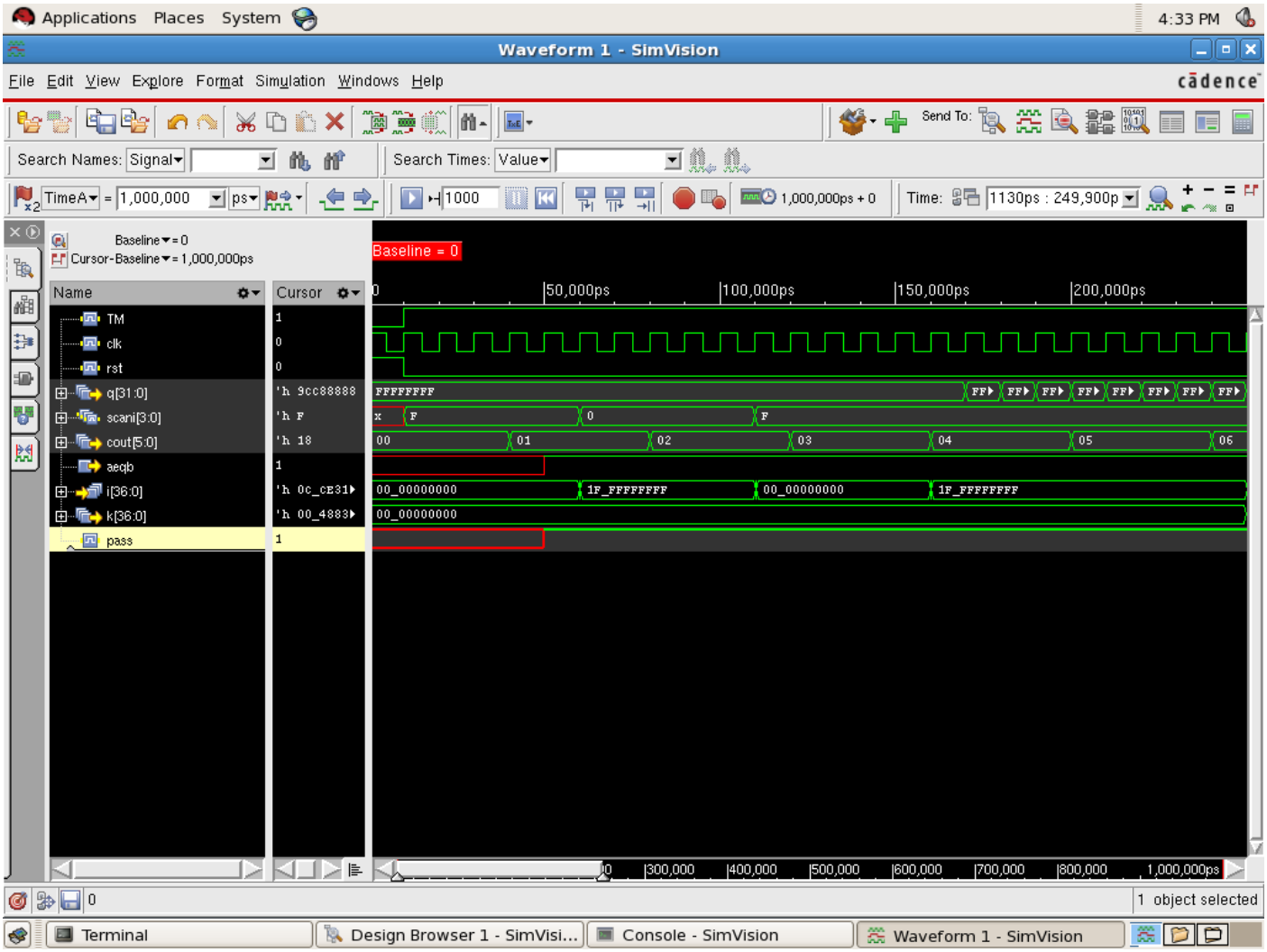

Fig.3(b)simulation waveform for scan segmented STUMPS BIST

5. CONCLUSION

The power reduction is one of the main challenge in VLSI domain. So it is very important to reduce the test power of the VLSI circuit. This paper proposes a new STUMPS BIST architecture which reduces the test power by making scan chain into a scan segmented chain. The 21% of the total power is reduced by scan segmented STUMPS architecture as compared to that of basic STUMPS BIST architecture.

REFERENCES

[1]. Gordan E Moore, "Cramming more components onto integrated circuits", Electronics, Volume 38, number 8, April 19, 1965.

[2]. "International Technology Road map for Semiconductors, process integration, devices and structures", 2013 Edition.

[3]. Ron press, Vidya Neerkundar., "Improve logic test with a hybrid ATPG/BIST solution", www.mentor.com, Mentor graphics, September 2013.

[4]. P. H. Bardell and W. H. McAnney, Self-testing of multi-chip logic modules, in Proc. IEEE Int. Test Conf., pp. 200 – 204, October 1982.

[5]. Nayana M, G harish and Siva Yellampalli, "Comparative analysis of BIST architectures", Proc. 2nd International Conference on Advanced Trends in VLSI and Signal Processing-2014 KSIT,Bangalore.

[6]. Nur A. Touba, "Survey of test vector compression techniques", IEEE Design & test of computers, pp 294-303 August 2006.

[7]. Ravi kiran N, G Harish, "Comparative analysis of different compaction techniques in BIST" proceedings IEEE national conference on electrical and electronics engg.NCEE-2014,HKBK college of engg., Pp 64, 5 June 2014

[8]. Stroud, E.C., "A Designer's Guide to Built-In Self-Test". ISBN 21-4020-7050-0., Kluwer Academic Publishers, Boston, MA, 313, 2002