HIERARCHICAL SCAN AND ATPG FOR TWO STAGE WRAPPER

Bhavana.N[1]

[1]*VLSI Design and Embedded Systems, VTU Extension Centre UTL Technologies Ltd, Bangalore*

Abstract

There are multiple scenarios where at-speed coverage over core boundaries is difficult. The idea is to resolve this problem using two stage wrapper. Generally single stage wrapper is used in the present design techniques, and is used in industries. Here two stage wrapper is used in which test coverage has been increased. Additional scan compression architecture is introduced to reduce the pattern count and test time.

Keywords *— Identifying Input and Output Wrapper Cells, Hierarchical Scan Insertion, Addition of Compression Logic, Increased Coverage.*

----------***----------

1. INTRODUCTION

According to Moore's Law, the complexity of the design is increasing [1]. The introduction of ICs, commonly referred to as simply SoCs, was accompanied by the requirement to test such devices. As the size of transistors becoming lesser, process variations like etching, lithography are becoming critical. These process variations lead to malfunction of the designs. The ever increasing complexity of digital designs resulted in devices with hundreds of millions of transistors leads to many new testing challenges.

The major scope of the project is to increase the fault coverage by the dedicated or shared wrapper cells. These wrapper cells are stitched into input and wrapper chains for better fault coverage and to isolate it from other blocks. The scope of the project is to do the comparative analysis of different stage of wrapper inserted architecture, that is, simple scan inserted architecture, single stage wrapper architecture, and two stage wrapper architecture. Also all three designs are compression inserted designs.

Context of this design includes development of generic script to identify input and output wrapper cells for all cores, hierarchical scan insertion for all cores and top module, addition of compression logic for each core, ATPG for all cores and top module in different modes hierarchical scan insertion of two stage wrapper for all cores, and ATPG for all cores and top module after second stage wrapper in different modes [2].

2. DESIGN METHODOLOGY

For Hierarchical Scan Insertion there is a need to isolate blocks from one another. All the inputs and outputs at block level should be registered. Signals like clocks, resets and static test control signals are not registered but are controlled from chip level pins. To isolate blocks from one another, there is a need to add the wrapper chains, which need to be identified first and insert the wrapper cells. This identification and insertion of wrapper cells is done be writing the TCL script. First the shared wrapper cells have been identified by tracing the logic from both input and output ports. Also tracing back the logic to identify which other flops are driving the same flop. Those flops are also added to shared wrapper chain as shown in Fig. 1.

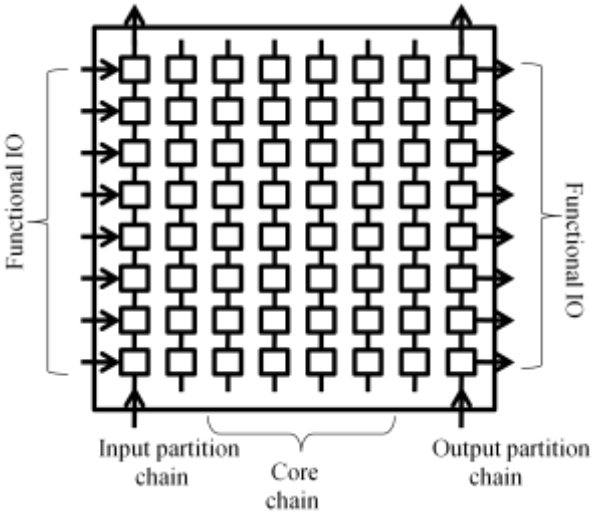


Fig. 1 Block level scan insertion

For second stage wrapper chains, same procedure is continued by tracing the logic from those identified wrapper cells. If the input or output port is driving flops more than threshold, then the dedicated wrapper cell is inserted at that port. All first stage and second stage wrapper chains are stitched. Remaining flops are stitched as core chains. Hence all the inputs and outputs are controllable and observable of the design on top module. After stitching scan chains, the fault coverage is obtained by running ATPG, instantiating four blocks at top level module. This top module is tested for different modes of operation like INTEST and EXTEST. This can be achieved by using JTAG [3] control logic as shown in Fig. 2.

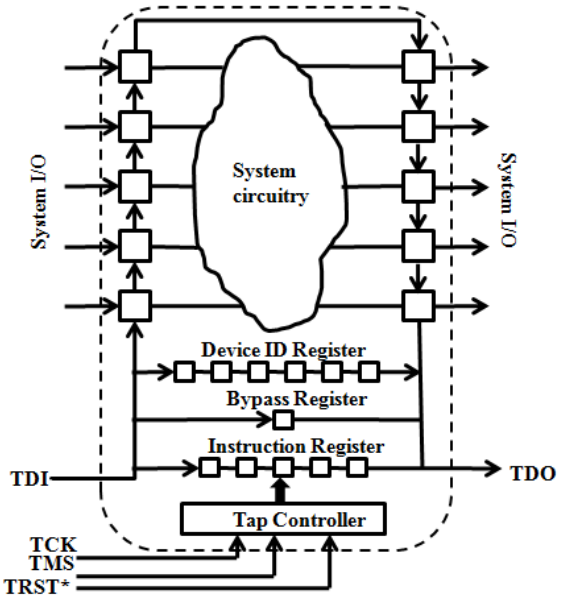


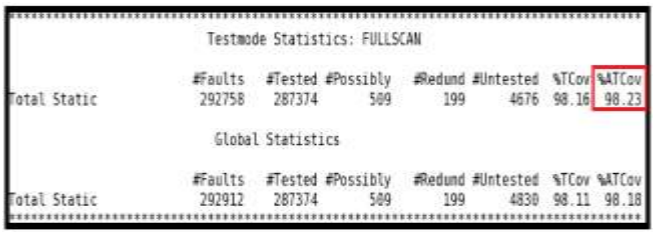
Fig. 2 JTAG architecture

3. DESIGN VALIDATION

To evaluate the hierarchical DFT architectures, hierarchical scan chains with two stage wrapper are inserted for S15850, S35932 and S38584 ISCAS89 standard benchmark circuits. For all the benchmarks 5 scan chains are created with the available flops. For calculating the fault coverage, six test sequences are generated and applied to all the architectures. The ISCAS benchmark circuits S15850 consists of 165 registers, S35932 consists of 1728 registers and S38584 consists of 1178 registers. Obtained fault coverage for each design. Thus generalized script has been made and is used for ahb2axi benchmark, which is hierarchical design.

4. SUMMARY OF DESIGN RESULTS

The obtained result shown in Fig. 3 is for ahb2axi benchmark which is having ten thousand plus flops and two clock domains. In bypass mode 98.23% of test coverage is achieved.



Testmode Statistics: FULLSCAN

	#Faults	#Tested	#Possibly	#Redund	#Untested	%TCov	%ATCov
Total Static	292758	287374	509	199	4676	98.16	98.23

Global Statistics

	#Faults	#Tested	#Possibly	#Redund	#Untested	%TCov	%ATCov
Total Static	292912	287374	509	199	4830	98.11	98.18

Fig. 3 Test results for Normal Scan Bypass mode

With compression mode 98.27% of test coverage is obtained as shown in Fig. 4 for compression ratio 8. Compression has been analyzed for values 4, 5, 6, 7, 8 and 9. The best obtained test coverage has been chosen as the compression ratio, that is ratio 8. Where there are eight top level scan chains and are subdivided into many number of scan slices with the ratio 8. XOR compressor and XOR decompressor has been used for the compression architecture.

Testmode Statistics: FULLSCAN

	#Faults	#Tested	#Possibly	#Redund	#Untested	%TCov	%ATCov
Total Static	297470	292051	488	286	4645	98.18	98.27

Global Statistics

	#Faults	#Tested	#Possibly	#Redund	#Untested	%TCov	%ATCov
Total Static	297624	292051	488	286	4799	98.13	98.22

Fig. 4 Test results for Normal Scan Compression mode

The obtained result for single stage wrapper as shown in Fig. 5 is for same ahb2axi benchmark which is having ten thousand plus flops and two clock domains. In bypass mode 98.24% of test coverage is achieved. Here also there are eight top level scan chains, where one is input wrapper chain, one is output wrapper chain and remaining 6 chains are core scan chains.

Testmode Statistics: FULLSCAN

	#Faults	#Tested	#Possibly	#Redund	#Untested	%TCov	%ATCov
Total Static	295772	290372	478	197	4725	98.17	98.24

Global Statistics

	#Faults	#Tested	#Possibly	#Redund	#Untested	%TCov	%ATCov
Total Static	295926	290372	478	197	4879	98.12	98.19

Fig. 5 Test results for first stage wrapper Bypass mode

With compression mode for single stage wrapper, 98.28% of test coverage is obtained as shown in Fig. 6 for compression ratio 8. To compare between the normal scan operation, single stage wrapper and two stage wrapper architecture, same compression ratio 8 is considered. Where there are eight top level scan chains where two are wrapper chains and six are core chains and each chain is subdivided into many number of scan slices with the ratio 8. XOR compressor and XOR decompressor has been used for the compression architecture [6] [7].

Testmode Statistics: FULLSCAN

	#Faults	#Tested	#Possibly	#Redund	#Untested	%TCov	%ATCov
Total Static	299598	294197	472	265	4664	98.20	98.28

Global Statistics

	#Faults	#Tested	#Possibly	#Redund	#Untested	%TCov	%ATCov
Total Static	299752	294197	472	265	4818	98.15	98.23

Fig. 6 Test results for first stage wrapper Compression mode

The obtained result for two stage wrappers as shown in Fig. 7 is for same ahb2axi benchmark. In bypass mode 98.24% of test coverage is achieved. Here also there are eight top level scan chains, where two input wrapper chains, two output wrapper chains and remaining four chains are core scan chains.

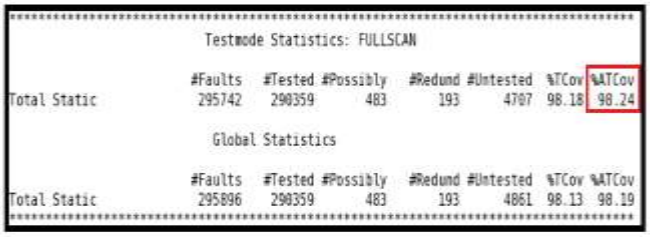


Fig. 7 Test results for two stage wrapper Bypass mode

With compression mode for two stage wrappers, 98.28% of test coverage is obtained as shown in Fig. 8 for compression ratio 8. There are eight top level scan chains where four are wrapper chains and four are core chains and each chain is subdivided into many number of scan slices with the ratio 8. XOR compressor and XOR decompressor has been used for the compression architecture [8].

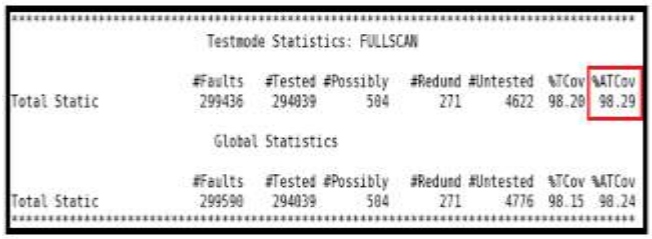


Fig. 8 Test results for two stage wrapper Compression mode

Fig. 9 represents the normal scan inserted design for hierarchical ahb2axi benchmark, which consists of sub-blocks ashl, axmrd and fc as shown.

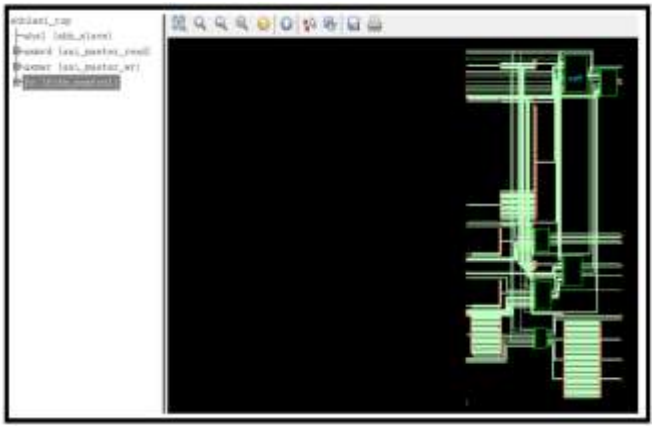


Fig. 9 ahb2axi hierarchical architecture for normal scan inserted design

Two stage wrapper inserted design with compression architecture is then instantiated four times at the top level and are connected to one another. Each ahb2axi design is considered as individual block. Hence there are four blocks at the top module. JTAG is also instantiated parallel to this design at the top module to control these blocks and to test the design in different modes of operation like EXTEST and INTEST. Using JTAG, all the blocks can be tested either individually or complete design is tested at once. EXTEST mode adds the advantage to increase the test coverage by testing the glue logic in between the blocks. For this a JTAG is designed and is verified using NCsim simulator.

5. CONCLUSION

In this work, the increase in fault coverage has been shown using ahb2axi hierarchical benchmark design which includes ten thousand plus flops. The additional advantage is the test time reduction because of addition of compression logic at the design. One disadvantage of this work is increase in power due to dedicated wrapper cells and some additional logic, which may also, leads to small increase area. Individual blocks can be tested by adding JTAG at the top level module. An individual block has been tested, which is called as INTEST. The future scope of the project is test the top module in EXTEST mode, which is used to test the glue logic at the top module, which may add advantage of increasing fault coverage.

ACKNOWLEDGMENT

The satisfaction of successful completion of work would be incomplete without expressing sincere thanks to the people, who helped in making it possible, though words are not enough to express the sense of gratitude towards everyone who helped directly or indirectly.

The author would like to take this opportunity to express deep sense of gratitude to Dr. Siva Yellampalli, Mr. Ashish Kothari, Mr. Lingraj Jeevangi, Mr. G. Harish and Mrs. Nayana. M.

REFERENCES

[1] Gordan E Moore, “Cramming more components onto integrated circuits”, Electronics, Volume 38, Number 8, April 19, 1965.

[2] Jeff Remmers, Moe Villalba, “Hierarchical DFT Methodology – A Case Study”, ITC International Test Conference, paper 30.2, pp 847-856.

[3] Kenneth P. Parker, *THE BOUNDARY-SCAN HANDBOOK SECOND EDITION Analog and Digital*, 2nd ed., Kluwer academic publishers New York, Boston, Dordrecht, London, Moscow-1998.

[4] P. Goel, An implicit enumeration algorithm to generate tests for combinational logic circuits, IEEE Transactions on Computer Aided Design, Volume 30, Number 3, pp 215–222, 1981.

[5] H. Fujiwara and T. Shimono, “On the Acceleration of Test Generation Algorithms,” IEEE Transactions on Computers, volume 32, pp. 1137–1144, December 1983.

[6] M.Abramovici, M.A Breuer and A.D.Friedman, “Digital System Testing & Testable Designs”, IEEE press, Piscataway, NJ, 1994.

[7] User guide “Design For Test in Encounter RTL Compiler”.

[8] K. Chakravadhanula, V. Chickermane, D. Pearl, A. Garg, R. Khurana, S. Mukherjee, P. Nagaraj, “SmartScan - Hierarchical Test Compression for Pin-limited Low Power Designs”, International Test Conference, Paper 4.2, 2013 IEEE.