MICROSTRUCTURE ANALYSIS OF CDTE/CDS THIN-FILM SOLAR CELLS FOR OPTIMIZATION OF DEVICES FABRICATED AT LOW TEMPERATURE WITH PULSED LASER DEPOSITION

Paul Harrison[1], Jake Meeth[2],Guanggen Zeng[3], Judy Wu[4]

[1,2,3,4]Department of Physics and Astronomy, University of Kansas, Lawrence, KS, 66046, USA
[2]Electrical Engineering Division, Department of Engineering, University of Cambridge, Cambridge, CB3 OFA,UK
[3]College of Materials Science and Engineering, Sichuan University, Chengdu 610064, China

Abstract

Low temperature fabrication of CdTe (1.25 μm)/CdS (120 nm) thinfilm solar cells was explored using in situ pulsed laser deposition (PLD) in order to control the CdTe grain morphology, crystallinity, and CdS/CdTe interface, which have proven to be crucial in CdTe/CdS solar cell performance. A comparative study was carried out on solar cells fabricated using PLD with the CdTe layer either grown directly at 400°C or at200°C followed with in situ annealing at 400°C for 5-40 minutes in 20 Torr Ar. The post annealed CdTe films exhibit better crystalline characteristics confirmed by optical transmittance and atomic force microscopy as well as improved CdTe/CdS p-n junction, which results in increasingly higher open circuit voltage and fill factor with increasing anneal times up to 20 minutes. Quantum efficiency measurements revealed that the post-annealed cells have more efficient electron collection, particularly below the CdS band edge, and a correlation is drawn between PLD annealing time and $CdCl_2$ annealing time to optimize device efficiency. The results suggest that the in situ post PLD annealing process developed in this work is advantageous because of much improved crystallinity of CdS and CdTe, a considerably lower deposition thermal budget for better control of the CdS and CdTe interface, plus flexibility for in situ materials mixing for energy band gap engineering.

Keywords: *CdTe, Thin Film, Solar Cells, Pulsed Laser Deposition*

----------***----------

1. INTRODUCTION

CdTe has long been researched for solar cell applications due to its optimal band gap of ~1.5 eV (single p-n) and high absorption coefficient approaching 10^5/cm, making it an ideal material for thinfilm (thickness on the order of 1 μm or less) solar cells.[1-3]This has prompted extensive research during the past two decades and exciting progress has been made with power conversion efficiencies up to 20% recently being achieved in thickfilm (thickness in the range of 3-8 μm) CdTe solar cells by constantly pushing up the key parameters of short circuit current J_{SC} (>25 mA/cm^2), open circuit voltage V_{OC} (>850 mV) and the fill factor FF (>75%).[4-8]The difficulties in further enhancing the performance of CdTe based solar cells is intimately associated to their polycrystalline structure that results in electron/hole recombination mechanisms.[8]Grain boundaries (GBs) within the polycrystalline CdTe films are sites for recombination and finding a way around this has posed certain difficulties.[5, 9-11]Typical grain size for thickfilm CdTe is on the order of microns. The larger the grain size becomes the lower the chance of charge carrier recombination at these GBs.

Thin film (thickness ~ 1 μm) CdTe solar cells could have much reduced recombination due to the reduced charge travel distance (thickness) in addition to the benefits of its optimal band gap and high absorption coefficient. However, the optimal grain size for thick film CdTe cells is unrealistic in thinfilm CdTe solar cells as it is comparable to the CdTe layer thickness and GBs can create a direct path for pinholes, or shorts. This issue may be resolved ultimately in epitaxial solar cells, but the large 10% lattice mismatch between CdS and CdTe can lead to highly strained interface between them, which prompts formation of defects as traps for charge carriers.[12] Before this issue is fully addressed, the grain size in polycrystalline CdTe/CdS thin film solar cells will have to compromise to much smaller than the CdTe thickness to avoid shorting but large enough to minimize the amount of GBs and hence charge recombination.

Pulsed laser deposition (PLD) is advantageous to *in situ* fabrication of multilayer structured thinfilm devices, including CdTe/CdS thin film solar cells, which minimizes complications on the interface between different layers. In a recent work, we have demonstrated the feasibility ofPLD deposition of CdS/CdTe thin films solar cells ata temperature of 500ºC for CdTe PLD fabrication.[13, 14]Power conversion efficiency up to 5% has been demonstrated. However, the uniformity of such devices was poor, most probably due to the high substrate temperature (T_s),exceeding500 °C, compared to other typical methods for depositing CdTe, such as close-space sublimation.[10, 15] A considerably lower deposition temperature is possible in PLD due to the extra energy supplied by the laser

plume.[15-17]In fact, the low temperature fabrication in PLD growth is preferred because of increased growth rate due to higher sticking coefficient at lower temperatures.[18]An additional benefit of low temperature growth is in reduced diffusion between CdTe and other materials such as ZnTe that has a low thermal budget of around 400°C[19], which may be considered inCdTe-based cells to make more complex cell structures for enhanced optoelectronic properties. Motivated by this, a systematic study has been carried out on solar cells fabricated with CdTe growth temperatures of 200 ºC, 400 ºC, and 200ºC with a 400ºC anneal in 20 Torr Ar for 5, 10, 20, and 40 minutes. Improved uniformity was observed in the annealed cells and higher power conversion efficiencies were obtained with increasing anneal time (up to 20 minutes). In particular, these cells out-perform those made with CdTe grown directly at 400ºC. The increase in performance with longer anneal time is due to increases in all three key parameters, J_{SC}, V_{OC}, and FF, with the biggest contribution coming from the increases in FF. In addition, for longer post anneal times in the PLD chamber, longer $CdCl_2$ anneal times are necessary to reach optimum performance.

2. MATERIALS AND METHODS

The PLD fabrication process used a 248 nm excimer laser for target ablation. For this experiment the laser beam first passed through a neutral density filter to reduce the energy density and then was directed into the PLD vacuum chamber at ~ 45 degree with respect to the normal of the targets. The energy densities of roughly 0.7 J/cm^{2}and 0.6 J/cm^{2}at the target surface were used for depositing CdTe and CdS, respectively.[13, 20, 21] A scanning stage controlled by computer was used to move the substrate in the plane perpendicular to the plume direction for large area uniformity. The sample to target distance was 5.5 cm.The base pressure was 5.0x10^{-6} Torr. PLD of CdS/CdTe hetero structure was made at 1.5 mTorr Ar, which was found critical to reduce material deposition on the laser entry window.

The CdS was deposited at 200ºC in 1.5 mTorr Aron fluorine-doped tin oxide (FTO), TEC 15 soda lime glass. The scanning stage was used to move the substrate 1.5 cm in a direction perpendicular to the plume to make the CdS window layer more uniform. The CdS layer thickness is 105 nm on the edge to 130 nm at the center and the thickness variation could be controlled through the scanning parameters. Three CdTe growth conditions were compared in this work:1) PLD of CdTe at 200ºC followed with an *in situ* post anneal at 400ºC with various periods of 5, 10, 20, and 40 minutes, 2) direct PLD growth of CdTe at200ºC, and 3) direct PLD growth of CdTe at 400 ºC. In the former, 200 ºC was selected considering the suitable sticking coefficient and thus higher PLD CdTe deposition rate as compared to higher temperatures.[19]400 ºC seems to be optimal in the range of 350 ºC -500 ºCin a preliminary test considering the CdTe crystallinity, morphology, and the solar cell performance. In particular, it is compatible to the $CdCl_2$ annealing (360ºC for 15 minutes in mixed (4:1) Ar/O_2 gases of atmospheric pressure) applied after the PLD fabrication for improvement of the CdTe grain connectivity and charge carrier doping.[10, 13, 14, 20-22] Br:CH_4O etching (0.2mL:40mL) for four seconds was employed to create a Te rich surface for better Ohmic back contact of(HgTe:Cu):graphite paste (253:1):2.5. To further reduce the contact resistance, the cells were annealed in a furnace at280ºC for 30 minutes in Ar gas. Liquid silver was applied on top of the back contacts and baked at 150ºC for 1 hour in air. The typical cell size was 2.5 mm^2.

Thickness measurements were performed with a KLA-Tencor P-16 profiler. Transmittance plots were obtained for all films using a Newport monochromator and optical power meter to determine their optical properties and to make band gap approximations. The Newport monochromator and a CHI 660D electrochemical workstation were used for external quantum efficiency (EQE) measurements. Atomic force microscopy (AFM) and Raman spectroscopy were performed using a WiTec Alpha 300 confocal MicroRaman system to obtain surface roughness and phase orientation for the different growth and annealing conditions. I-V measurements were taken with a CHI 660D electrochemical workstation while cells were illuminated with a Newport solar simulator under 1.5AM one sun illumination.

3. RESULTS AND DISCUSSION

Fig. 1 shows plots of the transmittance versus wavelength and absorption versus photon energy for CdTe films grown at 200ºC, 400ºC, and 200ºC with a 400ºC anneal for 5 minutes deposited on the FTO substrates. The absorption versus photon energy plots were made using equations (1) and (2) where α is the absorption coefficient, *d* is the film thickness, and I/I_o is the transmittance and can be used to approximate the band gapE_g for direct band gap semiconductors such as CdTe. The extracted E_g values for a set of selected samples are compared in Table 1. With the exception of the 200 ºC direct grown CdTe, all other films have a comparable band gap in the range 1.48-1.50 eV. The film grown at 200 ºC without post anneal has a broader absorption edge, that starts around 815 nm, than the CdTe films either grown at 400 ºC or at 200 ºC followed with *in situ* post annealing. The comparable sharp absorption edges at almost identical wavelengths for the latter two conditions means that polycrystalline CdTe could be obtained from either direct PLD growth at 400 ºC or *in situ* post annealing at the same temperature. With longer post anneal times there was little difference seen in the band gaps of the CdTe films, but there was a clear correlation between longer anneal times and sharper absorption edges which is indicative of better crystallinity in the CdTe films. The improved crystallinity, in addition with the higher growth rate and flexibility in controlling the optimal thermal budget, makes the thermal post annealing used in this work advantageous to PLD *in situ* grown CdS/CdTe solar cells. The result in this work agrees well with previous work which showed that PLD grown CdTe films begin to exhibit polycrystalline characteristics with a cubic structure, confirmed with XRD, when the substrate temperature is above 200 °C.[14, 21]

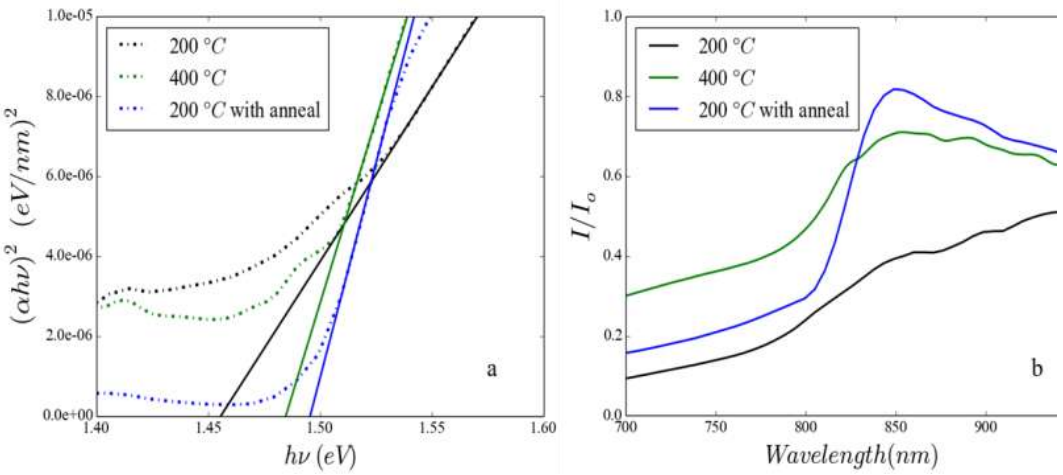

Fig 1: Absorption versus photon energy (a) with linear fits (solid lines) and transmittance (b) for CdTe films grown at 3 different PLD growth conditions of 200ºC, 200ºC with a 400ºC post anneal for 5 minutes, and 400ºC.

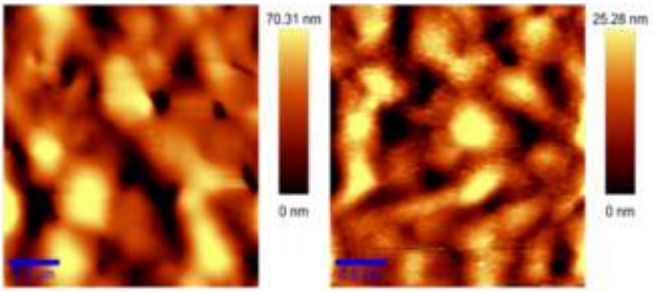

Fig 2: AFM measurements of (left) CdTe fabricated at 200 ºC with a 20 minute post-anneal and (right) 400 ºC direct growth. Both films have undergone the $CdCl_2$ treatment and have average surface roughness of 22.1 nm and 16.3 nm, respectively.

$$(\alpha h\nu)^2 = \left[\left(\frac{1240}{\lambda}\right)\left(-\frac{1}{d}\right)\ln\left(\frac{I}{I_o}\right)\right]^2 \quad (1)$$

$$h\nu = \frac{1240}{\lambda} \quad (2)$$

A deeper understanding of the differences between PLD CdTe thin films processed at the higher temperature conditions are provided by AFM analysis of the film surface morphology.The AFM analysis showed that both the direct grown CdTe at 400ºC and the post annealed CdTe had a surface roughness more than three times that of the CdTe grown directly at 200ºC.AFM images taken on the 20 minute post annealed and the 400 ºC direct grown CdTe are compared in Fig. 2. The post annealed CdTe has considerably larger grain sizes around 400 nm and consequently larger surface roughness of about 35% then in the case of CdTe grown directly at 400 ºC. The enhanced grain growth is favorable especially when it is controllable to yield grain dimension less than the CdTe thickness. An additional benefit of the post-annealing is in shorter high temperature (400ºC in this work) exposure time for the CdS window layer. In the directly grown case, the exposure time was 40 minutes, while in the annealed one it was reduced to~20 minutes, which has been found to be important in controlling the CdS/CdTe interface quality as we will discuss later in this paper.

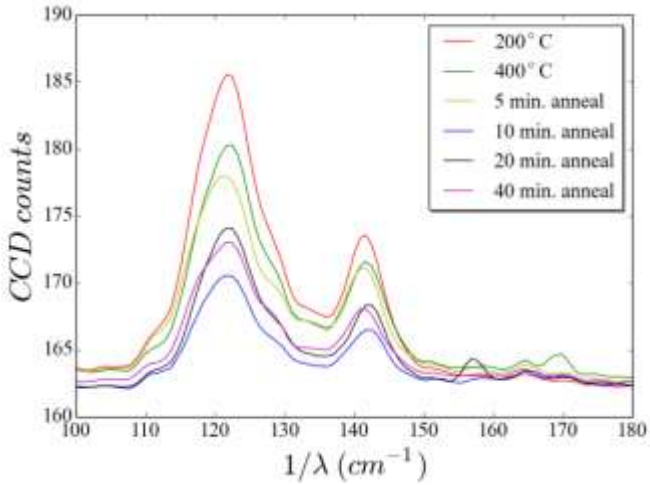

Fig 3: Raman shift for CdTe grown directly at 200ºC, 400ºC, and at 200ºC with 400ºC anneal for 5, 10, 20, and 40 minutes

Raman spectroscopy was performed on all of the CdTe samples to examine differences in their crystallinity and the result is compared in Fig. 3.Two distinct peaks can be seen on all spectra at 120 $cm^{-1}$and 140 $cm^{-1}$and are known to be the mode due to A_1 phonon symmetry for Te and the transverse optical (TO) mode for CdTe, respectively.[23] There are additional peaks observable at approximately 158 cm^{-1} and 169 cm^{-1}. These can be attributed to the surface optical (SO) and longitudinal optical (LO) modes, respectively, which have been reported previously.[23-25] The selection rules are that for (110) CdTe the TO mode is allowed, but the LO is not.[23, 26]CdTe with (111) orientation can have both the TO and LO mode. The post annealed CdTe appears to have a small peak at the 169 cm^{-1} shift, but this peak is notprominent as in the CdTe grown directly at 400 ºC. Thus, the CdTe grown directly at 400ºC has a (111) phase and all the post annealed films have a predominantly (110) phase with a possible small mixture of the (111) phase in the polycrystalline structure. A reduction in the 120 cm^{-1}peak as well as the ratio between the 120 $cm^{-1}$and the 140 cm^{-1} peaks was observed with increasing post anneal time. This indicates the amount of unreacted Te is

reduced with longer anneal time and is lower for post annealed CdTe than for the direct grown CdTe. The reduction in Te may occur because it is a more volatile species than the Cd, resulting in preferential loss of Te during the PLD fabrication. The high Raman intensity of the Te peak on the 200ºC direct grown CdTe suggests higher temperatures, exceeding 200 ºC, is necessary to form fully reacted CdTe crystalline phase. In fact, direct PLD deposition or post annealing at up to ~350 ºC was found inadequate to form high quality crystalline CdTe. The presence of unreacted Te (or Cd) will affect not only the doping of the material but also its stability.[27] Te rich CdTe is an n-type semiconductor and would be harmful for cell performance since the $CdCl_2$heat treatment dopes the CdTe p-type. Devices with large amounts of Te would then be expected to have poor performance due to the lack of doping in the CdTe.

Table 1: Summary of solar cell performance and band gap approximations for seven different PLD growth conditions

Growth Condition	CdTe E_g (eV)	J_{SC} (mA/cm^2)	V_{OC} (mV)	FF (%)	Eff. (%)
200 ºC	1.45	9.3	194	26.2	0.47
400 ºC	1.48	18.8	675	48.2	6.08
5 min. anneal	1.49	19.1	671	43.1	5.53
10 min. anneal	1.50	20.6	680	45.2	6.33
20 min. anneal	1.48	20.8	698	50.3	7.31
40 min. anneal	1.49	18.5	708	40.8	5.36

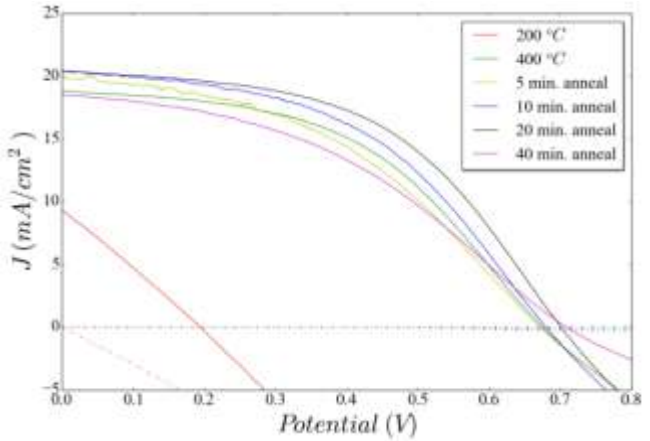

Fig 4: J-V plots of cells under one Sun illumination (solid lines) and in the dark (dashed lines) with CdTe fabricated at the six different PLD growth conditions of Table 1.

The J-V curves taken under AM1.5 illumination and in the dark for the samples fabricated with the six different growth conditions shown in Fig. 3 are plotted in Fig. 4. The cell made at 200 ºC without any *in situ* annealing has extremely poor performance due to a large number of pinholes formed during the post processing of the device. This resulted in low power conversion efficiency achieved of ~0.5% which is in agreement with the poor crystallinity and excess Te observed on this sample. In contrast, much improved performance was observed in the samples either directly grown at 400 ºC or annealed at this temperature. Table 1 compares the characteristics for the cells made for the six different PLD fabrication conditions. The J_{SC}, V_{OC}, and FF for the annealed devices increases with increasing anneal time up to 20 minutes, which had a power conversion efficiency at 7.3% with a J_{SC}, V_{OC}, and FF of 20.8 mA/cm^2, 698 mV, and 50.3%, respectively. This efficiency is a 20% increase relative to the cell made with CdTe grown directly at 400 ºC. When annealing longer than 20 minutes there was a drop off in efficiency due to drops in the J_{SC} and FF while the V_{OC}valueis slightly increased. Considering the FF is directly affected by series resistance (thus doping) as well as grain size, and taking into account the similarity between the 20 and 40 minute annealed CdTe the reduction in FF in the 40 minute post annealed device may be attributed to non-optimal $CdCl_2$ anneal condition, increased contact resistance between CdS and FTO from prolonged exposure to the higher temperature of 400 ºC, or excess diffusion between CdS and CdTe at the junction.

The first of these hypotheses was tested by making identical devices, but using different $CdCl_2$ annealing conditions. The results are shown in Figure 5 where $CdCl_2$ anneal times of 15 (same as previous cells), 20, and 25 minutes were used in the post-processing. The $CdCl_2$ time was clearly not optimized for the devices that underwent the 40 minute post annealing. The device that underwent 20 minutes of $CdCl_2$ annealing was the best performing cell with an efficiency of 7.6% with a J_{SC}, V_{OC}, and FF of 18.9 mA/cm^2, 728 mV, and 55.1%. This can be explained by understanding that the longer post annealed devices are more crystalline. The higher the initial crystallinity of CdTe the longer time it will take for the $CdCl_2$ diffusion process to fully complete. It could be expected that even better performance will be achieved for increasing post anneal and $CdCl_2$ anneal times.

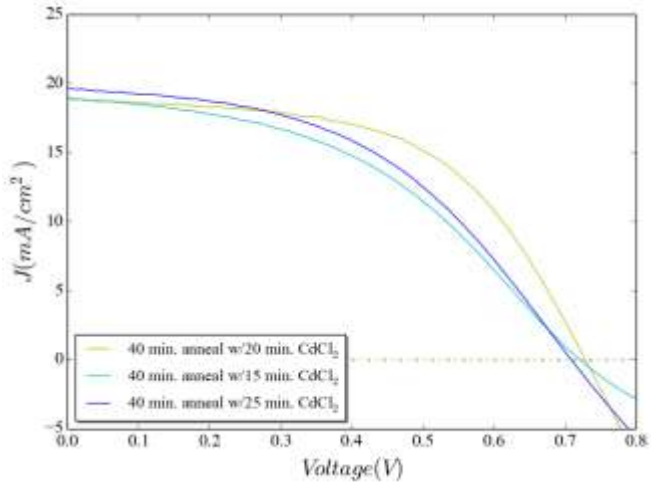

Fig 5: J-V plots of three cells that underwent identical PLD post annealing, but had three different $CdCl_2$ anneal times.

The EQE measurements on the set of five samples from Table 1 (minus the 200 ºC direct grown cell) are displayed in Fig. 6. It is seen that the 40 minute post annealed and the

400ºC direct growth cells haveworse collection above the absorption edge of CdS, of roughly 515 nm, than the other devices suggesting that there is more recombination or reduced doping in the CdTe for these devices. The EQE of the 5, 10, and 20 minute post annealed cellshave increased collection below the CdS band edge with increasing anneal time. This is suggestive that a higher quality CdS, with less recombination sites, was formed during the annealing process up to 20 minutes. When annealing for longer than 20 minutes the EQE shows that the majority of the current loss or poor collection happens in the CdTe, above the CdS band edge. The morphology and crystallinity of CdTe grains correlate to further electron doping and grain evolution of CdTe in the $CdCl_2$annealing process. Further insights may be obtained through the JV plots in Fig. 4when analyzing equation (3), which is a model for the ideal solar cell taking into account parasitic losses.[3] In this equation R_s is the cell's series resistance, R_{sh} is the shunt resistance, k_B is Boltzmann's constant, and T is temperature. Clearly, the 40 minute post annealed cell has much higher R_s than the 20 minute post annealed cell, which explains the lower FF in the former. Considering the R_s of our devices is considerably higher than the ideal value, better performance is anticipated when electron doping of the CdTe as well as the back contact are optimized.

$$J = J_{SC} - J_o\left(e^{\frac{q(V+JA\,R_S)}{k_BT}} - 1\right) - \frac{V+JAR_s}{R_{sh}} \quad (3)$$

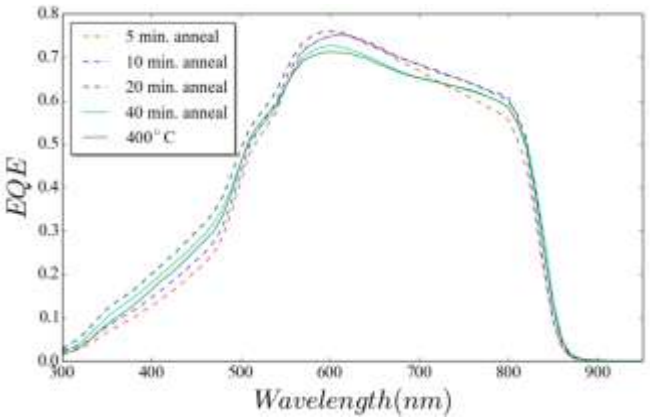

Fig 6: External quantum efficiencies for cells with CdTe made with five different PLD fabrication conditions.

CONCLUSION

In summary, low temperature growth and processing conditions were explored for fabrication of CdTe/CdS thin film solar cells using *in situ* PLD. Through a comparative study on samples made at 400 °C or at 200 °C followed with annealing at 400 °C for 5-40 minutes in 20 Torr Ar, we have found the cell characteristics are affected considerably when the microstructure and crystallinity of CdS/CdTe evolve differently in these two processes. The *in situ* annealed cells have improved V_{OC}, J_{SC}, and FF compared to the cell with direct grown CdTe. The post annealing was shown to reduce the relative amount of Te in the CdTe films which improved $CdCl_2$ doping and produced more crystalline films with mixed (110) and (111) phase orientations depending on the length of the annealing time. The annealed samples have an improved CdS/CdTe interface, shown by increasing values in V_{OC}, and promotes better electron collection due to larger CdTe grain size relative to CdTe thickness and overall higher quality CdTe and CdS. The device with 40 minute annealed CdTe obtained an efficiency of 7.6% which is to date the highest efficiency for CdS/CdTe solar cells made entirely by PLD. The longer post annealed devices require longer $CdCl_2$ treatment to reach optimal performance. The different fabrication procedure and conditions demonstrated in this work is advantageous for making complex structures *in situ* with PLD because the various materials used for deposition generally have different optimum conditions for PLD fabrication. Controlling the anneal time will allow for control of inter-diffusion between layers when making either single junction photovoltaics or devices with more complex structures. The low temperature growth increases the growth rate due to higher sticking coefficient requiring less time to fabricate and the post annealing ensures that the quality of material is not sacrificed.

ACKNOWLEDGEMENTS

The authors acknowledge support in part by NASA contract No. NNX13AD42A, ARO contract No. W911NF-12-1-0412, W911NF-16-1-0029and NSF contracts Nos. NSF-DMR-1105986, NSF-DMR-1337737, NSF-DMR-1508494and NSF-EPSCoR-0903806, and matching support from the State of Kansas through Kansas Technology Enterprise Corporation. P.H. would like to acknowledge the support from the Redeker Scholarship made possible by Maynard and Carol Redeker.

REFERENCES

[1] A. Luque, S. Hegedus, Handbook of photovoltaic science and engineering, Handbook of photovoltaic science and engineering, (2011).
[2] P. Würfel, U. Würfel, Physics of solar cells: from basic principles to advanced concepts, Physics of solar cells: from basic principles to advanced concepts, (2009).
[3] J. Nelson, The physics of solar cells, The physics of solar cells, (2003).
[4] M.A. Green, K. Emery, Y. Hishikawa, Solar cell efficiency tables (version 44), Progress in Photovoltaics: Research and Applications, (2014).
[5] A.D. Compaan, A. Gupta, J. Drayton, S.H. Lee, S. Wang, 14% sputtered thin-film solar cells based on CdTe, physica status solidi (b), 241 (2004).
[6] X. Wu, J. Keane, R. Dhere, C. DeHart, A. Duda, T. Gessert, S. Asher, D. Levi, P. Sheldon, 16.5%-efficient CdS/CdTe polycrystalline thin-film solar cell, James & James Ltd.: London, 995 (2001).
[7] J. Britt, C. Ferekides, Thin-film CdS/CdTe solar cell with 15.8% efficiency, Applied Physics Letters, (1993).
[8] M. Gloeckler, I. Sankin, Z. Zhao, CdTe solar cells at the threshold to 20% efficiency, Photovoltaics, IEEE Journal of, 3 (2013) 1389-1393.

[9] N. Amin, T. Isaka, A. Yamada, M. Konagai, Highly efficient 1μm thick CdTe solar cells with textured TCOs, Solar Energy Materials and Solar Cells, 67 (2001) 195201.
[10] P. Paulson, V. Dutta, Study of in situ CdCl2 treatment on CSS deposited CdTe films and CdS/CdTe solar cells, Thin Solid Films, 370 (2000) 299306.
[11] B.E. McCandless, R.W. Birkmire, D.G. Jensen, J.E. Phillips, I. Youm, Processing issues for thin film CdTe/CdS solar cells, 394 (1997) 647.
[12] G.J. Bauhuis, P. Mulder, E.J. Haverkamp, J. Huijben, 26.1% thin-film GaAs solar cell using epitaxial lift-off, Solar Energy Materials and Solar Cells, (2009).
[13] P. Harrison, J. Meeth, J. Liu, R. Lu, L. Feng, J. Wu, The effects of fabrication pressure on the physical properties of CdS/CdTe thin film solar cells made via pulsed laser deposition, Photovoltaic Specialists Conference (PVSC), 2013 IEEE 39th, (2013).
[14] L. Bing, L. Jianwei, X. Guowei, L. Rongtao, F. Lianghuan, W. Judy, Development of pulsed laser deposition for CdS/CdTe thin film solar cells, Applied Physics Letters, 101 (2012).
[15] C.-C. Jose Luis, Z. David, CdTe thin film growth model under CSS conditions, Solar Energy Materials and Solar Cells, 93 (2009).
[16] D. Bonnet, Manufacturing of CSS CdTe solar cells, Thin Solid Films, (2000).
[17] K. Durose, P.R. Edwards, D.P. Halliday, Materials aspects of CdTe/CdS solar cells, Journal of Crystal Growth, 197 (1999).
[18] R. Eason, Pulsed laser deposition of thin films: applications-led growth of functional materials, Pulsed laser deposition of thin films: applications-led growth of functional materials, (2007).
[19] P. Harrison, A. Kadhim, G. Zeng, J. Wu, Regulating CdTe Grain Boundaries with CdTe/ZnTe superlattice spacers for increased solar cell performance, Unpublished, (2015).
[20] J. Meeth, P. Harrison, J. Liu, B. Li, R. Lu, L. Feng, J. Wu, Pulsed Laser Depositin of Thin Film CdTe/CdS Solar Cells with CdS/ZnS Superlattice Window, Photovoltaic Specialists Conference (PVSC), 2013 IEEE 39th, (2013).
[21] H. Pengchen, L. Bing, F. Lianghuan, W. Judy, J. Haibo, Y. Huimin, X. Xinju, Effects of the substrate temperature on the properties of CdTe thin films deposited by pulsed laser deposition, Surface and Coatings Technology, 213 (2012).
[22] B.E. McCandless, L.V. Moulton, R.W. Birkmire, Recrystallization and sulfur diffusion in CdCl2-treated CdTe/CdS thin films, Progress in Photovoltaics: Research and Applications, 5 (1997).
[23] P.M. Amirtharaj, F.H. Pollak, Raman scattering study of the properties and removal of excess Te on CdTe surfaces, Applied Physics Letters, (1984).
[24] V. Dzhagan, M.Y. Valakh, J. Kolny-Olesiak, Resonant Raman study of phonons in high-quality colloidal CdTe nanoparticles, Applied Physics Letters, (2009).
[25] S.S. Islam, S. Rath, K.P. Jain, S.C. Abbi, C. Julien, Forbidden one-LO-phonon resonant Raman scattering and multiphonon scattering in pure CdTe crystals, Physical Review B, (1992).
[26] B. Ghosh, S. Hussain, D. Ghosh, R. Bhar, A.K. Pal, Studies on CdTe films deposited by pulsed laser deposition technique, Physica B: Condensed Matter, 407 (2012) 4214-4220.
[27] A. Picos-Vega, M. Becerril, O. Zelaya-Angel, Cd self-doping of CdTe polycrystalline films by co-sputtering of CdTe–Cd targets, Journal of applied Physics, (1998).