THD ANALYSIS OF DIFFERENT CASCADED MULTILEVEL INVERTER TOPOLOGIES WITH DC MEASUREMENT ALGORITHM FOR DRIVE APPLICATIONS

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Abstract

This paper presents about the development of new single phase cascaded MLI topology and comparative study of new development one with the existing topologies. A single basic unit is first developed and cascaded connection of basic units made to generate positive levels at the output. Therefore, to generate all the voltage levels, H Bridge is added in the outside of series connected basic units .The structure forms the new proposed topology. Four algorithms are proposed for measuring the magnitude of DC voltage. The comparative study is made to prove that the proposed inverter uses the reduced no of power switches, driver circuits and DC voltage sources. The performance and functional of proposed system are confirmed by both computer simulations using MATLAB software and laboratory prototype implementation.

Keywords: *Cascaded MLI, Basic Units,DC Voltage Measuremnts*

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I. INTRODUCTION

Multilevel inverters includes an arrays of power semiconductors switches and Dc voltages sources, the output of which generates voltage with stepped waveforms .In recent days, multilevel power conversion technique has been considered as the key element in power electronics field development .In comparison with the conventional two level inverter, the incriminating process of DC voltage sources leads to more qualified output waveforms with lower harmonics content. The main advantage of multilevel inverter is high power quality, lower order harmonics, lower switching losses and better electromagnetic interference.

Three main structures of multilevel inverters have been presented: Diode clamped multilevel inverter, flying capacitor multilevel inverter and cascaded multilevel inverter. Out of these three structure, cascaded MLI its doesn't requires clamping diodes and flying capacitors and it require the lowest number of semiconductors switches to produce particular leveled waveform. These cascaded multilevel inverter has two broad categories i.e. Symmetric MLI with same DC voltage source amplitude and asymmetric MLI with the different DC source magnitude. Asymmetric structure produces higher number of levels comparing with symmetric structure.

Unfortunately, MLI structures have some disadvantages. Larger number of levels increases the number of switching levels that must be controlled. Therefore, a new topology developed to increase the number of generated output levels with the aid of lower switches.

At the first step, single basic unit is developed. By series connection of several proposed units, a new proposed topology is developed, which will produce only positive levels at the output. In addition to the basic series connected unit, H Bridge will be added at output to produce positive negative output levels. Four different algorithms are proposed for measuring DC voltages. The proposed multilevel inverter is compared with the other MLI topologies. Based on these comparisons, developed cascaded inverter requires minimum number of power switches, diodes, driver circuits and DC voltage sources. The experimental results prototype model and simulation have demonstrated the feasibility and practicality of the proposed inverter.

II. PROPOSED TOPOLOGY

Fig.1 shows the proposed basic unit structure comprised of 5 unidirectional switches and 3 dc voltage sources. The switch combinations (S_2, S_4), (S_1, S_3, S_4, S_5) and (S_1, S_2, S_3, S_5)

should not be triggered to avoid short circuit issues. Table I depicts the switching sequence of the proposed basic unit.

Table 1. Switching Scheme for Proposed Basic Unit

State	S_1	S_2	S_3	S_4	S_5	V_0
1	0	0	0	0	1	0
2	1	0	1	1	0	V_1+V_3
3	1	1	1	0	0	$V_1+V_2+V_3$

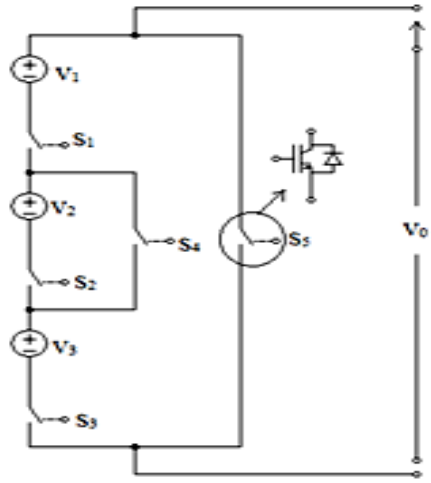


Fig. 1. Basic unit

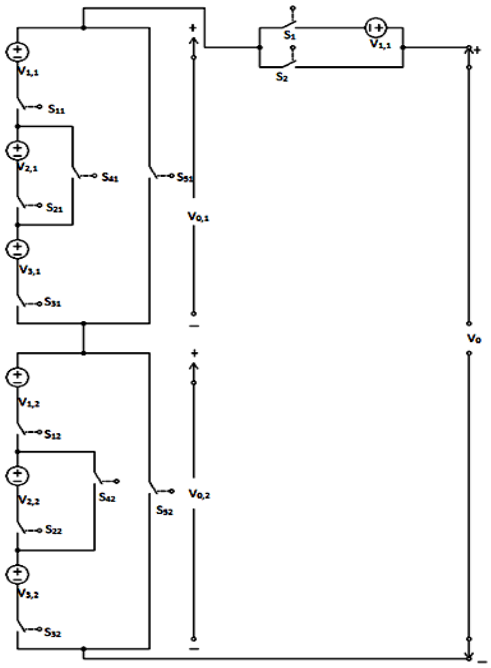


Fig.2 (a). Proposed topology

It's inferred that, basic unit will generate 0, (V_1+V_3), $(V_1+V_2+V_3)$ levels. Fig 2.(a) shows the series connected basic unit. As this kind of inverter will generate all the voltage levels except V_1,an additional dc source with V_1 magnitude added in the system. It's important to note that, the proposed system generates only positive levels; H Bridge is added at the output side of the circuit to get both positive and negative levels.V_1, S_1, S_2 combination will produce lowest output level. Table II indicates the switching sequence of series connected basic unit system.

Output voltage levels can be calculated using,

$V_0(t)=V_{0,1}(t)+V_{0,2}(t)+\ldots\ldots\ldots\ldots\ldots+V_{0,n}(t)+V_0(t)$

$\mathbf{N}_{switch}=5N_{bs}+6$; $N_{DC\ source}=3N_{bs}+1$ Where N_{bs} is number of basic units in the proposed

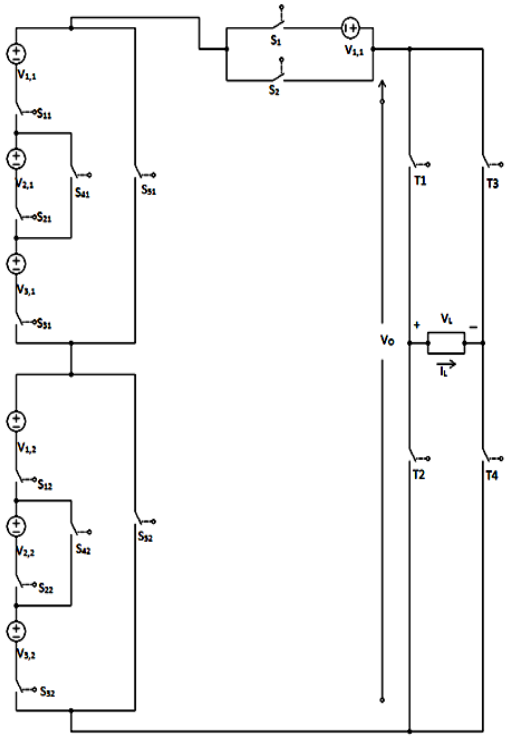


Fig.2 (b). Proposed topology with H Bridge connection

Table 2. Switching Scheme of Proposed Topology

Switches	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0
S_1	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0
S_2	1	0	1	1	1	1	1	0	1	1	1	1	1	0	1
S_{11}	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0
S_{21}	0	0	0	1	0	1	1	1	1	1	0	1	0	0	0
S_{31}	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0
S_{41}	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0
S_{51}	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1
S_{12}	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0
S_{22}	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0
S_{32}	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0
S_{42}	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0
S_{52}	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1

III. DIFFERENT TOPOLOGIES IN CASCADED MLI

In multi level inverter systems, the requirement of power devices depends upon the requirement of no of levels in the output voltage. The increment in the switches count leads to increase the circuit size, cost, installation area and makes the control as complex. Therefore to provide large no of levels without increasing switches, different topologies were developed.

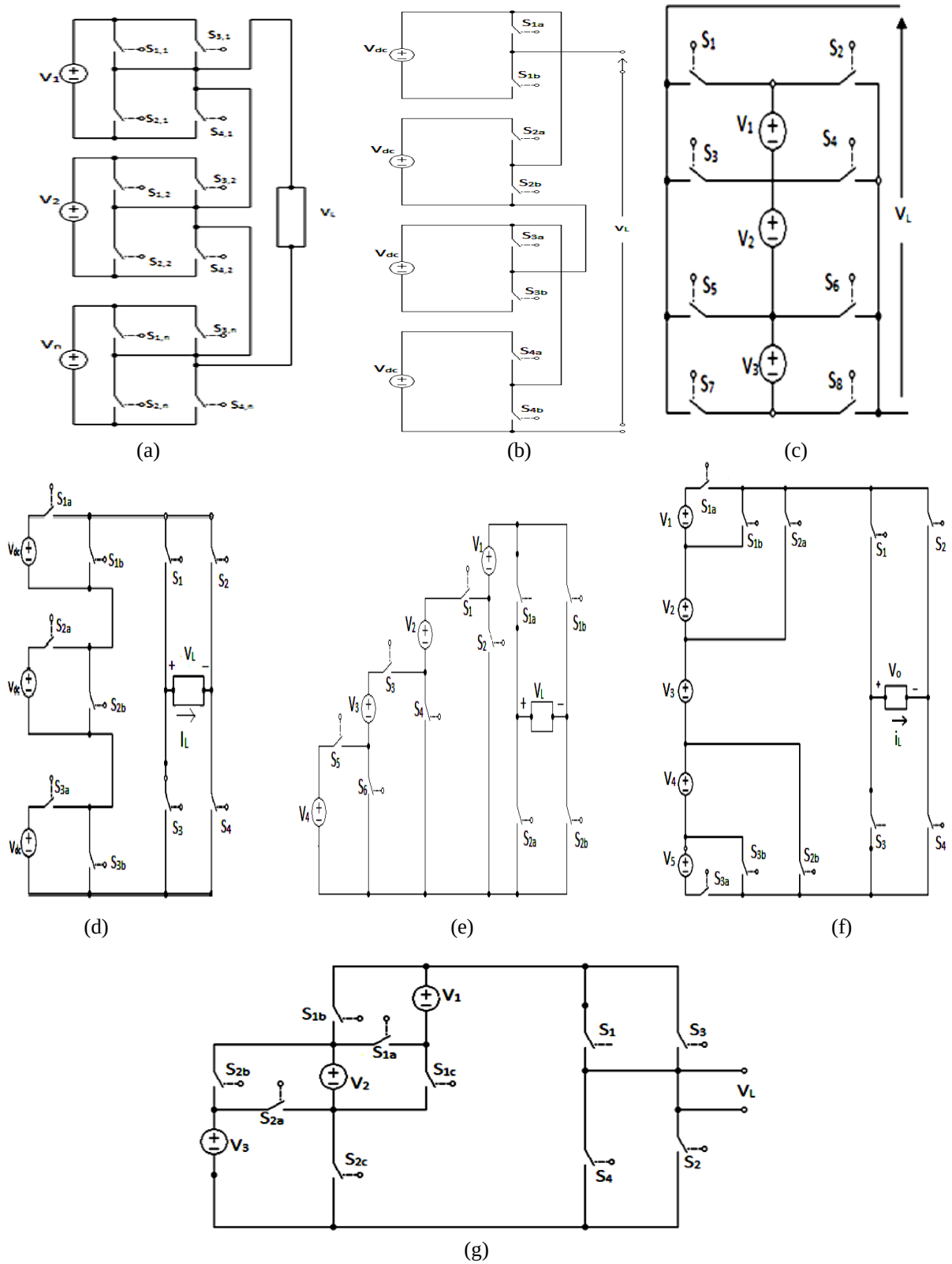


Fig.2 (c). Different MLI topologies for comparative study

Topology B:

The topology B is shown in fig.2.c.For a three phase topology, it requires ($3N_L$-3) switches and ($3\ N_L$ -3)/2 isolated DC sources. Where N_L is the no of levels in line to line output waveform. Each basic unit is composed of two inverter legs as connection shown in Fig.2.c.When switches S_1,S_2conducts,$V_0(t)=V_{dc}$, When switches S_1',S_2'conducts,$V_0(t)$ = -Vdc When switches S_1, S_2' conducts (or) S_2, S_1' conducts $V_0(t)$ = 0.The no of voltage levels in the line to line and phase to neutral is given by

V_{AB} (t) =$4N_{bs}$+1

V_{AN} (t) =$2N_{bs}$+1

Where N_{bs} is the no of basic systems per phase. In this topology, the no of output voltage is always odd.

Topology C:

Topology C consists of X dc voltage sources and 2(x+1) bidirectional switches.Here, DC sources may chosen with different voltage levels, leads to asymmetric topology.

No of voltage levels n=1+x(x+1)

Output voltage levels are given by $-\sum_{j=1}^{x}(\mathrm{Vdc,j}) + \sum_{j=1}^{x}(\mathrm{Vdc,j})$

Maximum output voltage ($V_{0,max}$)= $\sum_{j=1}^{x}(\mathrm{Vdc,j})$

The usage of bidirectional switches leads to more power losses.

Topology D:

The basic unit of this topology consists of dc sources with 2 switches. Basic units are connected in series. The output voltage of a series connected basic unit is zero or positive value. Full bridge circuit added to the output terminals for generating both positive and negative voltage levels.IGBT with anti parallel diode is chosen as switch.3 possible methods to produce different voltage levels at the output side.

Method1: All DC Voltage sources equal to Vdc.Symmetric topology. No of levels= n+1. Method2: Binary fashion. The no of levels increases in exponential manner. No of levels =2^n

Method3: DC voltage sources are chosen based on the equations, $V_1=V_{dc}$; $V_2=2V_{dc}$…….$V_n = nV_{dc}$

The no of levels increases in exponential manner.

No of levels =2n

Maximum output voltage of this topology is $V_{0,\ max}$= (2n-1) V_{dc}

Topology E:

Consider with an conventional H-Bridge MLI, by using 4 Switches, 3 level output waveform is produced. With addition of 4 switches on left hand side, the levels increased to 7.But the requirement of more DC sources make this system much suitable for PV power generating systems.

No of switches required=m+1

No of diodes= m+1

Input DC sources= (m-1)/2

Topology F:

The proposed topology consists of n DC voltage sources & (n+1) switches. DC source can be taken as symmetric or asymmetric .Care must be taken while turning on & off of the upper and bottom level switches to avoid short circuit problems.S_1,S_2…….S_n and S_1',S_2'……S_n' will not turned on simultaneously.IGBT with antiparallel diodes used as switches. Depending upon the switching sequence, this system produces positive output voltage levels. This system cannot generate zero and negative level at the output side.

No of levels=n, no of switches per unit=n+1, no of IGBT per unit=2n-2.

The output maximum voltage $V_{0\ max}=\sum_{i=1}^{n} Vi$

Topology G:

The topology G consists of dc voltage sources independent of each other. Here the switches are termed as S_{1a}-Sna, S_{1b}-S_{nb}, and S_{1c}-$S_{nc.}$ When the switch S_{1a} ON, V_1, V_2 are connected at the output. By connecting dc voltage sources in series or parallel combination the output levels will be increased 4n+3.

IV. COMPARISON OF PROPOSED SYSTEM WITH OTHER TOPOLOGIES

The utmost aim of developing new cascaded MLI topology is to increase the no of output voltage levels with the usage of minimum no of power electronics components.Compartive analysis made between the developed topology with respect to the no of IGBT's, driver circuits, diodes and DC voltage sources. From the above discussions, it can be concluded that, the proposed inverter has the best performance among all the other topologies. The remarkable advantages are reduced IGBT switches, diodes, driver circuits and DC voltage sources.

V. EXPERIMENTAL RESULTS

The ability of the proposed inverter is confirmed by mat lab simulation and scaled prototype structure.IGBT used in the prototype are .The microcontroller has been used to generate all the switching sequences. In the simulation and hardware implementation, R load is assumed with R=100 OHM. The simulated output voltage and current waveforms are shown in fig 7. Also the harmonic spectrums of the proposed and other topologies

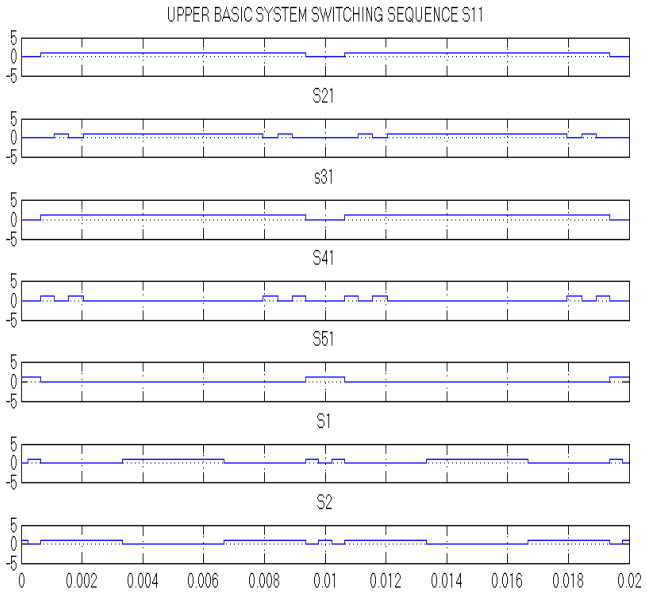


Fig .4a. Switching sequences for the upper basic unit proposed topology

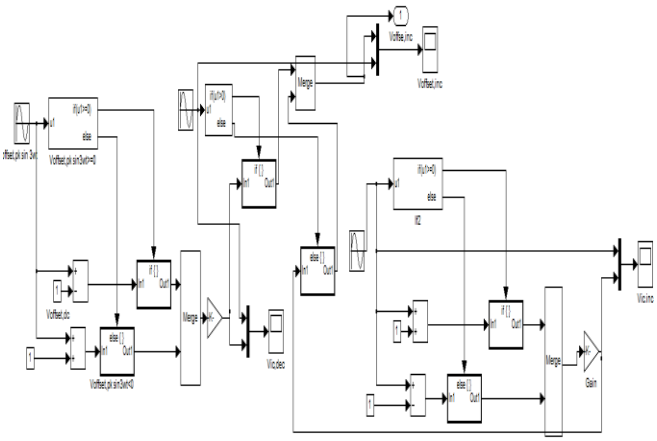


Fig .4b Switching sequences unit for proposed topology

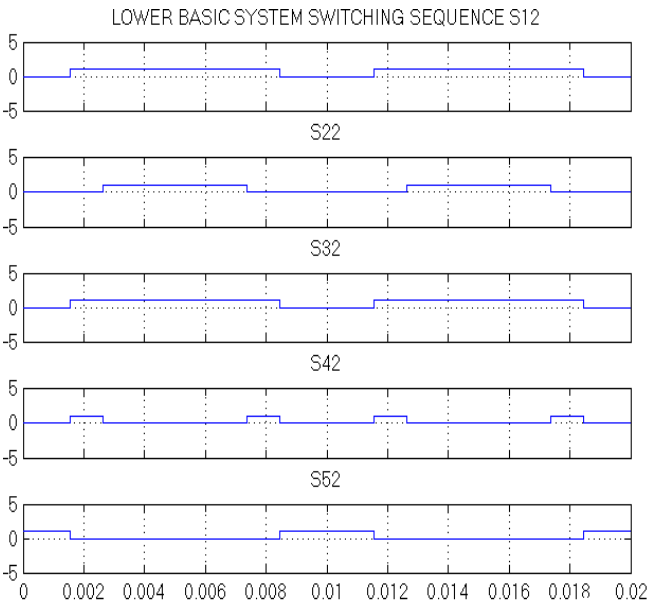


Fig .5. Switching sequences for the lower basic unit proposed topology

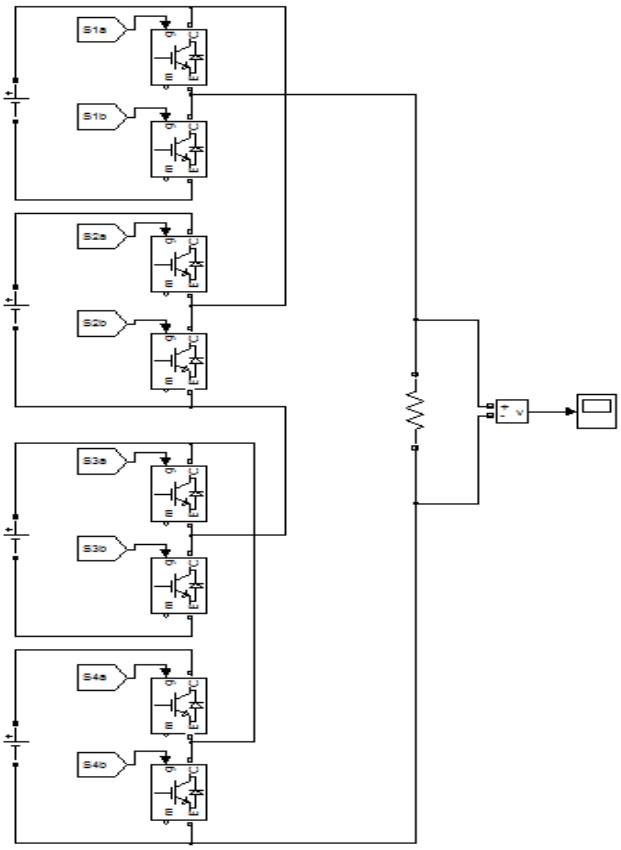


Fig.6. Simulation circuit for the topology B

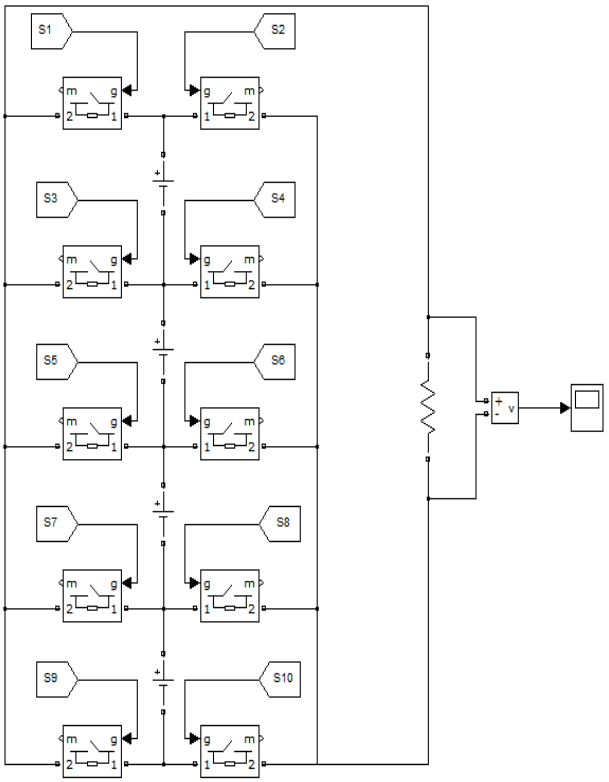


Fig .7. Simulation circuit of Topology C

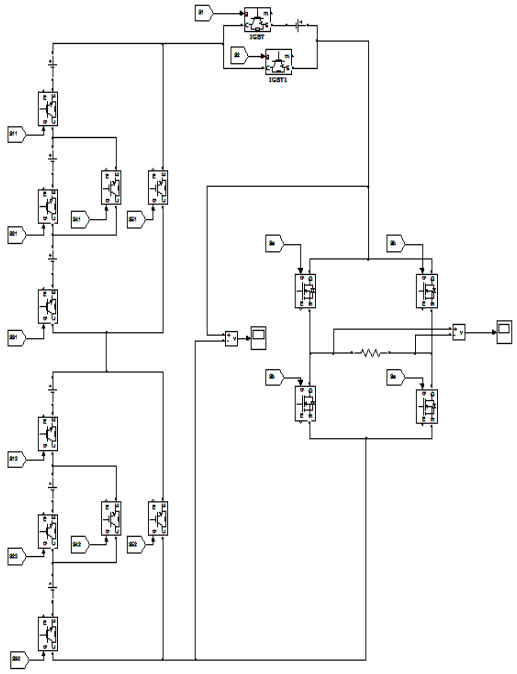


Fig .8. Simulation circuit of the proposed multilevel inverter

Table III: THD Comparison of Multilevel Inverters

S.No	Topology	THD%
1	B	17.12
2	C	9.38
3	D	12.11
4	E	9.38
5	F	7.65
6	Proposed topology	5.55

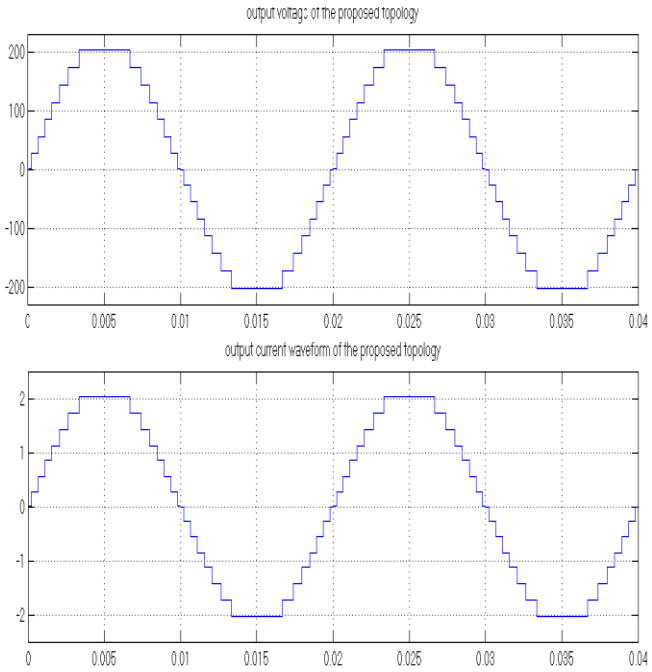


Fig .9. Output voltages and current waveform of the proposed multilevel

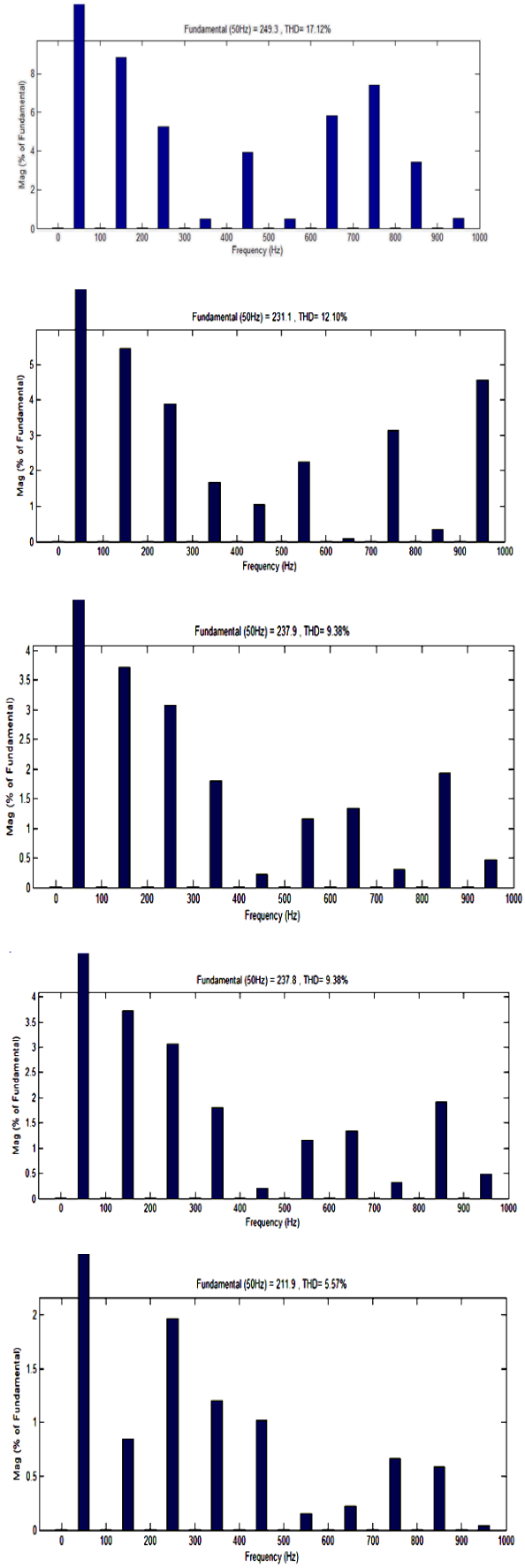
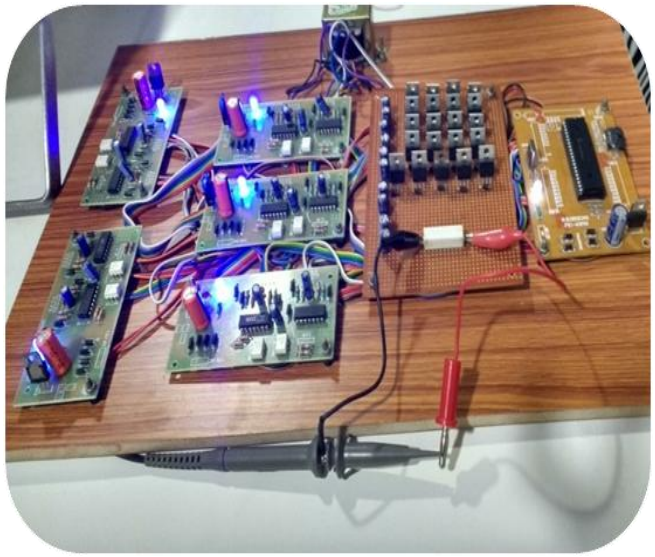


Fig.10. Simulation results showing the Harmonic spectrums of different cascaded multilevel inverter (b, c, d, e, f, g) topologies

VI. EXPERIMENTAL RESULTS

The ability of the proposed inverter is confirmed by mat lab simulation and scaled prototype structure. IGBT used in the prototype is .The microcontroller PIC 16F887 has been used to generate all the switching sequences. In the simulation and hardware implementation, R load is assumed with R=100 Ohm. The simulated output voltage and current waveforms are shown in fig 9. Also the harmonic spectrums of the different multilevel inverter topologies and the proposed inverter from the mat lab simulation systems are shown in fig 10.From the table III it's concluded that the proposed inverter has the minimum THD limits.



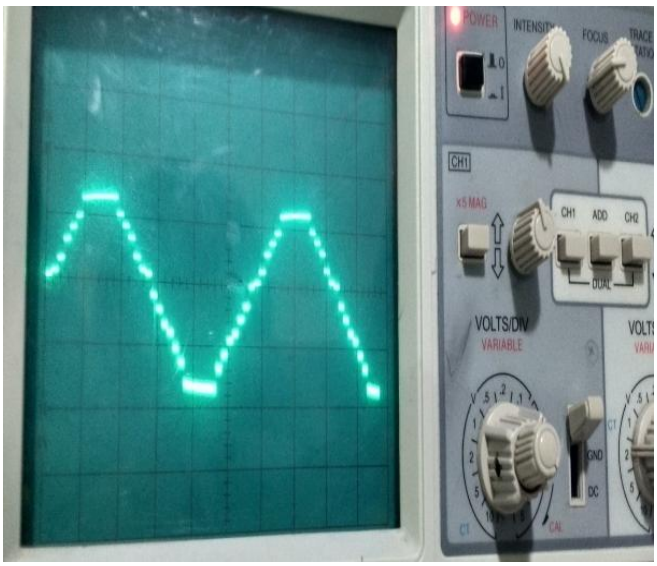


Fig. 11. Hardware implementation of proposed inverter prototype model and output voltage waveforms

VII. CONCLUSION

In this paper, a new cascaded H-Bridge MLI topology is proposed. This proposed system produces only positive voltage levels at the output side. Therefore H-Bridge is added at the output side to generate both positive and negative voltage levels. Several comparisons are made between the proposed one with other topologies. From this comparative study, it's concluded that the new developed topology requires less no of IGBT'S, diodes and driver circuits and DC voltage sources. This developed system has better performance. The performance of new developed system checked out by implementing with scaled down experimental hardware setup.

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