ENHANCING PERFORMANCE OF NOC BY EMPLOYING FAULT TOLERANT ROUTING ALGORITHM

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Abstract

In the state-of-art of high performance computing, Network on chip (NoC) is emerging as a new trend for inter-connection solutions to dense System on chip (SoC) design. The key advantages of NoC are high performance and scalability. Despite those improvements over the conventional shared-bus based systems, NoC are not shown as the ideal solution for the future SoC. Recently, with the three dimension (3D) technology, the 3D NoC has been designed to overcome the high power consumption, high cost communication and low throughput. In this project, 3x3x2 virtual channel router with mesh topology connection is to be designed and synthesized using Xilinx EDA tools. A 3D router design which can support at maximum seven requests simultaneously depending upon location of router in NoC. This 3D model is natural extension of 2D mesh NoC. The routing algorithm will be the Look Ahead –XYZ routing which is simple and free of deadlocks and enhances system performance by reducing packet delay. This will be suitable for ultra high speed application with low latency and low power consumption. Here in this project system is simulated using VHDL and implemented on FPGA kit of Virtex 5 LX110T.

Keywords: *SoC, NoC, LA-XYZ, FTLA -XYZ*

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1. INTRODUCTION

The state of art in designing of chip fabrication is moving beyond the system on chip and shared bus methods gets obsolete, to sustain needed performance of system. The bottlenecks of shared bus communication in inter/intra chip communication is overcome by the concept on network on chip. Systematically, arranging the processing elements (PE) and forming a network having dedicated path for each PE for communication, describes the concept of NoC in SoC. With the increasing use of concepts like MPSoC and MIPS, complexity in chip increases which challenges system communication and performance. Increase scalability can be achieved by 3D integration technology for chip fabrication. So, by focusing to improve NoC designing and thereby enhancing system performance is the motivation behind this proposed work.

The backbone element of NoC is the Router. Basically the NoC performance depends on three factors and they are 1) Topology 2) traffic pattern and 3) router architecture. Here, we have chosen mesh topology for the benefits of less complexity, concurrent data passing and others. Again the parameter of traffic pattern, depends upon the complexity of application, so finally here to improve the performance of NoC, we have to improve router performance. The router designing can be optimized by efficient FIFO buffer, arbitration and routing algorithm designing. In this work, we are working to improve routing algorithm to bypass the faulty links/ nodes in the path of packet transition from source to destination. By comparing conventional dimensional order routing along with look –ahead with fault by passing algorithm on 2D and 3D NoC result are shown by simulation waveform.

2. LITERATURE REVIEW

By advancing to 3D integration from2D integration the system performance is enhanced by 40% in terms of latency and power per hops. Ferro et al[1]. By considering 7x7 router designing in 3D NoC can be designed using hybrid shared bus structure increases performance by reducing ports from 7 to 6 and thereby reducing complexity and hops but degrades performance to some extent. Li at al[2]. Yan et al [3] has proposed unique router architecture having all vertical links in 3D crossbar and thereby reduced the overhead of separate vertical ports. Many researches were also carried out on routing algorithm some are presented here. Ramanujan et al [4] proposed oblivious algorithm named as Random partial minimal (RPM) for managing traffic load in worst case by routing packet randomly to any layer and then routing packet towards destination. By Ben et al [5] proposed the look ahead XYZ routing algorithm where it reduced the pipelining by combining switch allocation with calculating next node identifier in same stage but the proposed algorithm is not susceptible to overcome the problem of deadlock and live lock and thereby failure of algorithm in faulty nodes/ links. Here in our proposed work we are combining advantages of look ahead routing and adding feature of bypassing the faulty link or path. In conventional routing the sequence of routing order is fix for example in XY it will first route packet in X direction and first satisfy X co ordinate with destination X co-ordinate and then same procedure for Y co-ordinate, but if there is faulty node in path the algorithm fails. In our proposed system we librated the restricted sequence of routing and using the advantage of look ahead routing and checking the congestion or faulty status of next node by routing dummy packet, and thereby preventing or bypassing faulty path we

route packet to destination. Similarly, we will explain routing of packets in 2D and 3D NoC in preceding section.

3. PROPOSED NOC ARCHITECTURE

3D-NoC is a scalable Network-on-Chip based on *Mesh* topology. The packets are forwarded among the network using *Wormhole-like* switching policy and then routed according to *Look-Ahead-XYZ* routing algorithm (LA-XYZ). As a flow control, 3D-NoC adopts *Stall-Go* mechanism and *round robin* as a scheduling technique.

The 3D-ONoC system is based upon *Mesh* topology, where *x-addr*, *y-addr* and *z addr* are attributed to each router and define its X, Y and Z coordinates respectively and its position along the network. Many topologies exist for the implementation of NoCs, some are regular (*Torus, tree-based*) and other irregular topologies are customized for some special application. We choose the Mesh topology for this design thanks to its several properties like regularity, concurrent data transmission, and controlled electrical parameters. Figure 3.1shows 3x3x2 3D NoC structure having two stack structured as shown below. Here in this project we are designing NoC with dummy nodes having BRAM and router at every node.

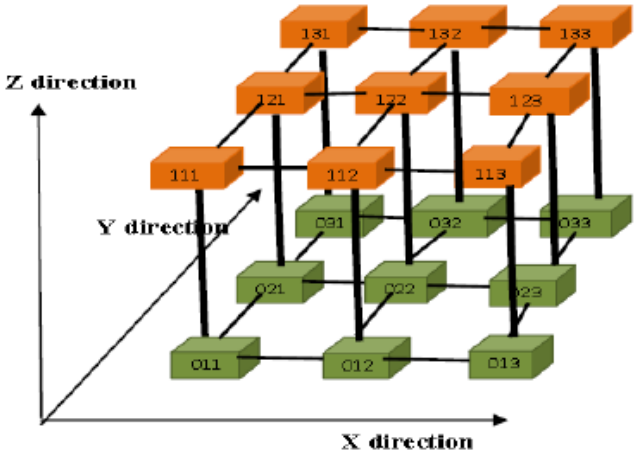

Figure 1: A 3x3x2 NoC proposed two stacked structure with mesh Topology

3D-NoC employs Wormhole switching and forward method here used is Virtual-Cut-Through. The forwarding method mainly depends on the given instance on the fragmentation. Each router buffer stores four flits at given instance. If the packet is divided upto four or more flits the virtual cut through is employed otherwise wormhole is used. Combined switching techniques provide the guarantee of forwarding packet efficiently with small buffer size. This results to reasonable area utilization with enhanced system performance at low power consumption.

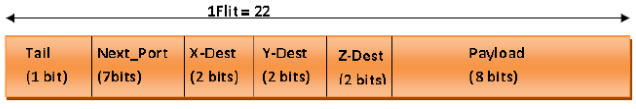

Figure 2. Flit format for 3D NoC

Figure 2 demonstrates the 3D-NoC 22 bits flit format. The first bit is the tail bit which indicates end of the packet. The next seven bits indicate the Next-Port address that will decide the next downstream direction. Two bits are used to store information of destination of each xdest, ydest and zdest. Having two bits for each destination field allows the network to have a maximum size of 3x3x3. 3D-NoC. But if the network size needs to be extended, the addresses fields may also be increased to accommodate a larger network size. Finally the remaining 8 bits are dedicated to store the payload. According to the need of application the size of payload can be modified. Figure 2 shows the 3D-NoC packet format. The architecture do not support a different header flit, so every packet routes to destination along XYZ directional routing having additional tail bit to indicate end of packet.

4. ROUTER ARCHITECTURE

Router directs the data packets to reach their destination by using proper routing algorithm that must avoid the the most frequently encountering problems such as deadlocks, live locks and starvation. Deadlocks can be defined as the data packet gets blocked intermediate between resources. Live locks can be defined as the packet enters the cyclic path and undergoes recurring manner and thus dose not reaches destination. And finally starvation can be stated as the state at which data packet does not get access or grant to pass through particular nodes. Thus the routing algorithm must be smart enough to avoid these problems. Here we are adopting dimensional based static routing along all three axes that are X, Y and Z. the simplicity and ability to overcome the problem of live locks and deadlocks makes this algorithm best choice for this project.

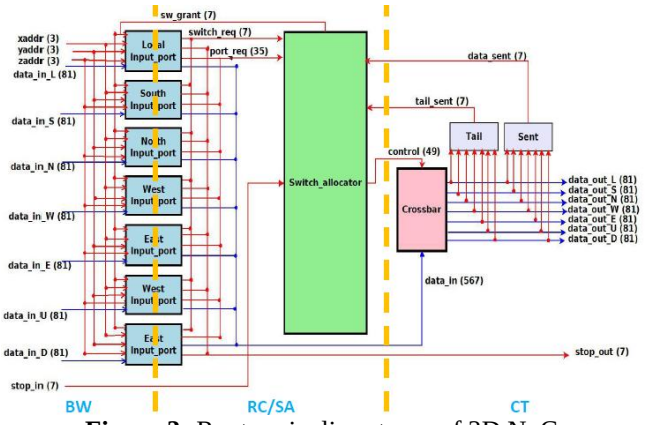

Figure 3: Router pipeline stages of 3D NoC

1) Buffer Writing (BW):

The input buffer simply stores incoming flits before it moves further toward computing routing algorithm. The depth of input buffer is equal to four and each of four can store flit size up to 81 bits as shown in figure. The arbitration is done by using FIFO scheme to manage flits. The buffer occupies sufficiently large amount of area of router but nevertheless improves the performance of system.

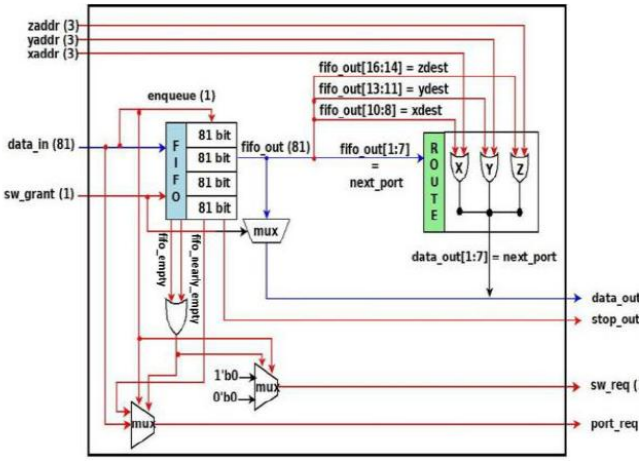

Figure 4: Input port

2) Routing Calculation (RC):

At each input port when flit comes its destination address is fetch and decoded destination address is compared with present node address and comparative computation are done to proceed the flit to particular direction to next node. The computations are done as below

- if xdest is larger than xaddr then New-Next-Port will be EAST. In the opposite case New-Next-Port will be WEST.
- if ydest is larger than yaddr then New-Next-Port will be NORTH, else New-Next-Port will be SOUTH.
- if zdest is larger than zaddr then New-Next-Port will be UP, and if this condition is not satisfied New-Next-Port will be DOWN.
- if xdest is equal to xaddr, ydest is equal to yaddr and zdest is equal to zaddr then New-Next-Port will be SELF.

3) Switch Allocation (Sw):

Once the routing calculation stage ends, the calculated information of next new port is passed over to switch allocator. The switch allocator decides to which output port should be connected to given input port. When the number of inputs demands for same output port that time round robin scheme is implied. This scheme serves fairly to each request without considering priority.

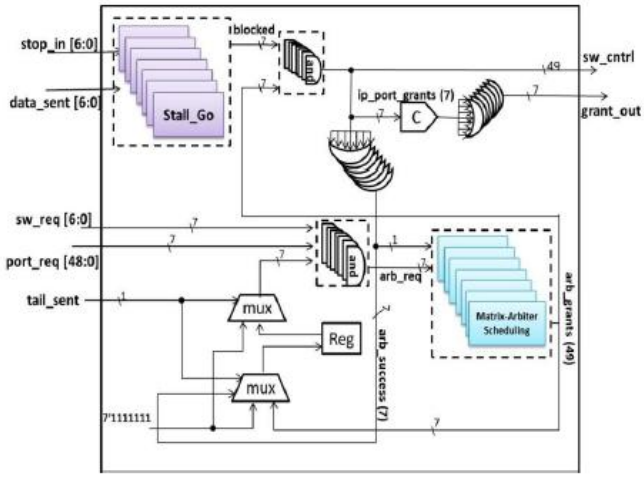

Figure 5: Switch allocator block diagram.

4) Crossbar traversal (CT):

The switch allocator combinedly sends the information of selected input port and next new port to the crossbar. Crossbar routes flit accordingly to the appropriate port as shown in fig. 6. Tail sent signal informs switch allocator that all flits are sent and channel is free for transmission of other flits.

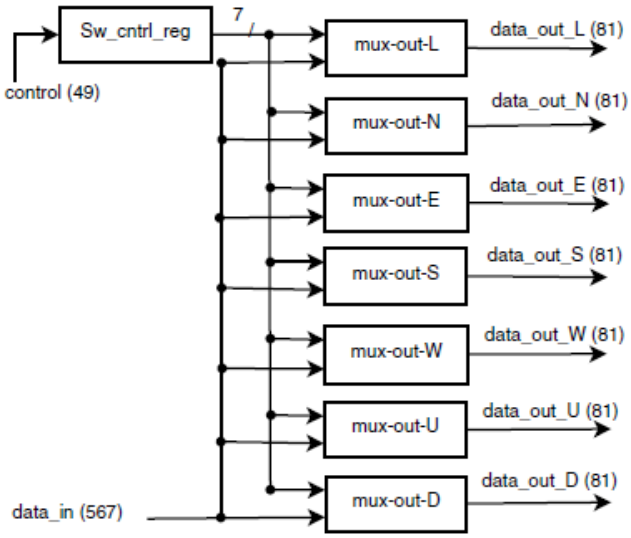

Figure 6: Crossbar circuit

5. RESULTS AND DICUSSION

5.1 Packet Routing Through 3D NoC

In this project we are designing 3D NoC, were each node is connected to Block RAM. To make project less complex and feasible, we have simply designed NoC with dummy nodes that is having BRAM instead of cores. NoC performance is simply evaluated by routing data packet from source node to destination node and calculating number of hops in the path. By employing simplicity of dimensional order routing XYZ packet in the network will be routed. In the case of high traffic application or in the case of node failure, system performance degrades greatly and may cause packet drop or undesirable latency; that time smart routing could make a way out for a packet to reach destination with possible minimal path.

5.1.1 Conventional XYZ Routing

For better understanding of the conventional XYZ routing algorithm route packet to destination here we consider our proposed NoC of dimension 3x3x2 as shown in the figure 7. According to DOR rule of XYZ, it will first take a path to satisfy X co-ordinate by comparing destination and source co-ordinate it moves either east or west side. Once the X co-ordinate is satisfied then the same procedure will be carried out for Y co-ordinate by moving in north or south direction. And finally, after satisfying X and Y co-ordinate it will go for Z co-ordinate by moving up side down or down side up as in our proposed NoC we have only two stacked layers.

From figure, for explaining routing by conventional XYZ algorithm we consider source node as Node 9 having co-

ordinates as (X=1, Y=1, Z=1) and destination node is Node 8 having co-ordinate (X=3, Y=3, Z=0). **(Note: In the figure given below co-ordinates are written in the order of ZYX)**. Thus, to reach destination node packet trace the path shown in the figure 7 by red arrow. In first step at node 0 destination and present node x co-ordinate will be compare and as dest X is less than source X the transition will be in east direction and this transition will continue till node 11 (3, 1, 1). Now at this stage packet transition begins in Y direction till node 17 (3, 3, 1) where Y co-ordinate gets equal and finally, from node 6 it transits downward to reach destination node 8(3, 3, 0). The total number of hops here are 5.

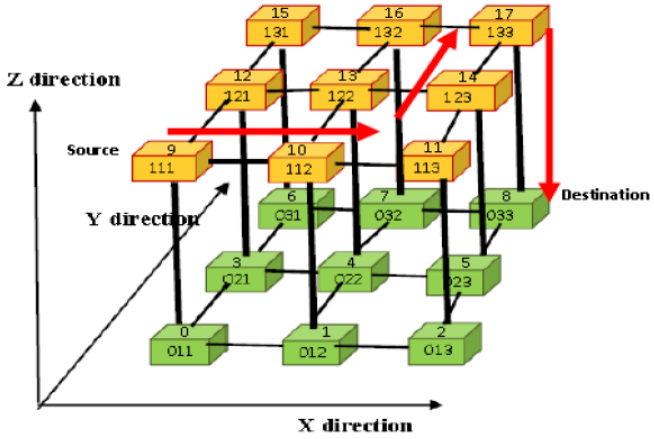

Figure 7: Conventional DOR XYZ routed path for packet in proposed NoC

5.1.2 Look Ahead XYZ With Fault Bypass Routing

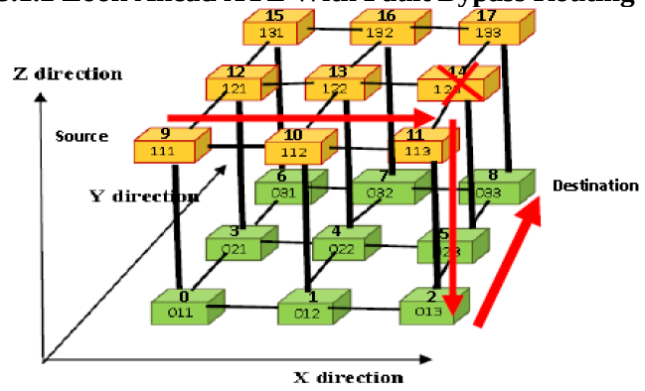

Figure 8: Look Ahead XYZ bypassing faulty node routed path in proposed NoC

Again by keeping same source and destination node as above that is source node as node 9 and destination node as 8, but as shown in the figure 5-2, node 14 is faulty one or the path through node 14 is congested one. So, here the conventional XYZ algorithm fails to route packet to destination, as it strictly follows the sequence of direction that is first X must get satisfied then only proceeds for Y co-ordinate and once both X-Y gets satisfied then it will approach for Z co-ordinate. Due to failure of node 14 Y coordinate cannot be achieved and hence algorithm fails. Now here to overcome fault, we use look ahead XYZ again with no constraints of sequence in direction for routing. In look ahead XYZ, it calculates for next node identifiers and checks for congestion or faulty link on the path ahead, so by this it get acknowledge that node 14 is faulty one and thus it changes its path. Packet after reaching at node 11, router at node 11 calculates for other two nodes in two directions that are node 14 and node 2. As node 14 is faulty, packet will routed in Z direction first rather than Y direction. Thus, after reaching node 11(3, 1, 0) now journey begins in Y direction to reach destination node 8 (3, 3, 0). The total numbers of hops here are 5. Thus, we successfully bypassed faulty node with same number of hops to reach destination.

5.2 Routing of Packet in 2D NoC

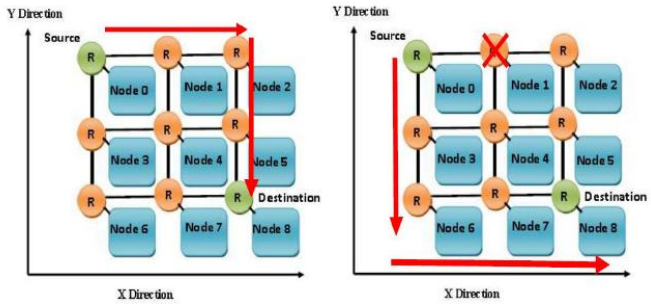

Figure 9: (a) Conventional XY routing in 2D NoC (b) look-ahead XY routing with bypassing faulty node

As explained above for proposed 3D 3x3x2 NoC both routing methods similarly we are employing this on 2D 3x3 NoC as shown in figure 9. Figure 9 (a) shows conventional XY routing that firstly satisfying X co-ordinate and then Y co-ordinate and reaching to destination node 8 from source node 0 in 4 hops. In figure 9 (b) node 2 is failed one and again XY routing fails here, by look ahead with fault bypass method, after getting acknowledgement of fault at node 2 it first follows Y direction and then X direction and reaches destination in 4 hops. Path traced by packet in both ways are shown by red arrows.

5.3 Synthesis Result

After the HDL synthesis phase of the synthesis process, the RTL Viewer is used to view a schematic representation of the pre-optimized design in terms of generic symbols that are independent of the targeted Xilinx device, for example, in terms of adders, multipliers, counters, AND gates, and OR gates.

Figure 10: RTL schematic of router

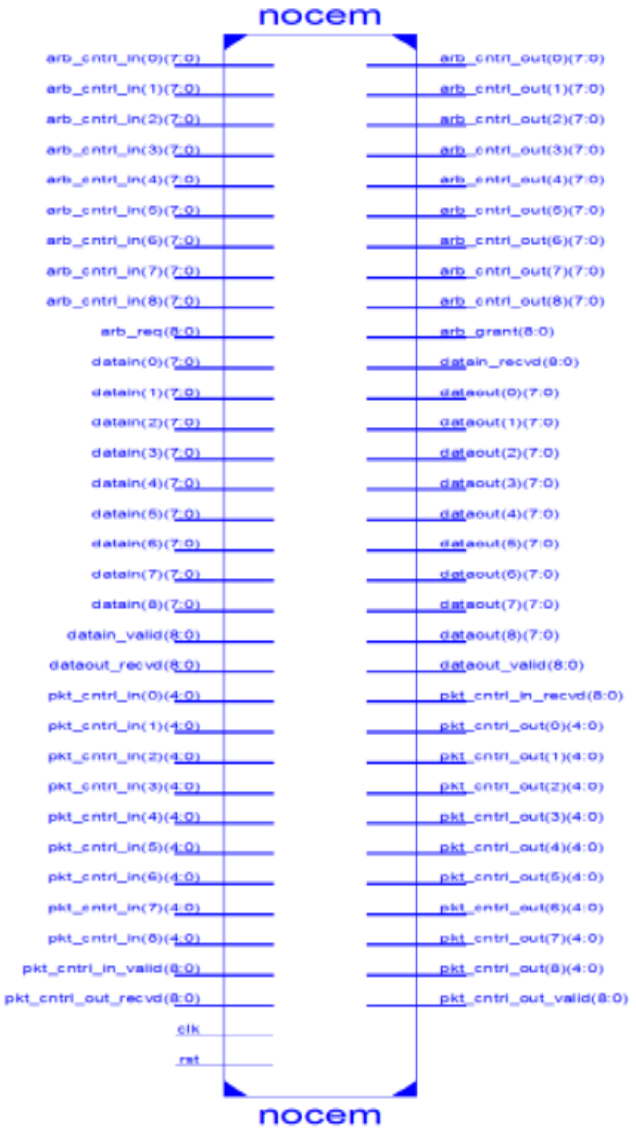

Figure 11: RTL schematic of NoC

Figure 10 shows the RTL schematic of other vital sub-blocks of the NoC project top module *nocem.* NoC comprises of Routers as main block. And router has other sub-blocks such as arbiter, input buffer and crossbar. Routers are interconnected by wires together to from network. On the completion of optimization and technology targeting phase of the synthesis process, Technology Viewer can be used to view a schematic representation of the design in terms of logic elements optimized to the target Xilinx device or "technology," for example, in terms of LUTs, carry logic, I/O buffers, and other technology-specific components.

5.4 Device Utilization

The key architectural characteristics of the NoC were summarized in earlier section 5.2. The actual resources utilization of the selected target device by the designed modules is now presented here. They are being synthesized by Xilinx's ISE design Suite 14.5 EDA tool and create a web file of *Design Summary* in the related project file.

Table 5-1 Device utilization summary of nocem

Target Device Xc5vls110t-1ff1136			
Slice logic utilization	**Used**	**Available**	**Utilization**
Number of slice registers	8,249	69,120	11%
Number used as Flip flops	8,249		
Number of slice LUTs	9,807	69,120	14%
Number used as logic	9,807	69,120	14%
Number using 06outputs only	9,543		
Number using 05 and 06	259		
Number of route-thrus	4		
Number using 05output only	4		
Number of occupied Slices	5,456	17,280	31%
Number of LUT Flip Flop pair used	13,898		
Number with un used FF	5,456	13,898	40%
Number of unused LUT	4,091	13,898	29%
Number of fully used LUT-FF pairs	4,158	13,898	29%
Number of unique control sets	711		
Number of slice register sites lost to control set restrictions	1,831	69,120	2%
Number of bonded IOBs	425	640	66%
Number of BUFG/BUFGCTRLs	2	32	6%
Number used as BUFGs	2		
Average fanout of Non-clock nets	4.75		

Table1: summarizes the FPGA resource utilization by the different systems in terms of registers; lookup tables, and block RAMs. The *nocem* module uses 66% of bonded IOBs out of available resources.

The *NoC* system is running at 100 MHz, which is the clock frequency of the top module, regardless of the size of the mesh. The *router* module runs slower at 33 MHz speed and introduces some latency. This causes delay in the outcome of desired result. The worst case timing is said to have critical path.

5.5 Simulation Results

Here, we have designed 3x3x2 NoC in Xilinx using VHDL, where at each node we have router, so in all 18 routers in 2 stacked layers. To evaluate the performance of NoC we will just route the packet from source to destination, and will trace the path. Firstly we will trace the path of packet and count the number of hops for non faulty link/node and then will trace the path for faulty node and will count number of hops and will compare the simulation results.

5.5.1 Simulation Waveform

The simulation waveform generated for the written and loaded test code is shown in figure 10. The simulation waveform of NoC which shows the various signal such as arbitration request and grant for passing packet through router and switch allocation request and grant signal for connecting input to particular output line in direction of destination. Similarly, other status signal at various nodes is determined from waveform. For getting accurate status and the hops path traced by packet in NoC, here simulated for tracing path of packet in with/without faulty link in NoC. Fig 13 shows the path of packet from node 0 to node 8 referring figure 9(a) and figure 14 shows path for fig 9(b).

Figure 12: Simulation waveforms of NoC

From Fig. 7 here we are using two binary bits to define X-co ordinate, two for Y co ordinate and only one for Z co ordinate to define the node. Considering source node as 0 and destination 8 the simulation waveform shows source and destination node in binary form and the middle nodes of the path along with the hop number is shown by red box. The total numbers of Hops required to reach destination are equal to 4. (Refer fig 8(a)).

In conventional routing XY, the path followed is as shown in fig 9(a), that is 0-1-2-5-8. Firstly, it routes along X direction and then Y direction as there is no issue of congestion or fault in between anywhere. As we are using lookahead routing the next node calculation is already done before next hop, this is also shown in Next_hop waveform as shown fig.13.

From fig. 9(b) source and destination is the same node 0 and node 8 respectively, but the node 2 is faulty or the path is congested one, so the previous path traced during conventional XY will not be the option here. So, by look-ahead fault bypass routing routes packet through path 0-3-6-7-8 and have same number of hops that are equal to four as shown in simulation Fig. 14.

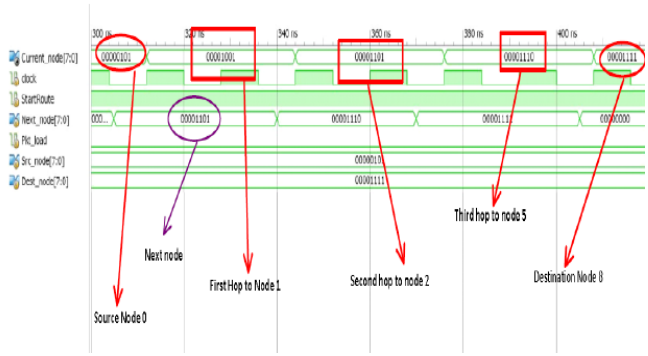

Figure 13: Simulation waveforms for path traced by the packet in NoC without faulty link

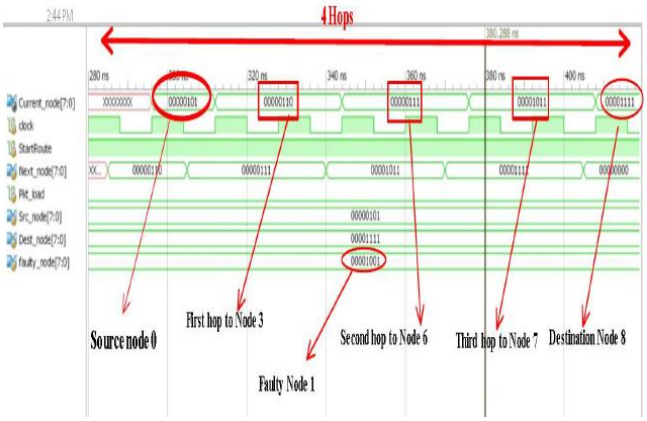

Figure 14: Simulation waveforms for path traced by the packet in NoC with faulty link

Figure 15 shows routing of packet in 3D NoC (for routing path refer figure 7), here source node is considered as node 9 in 2nd stacked layer and destination node as node 8 in 1st stacked layer, thus the path traced by path packet while routing and the middle nodes in binary form and order-wise hops are also shown by red box. The total numbers of hops needed from source to destination are 5 hops. And path is 9-10-11-14-17-8.

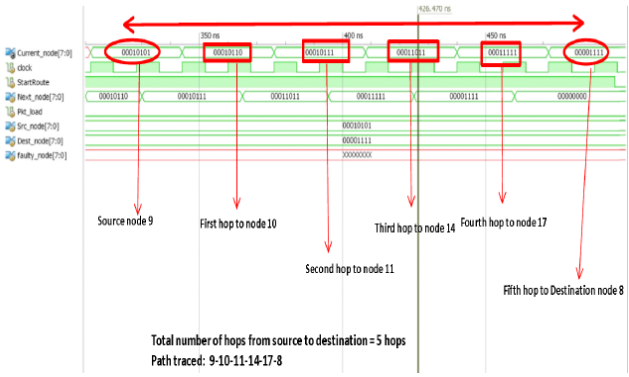

Figure 15: Simulation waveforms for path traced by the packet in 3D NoC

Figure 16 shows routing of packet with a faulty link in 3D NoC, here conventional XYZ routing fails, as shown in figure 8 and the path traced is shown by red arrows. In simulation the same path and hops wise transition of packet from source to destination shown in binary form of node co-

ordinates. The number of hops is same to previous one that is five hops. And path traced is 9-10-11-2-5-8

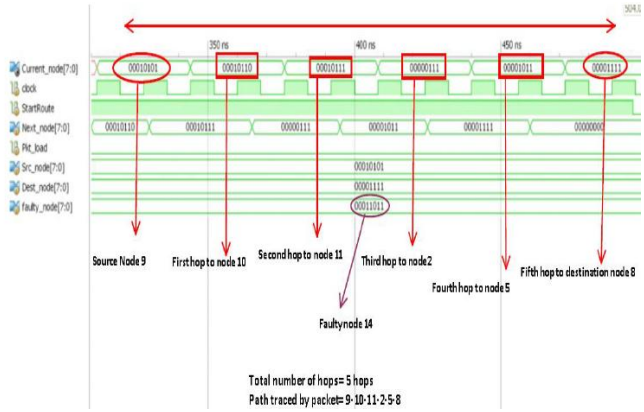

Figure 16: Simulation waveforms for path traced by the packet in 3D NoC with faulty node

5.5 Hardware Implementation

The 2D NoC system is implemented on FPGA kit of Vitex 5 vls110t-1ff1136 as target device and we have implemented packet routing for conventional XY and Look ahead fault bypass XY and the source and destination node along with traced path and number of hops are displayed on LCD 16x2 display. Figure 17 shows the routing of packet for conventional XY without any faulty link/node. And Figure 18 shows the routing of packet in 2d NoC with faulty node/ link. As target device was moving out for memory for 3D NoC it could be implemented on the higher versions of FPGA kit.

Figure 17: FPGA implementation of packet routing in NoC without faulty Link

Figure 18: FPGA implementation of packet routing in NoC with faulty Link

6. CONCLUSIONS

A complete, realistic, fully parameterized, synthesizable, modular, Network on Chip architecture has been tried to present here. The designed NoC comprises of an efficient router with wormhole switching and round robin arbitration having look ahead XYZ with fault bypass routing algorithm. The proposed NoC provides prominent solution, to enhance the performance of MPSoC, for reliable inter/intra communication without latency, low power consumption with deadlock free routing of data packets. It has been successfully implemented on the Xilinx Virtex-5 LX110T FPGA board.

6.1 Opportunities

1. The Look-ahead XYZ with fault bypass routing algorithm keeps the simplicity of Dimensional order routing and ability to avoid faulty path to some extent.
2. The proposed system is a promising solution for high speed parallel computing in highly complex System on chips.
3. Actually designed 3D NoC device, carries advantage of Through Silicon via for inter-layer communication
4. Low power consumption of the system as it is running on slower clock speed viz.100MHz. But, at the same time performance is not sacrificed by shutting off unwanted links.

6.2 Limitations

1. With the given routing algorithm, livelock paths cannot be overcome.
2. Due to the 3D structure, the thermal stability is the issue of concern, and it also degrades system performance.
3. For the more efficient routing adaptive and minimal routing can be employed, but it increase hardware and algorithm complexity

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