PERFORMANCE ANALYSIS AND IMPLEMENTATION OF MODIFIED SDM BASED NoC FOR MPSoC ON SPARTAN6 FPGA

Y. Amar Babu[1], G.M.V.Prasad[2]

[1]*Department of Electronics & Communication Engineering, LBR College of Engineering*
[2]*Principal & Professor in ECE, B.V.C Institute of Technology & Science*

Abstract

To meet todays demanding requirements lowpower consumption, high performance while maintaing flexibility and scalability, system-On-Chip will combine several number of processors cores and other IPs with network-On-chip. To implement NoC based MPSoC on an FPGA, NoCs should provide guaranteed services and be run-time reconfigurable. Current TDM and SDM based NoCs takes more area and would not support run-time reconfiguration. This paper presents modified spatial division multiplexing based NoC on FPGA, in this we have modified complex network interface and proposed flexible network interface and efficient SDM based NoC.This architecture explored feasibility of connection requirements from IP cores during run-time.

Keywords: *NoC, MPSoC, FPGA, NoCs, SDM Based NoC*

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I. INTRODUCTION

According to moore's law chip density is increasing exponentially, allowing multiple processor system-on-chip can be implemented on single FPGA. The main challenge in todaysMPSoC is communication architectures among processors. The conventional way of utilizing bus architectures for inter IP core communication has many limitations. Mainly, it does not scalable well with increasing soft cores on single FPGAs. Next, it is tough to couple high computation and demanding communication of the MPSoC platform leading to expensive design flow with long design time. Network on chip have become only alternative to solve these problems.

Most of existing NoC offers and relay on a best effort service those are depends on packet switing technique. Examples of packet based NoCs are MANGO and Xpipes[3]. Another class of NoCsare based on circuit switching technique whose methodology is to fix the entire path from source node to the destination node before coming data from thesource node. PNoC and SPIN[4], based on circuit switching method. Todays multimedia based system demands predictable performance as node link between soft cores are tightly time constrained. For such multi-core systems, it is compulsory to provide guaranteed throughput service before run-time. To meet these constraints, link allocation should be done in advance during design flow time.

TDM based NoC provides guaranteed throughput where different time slots are used on the same link. One demerit of TDM is that router switching configuration need to be changed every time slot. This feature requires time slot tables that needs area and consume power in every router. Nostrum and AEthereal are based on TDM NoCs, those architectures has to maintain time slot tables. Spatial division multiplexing is best method where node links, which inter connect the routers are allocated to different links. Each link has flexible number of wires to assigned to them.Theserialised data sent from sender on the wires allocated and those are deserialised by the receiver before forwarding to the IP core. The main merit of SDM over other technique is that it removes the need of time slot tables thus power optimised but complexity is moved to the serializer and deserializer of network interface.

In this paper, we provide best methods to the above problems. We have proposed a novel design and modified architecture for network interface to handle the serializer and deserialiser complexity that is common in SDM based NoC[7]. A simple router with less complexity is proposed which uses lower area at the cost of routing flexibility. This mainly reduces the problem of reordering the data when data arrive at the destination Network Interface.Our design flow provides dynamically reconfiguring the NoC with different link setups during run-time. We have modeled VHDL code for SDM based NoC.We have connected microblazes in a MPSoC using modified SDM based NoC with Xilinx EDK and a working prototype has been implemented on a xilinx spartan6 FPGA SP605 Evaluation board(SP605). The softcoresmicroblazes were used to evaluate the dynamic reconfiguration of the NoC as well as to communicate data between each other.

II. MODIFIED SDM BASED NoC ARCHITECTURE

The proposed architecture has been modeled as dual layer structure where first layer is responsible for data transfer while the second layer is the responsible for configuring router links. The network topology is used for the architecture is mesh which is best for multimedia applications.Figure1 shows basic architecture of modified SDM based NoC.

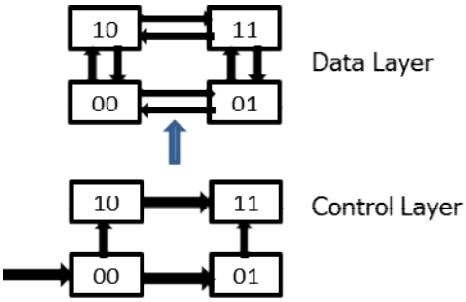

Figure 1: Modified SDM based NoC

A. Dual layer structure

The second layer is simple network mainly used to program the NoC as application demanded bandwidth. To program the NoC , links between router should be fixed as soft cores which requires data from other IP or soft cores. Number of programming byte required to program the NoC depends on size of mesh network(i.e 2x2 to maximum 7x7) that can mapped on to target FPGA. For each router there will be one soft IP which internally connected through network interface. Network interface in each IP serializes soft IP data from sender and deserializes at receiver side in order to receive data from source IP. All routers and soft IP with network will place in first layer which is responsible to transfer data from any source node to any destination node through router links. Designer fix the number of wire required to transfer data from source node to destination node as per bandwidth requirements which is programmable at design time.Figure 2 shows Dual layers in detail.

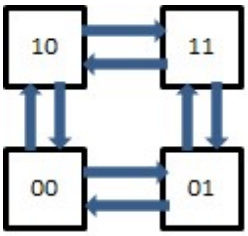

Figure 2(a) Data Layer

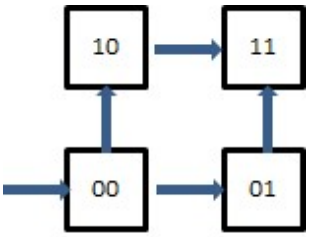

Figure 2(b) Control Layer

B. Modified Network Interface

The modified network interface for the spatial division multiplexing based network on chip has special control block that will be used to control in coming 32 bit data from different channels of soft IP cores. This intelligent control unit replaces multiple data distributors at transmitter side and multiple data collectors at receiver side with only one data distributor and one data collector. Proposed control unit can be used for fault tolerance to minimize faults at transmitter and receiver blocks of network interface. The modified network interface has many features, one of the feature is huge area saving that main problem in any Network on chip architectures and fault tolerance that is very demand for multi-core system-on-chip in embedded applications. We have modified 32 bit to 1 bit serializerwith intelligent control unit in network interface. Figure 3 shows Network Interface.

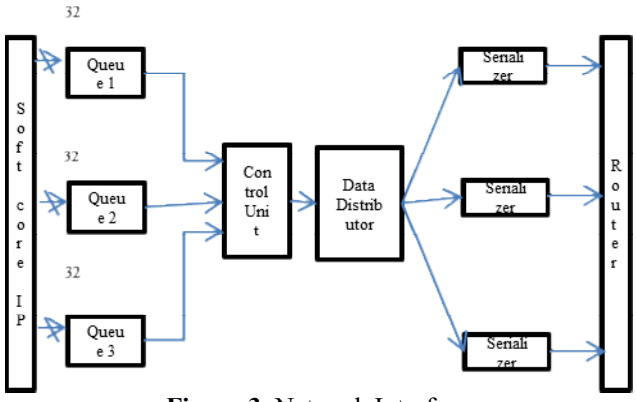

Figure 3. Network Interface

C. Router for modified SDM based NoC

We have targeted xilinx FPGA to implement SDM based NoC for MPSoC platform, so router architecture modified just like architecture of xilinx switch by avoiding unnecessary complex logic. In modified router for proposed network-on-chip has five port which includes north,south,east,west and local. Soft IP cores are connected through local port. From local port designer can send data to adjacent router through other four ports. This feature is very unique when compared with any other Network-on-chip architectures. Which provides more flexibility, scalability and huge area saving. Each port size can be design parameter which can be fixed at design time depending on application bandwidth demand.Figure4 shows router architecture in detail. Each side has one input port of size 8 bit, one output port of size 8 bit, one out allocated input port of size 3 bits and one out allocated input index port of size 3. The size of out allocated input size 3 bit because in this only 5 possible direction data can be sent from any side. The size of out allocated input index depends on size if input port and output port on each side.

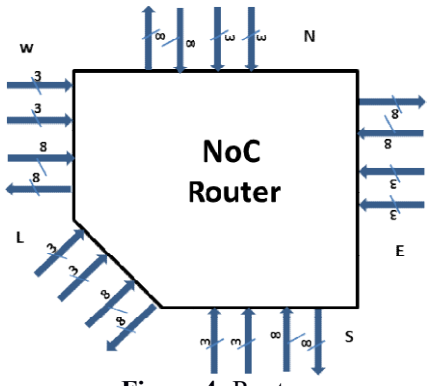

Figure 4: Router

III. RESULTS

A. Simulation Results

We have setup 2x2 NoC architecture with proposed blocks which are modeled using VHDL and simulated using xilinx ISE simulator ISIM. Figure shows network interface results and data sent from transmitter of network interface and data received from soft IP core into receiver of network interface. Figure also shows top level 2x2 NoC architecture results with all four routers.

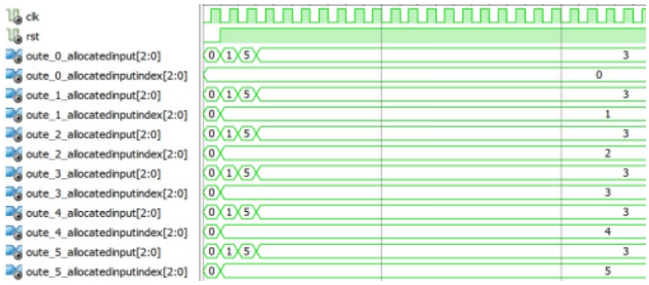

Figure 5. Simulation Results

B. Synthesis Results

For our experimental test setup 2x2 modified SDM based NoC for MPSoC platform synthesis reports are generated using xilinx synthesis tool XST. Figure shows synthesis report which has available resource on spartan6 FPGA and used for our test setup and percentage utilization of available resources. Our report concludes that area is optimized at network interface level and router side which can be compared with any other network-on-chip architectures for area optimization

Table : Synthesis Report

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	6062	54576	11%
Number of Slice LUTs	5257	27288	19%
Number of fully used LUT-FF pairs	2457	8862	27%
Number of bonded IOBs	288	296	97%
Number of BUFG/BUFGCTRLs	2	16	12%

C. Implementation Results

We have integrated proposed modified SDM based NoC for MpSoC platform with four microblaze soft xilinx IP RSIC cores and 9 Fast Simplex Links(FSL) using Xilinx Embedded Development Kit (EDK) 13.3 ISE design suite. Figure shows device utilization summary after implementation. Table I shows device utilization summary of proposed modified SDM based NoC.

Table I: Device Utilization Summary

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	1321	54576	2%
Number of Slice LUTs	1645	27288	6%
Number of fully used LUT-FF pairs	999	1967	50%
Number of bonded IOBs	103	296	34%
Number of BUFG/BUFGCTRLs	1	16	6%

IV. PERFORMANCE ANALYSIS

To analyze the performance of proposed NoC architectures on spartan6 FPGA we have selected some case studies which includes Advanced Encryption Standard(AES) algorithm, JPEG compression ,JPEG2000 compression and H263 video compression standards. We have evaluated the application programs on proposed NoC architecture and other well popular TDM based NoCs, SDM based NoCs,Shared bus architectures and Advanced eXtensible Interconnect (AXI) architecutres and compared. Our NoC architectures shows better results than other popular architectures in terms of area, power, execution time and reconfiguration time.

Table I: Device Utilization In Slices

Application	Proposed NoC architecture	SDM based NoC	TDM based NoC	PLB Shared bus	AXI architecture
AES	6000	6500	7250	6250	6450
JPEG	6300	7000	7780	6700	6900
JPEG2000	7000	7500	8300	7400	7600
H263	7900	8200	9000	8200	8500

Table II: Power Consumption

Application	Proposed NoC architecture	SDM based NoC	TDM based NoC	PLB Shared bus	AXI architecture
AES	200mW	250mW	300mW	400mW	390mW
JPEG	236mW	290mW	320mW	410mW	400mW
JPEG2000	300mW	360mW	390mW	490mW	480mW
H263	435mW	450mW	490mW	560mW	550mW

Table III: Execution Time Of Application On Test Architectures

Application	Proposed NoC architecture	SDM based NoC	TDM based NoC	PLB Shared bus	AXI architecture
AES	2s	4.5s	6s	59s	50s
JPEG	3s	6.3s	8s	90s	80s
JPEG2000	4s	7s	9s	120s	90s
H263	5s	8s	12s	200s	170s

V. CONCLUSION

In this paper, we have proposed a novel design and flexible network interface architecture for existing SDM based NoC to improve performance and provide guaranteed service for multimedia applications. This architecture saves huge area and required only 5% of existing architectures. In future, multiple applications can be evaluated concurrently on modified SDM based NoC to explore high scalability and performance.

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