COMPARATIVE ANALYSIS OF TECHNOLOGY ADVANCEMENT FROM SINGLE GATE TO MULTI-GATE MOSFET

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Abstract

Among the entire contender in modern microelectronics,DG-MOSFET is a front line runner in planar technology. Itsunique structure allows scaling the device at sub-nanometer region and mimicking the electrical characteristics of a MOSFET.Here simulation of NMOS, SOI-NMOS, and DG-NMOS is presentedand relative comparison among short channel characteristics ispresented.It has been seen that among all the above stated device, DG-MOSFET possess better immune to leakage current with betterDIBL, whereas SOI MOSFET have better driving capacity.

KeyWords:*SOI-MOSFET, DG-MOSFET, UTB, DIBL,SCEs*

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1. INTRODUCTION

In this modern world of technology, where unlimited functions need to be done using limited resources so a lot ofresources and work force is devoted to miniaturization of a transistor so-called “Scaling” [1] Scaling affects the density, speed, functionality, power dissi-pation and cost of an IC[2,3] According to Moore’s law transistor is considered as a fundamental element of a digital IC. Now a days scaling reachedpractical limits where it cannot retains the original characteristic due to the presence of short channel effects(SCEs).Due to SCEs devices power dissipation increases. The SCEscomes into picture in the presence if high electric field.This electric field lines are present between drain and source regions. As the device size reduced drain get closer tothe source and punch through effect is observed [4].Here electrostatic potential for NMOS, SOI-MOSFET, and DG-MOSFET for lightly doped channel is obtained. The three structure are compared for sub-threshold swing, Ion, Ioff,DIBL and channel potential. The paper is organized as follows: Section 2 discuss the device structures. Section 3 simulation of short channel characteristics of planar device such as NMOS, SOI-NMOS, DG-NMOS. The simulation of result and comparison of different device based on performance parameter havebeen given in Section 4 and finally Section 5 concludes thepaper. Paragraph comes content here. Paragraph comes content here. Paragraph comes content here.

2. DEVICE STRUCTURE

The schematic structure of NMOS, SOI-MOSFET, DG-MOSFET is shown in figure 1. In all structure gate length (Lg)

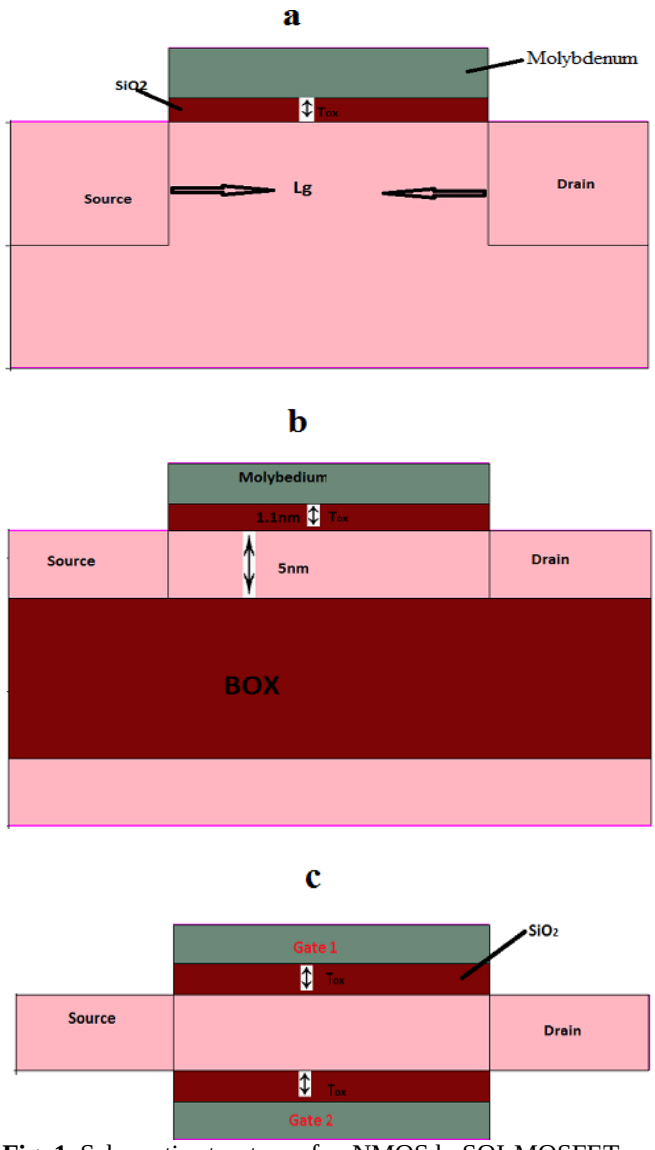

Fig. 1. Schematic structure of a. NMOS b. SOI-MOSFET c. DG-MOSFET, Respectively.

Table-I. Device Dimension and Doping Concentration

Oxide Thickness (Tox)	1.1nm
Gate Length (Lg)	22nm
Source/Drain Doping(ND)	5×10^{18}
Channel Doping (NA)	1×10^{15}

is fixed as 22nm.Width of channel is taken as 5nm in SOI-MOSFET and DG-MOSFET. Total width of device is 10nm.The Oxide thickness Tox=1.1nm (EOT) is taken. Molybdenumis used gate material.

3. SHORT CHANNEL CHARACTERISTICS

3.1 Sub-Threshold Characteristic

It is assumed that Id = 0 for Vgs<Vth but there is finite Current flow called Ioff current or sub threshold current. Id Decreases exponentially below Vth.It is one the main cause of static power dissipation.Fig. 2 shows Ion and Ioff of a different MOSFET. Ioncurrent is maximum in SOI MOSFET indicates maximumdriving capacity but it has also largest Ioff (sub thresholdcurrent). On the other, hand least sub threshold leakage currentfound in DG-MOSFET.

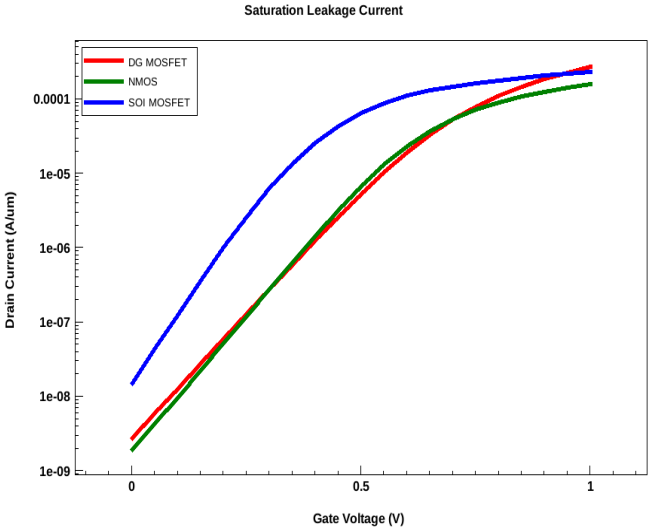

Fig. 2. Ion and Ioff current

3.2 Sub-Threshold Swing

It is change in gate voltage that must be applied in order to create one-decade increase in the output current. More sharp the slope, more quickly the device moves from ON to OFF state

$$\text{Sub-threshold Swing} = \frac{dVgs}{d\log Ids}$$

Fig. 3 shows sub-threshold swing of DG-MOSFET is greaterthan SOI-MOSFET but slightly greater than NMOS, so SOI-MOSFET takes more time to switch from ON state to OFF State. Delay in SOI MOSFET is largest. This is main problem faced by SOI-MOSFET. DG-MOSFET shows comparable sub-threshold swing with MOSFET.

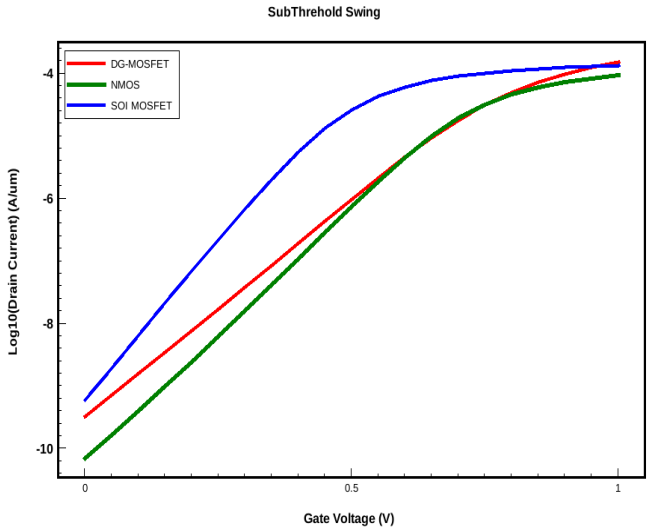

Fig. 3. Sub threshold Swing.

3.3 DIBL

Effective gate length reduces as Vds increases. Drain depletion region moves closer to source, resulting in significant field penetration from drain to source. Due to this penetration, potential barrier at source results in increase in drain current. This process called DIBL (Drain Induced Barrier Lowering)

$$\text{DIBL} = \frac{\delta Vt}{\delta Vds}$$

DIBL of NMOS is much larger which is expected to increase at lower gate length. Higher the DIBL higher the chance of device fails to go in off state. DIBL is least in DG-MOSFET, so it is more prominent candidate for further scaling.

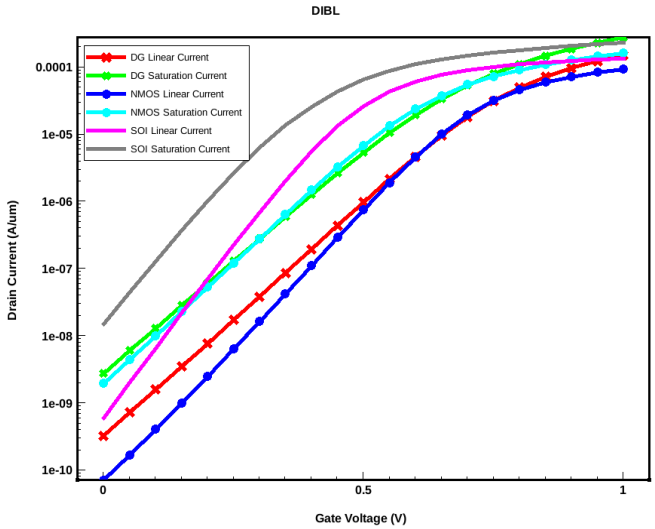

Fig. 4. DIBL

3.4 Electrostatic Potential

Electrostatic potential in lightly doped channel is obtained by solving 2D poisons equation:-

$$\frac{\partial^2\psi}{\partial x^2}+\frac{\partial^2\psi}{\partial y^2}+\frac{\partial^2\psi}{\partial z^2}=\frac{qN_a}{\epsilon si}$$

By solving above equation with appropriate boundary condition of device, we get potential inside channel region. Potential variation along length of devices is shown. It can be inferred from fig.5 that DG-MOSFET has greater channelControl compared to others. SOI-MOSFET and NMOS has relatively same control over channel.

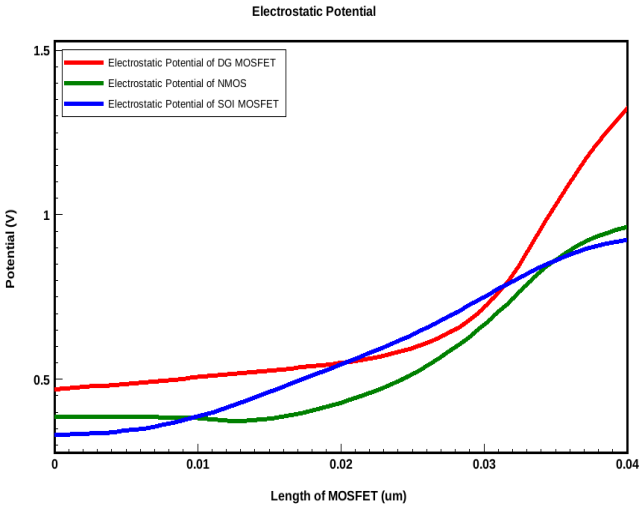

Fig. 5. Variation of Potential along Length of Device

4. RESULT AND DISCUSSION

All the structure are realized and plotted by using SENTAURUS TCAD. The comparison between different short channel effect are given below:- From Table II, DG-MOSFET andNMOS has comparable sub threshold swing. It is better toHave higher sub threshold swing so that the device quicklyswitches from on to off state or vice-versa. In short the device is fasterIoff current in DG-MOSFET is least indicates less leakage

Table II- Device dimension and doping concentration

Parameter	DG-MOSFET	SOI-MOSFET	NMOS
S.Swing (mV/dec)	127.2	96.3	139.4
DIBL	0.0422	0.133	0.166
Ion (A/um)	$1.312x10^{-4}$	$2.37x10^{-4}$	$1.6x10^{-4}$
Ioff (A/um)	$1.03x10^{-10}$	$1.53x10^{-9}$	$1.976x10^{-9}$

Current. Ion current in all device is relatively same, thus Ion To Ioff ratio is maximum in DG-MOSFET.
DIBL of DG-MOSFET is 0.0422, which is comparatively veryless than other both device. DIBL of NMOS is highest signifiesgreater chance of device failed to min off condition. HigherDIBL least possibility of device scaling, so DG-MOSFET ismore prominent candidate in planar technology for furtherscaling.

5. CONCLUSION

The simulation of SOI-NMOS, DG-MOSFET device has been studied. We found that DG-MOSFET has better controlover channel. It has comparable sub threshold swing and Ioncurrent to NMOS. In addition, least DIBL and Ioff current make itprominent candidate for further scaling.

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BIOGRAPHIES

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