AN AREA EFFICIENT DIGITAL DOWN CONVERTER USED IN 4G WIRELESS RECEIVERS

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Abstract

A Digital Down Converter (DDC) forms an integral part of wireless receivers. The major functional blocks of a DDC constitute a mixer, Numerically Controlled Oscillator (NCO) and an FIR filter chain. In this paper, an area efficient DDC has been designed and implemented. The designed architecture achieves 44.8% area efficiency, on comparing it with that of the existing methodology. The lesser the area required, the lesser will be the power consumption, thus making it environmental friendly.

Keywords: *DDC, Folded, Unfolded, Filter Chain, Area*

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I. INTRODUCTION

Communication is mainly classified into wired and wireless. The invention of wireless communication has been a boon to mankind. Information can now be transmitted from one place to another, without the use of a physical electrical medium. With the advances in wireless technology, information can be transmitted through a distance of few meters (Ex: Television remote control) to thousands of kilometers (Ex: Radio communication).

The wireless communication technology has evolved from the first generation (1G), which marks the beginning of the mobile cellular era; through the second and third generations (2G, 3G), where technologies such as GPRS, EDGE, GPS, GSM, video conferencing emerged; and now, to the fourth generation (4G), which provides advanced services such as IP telephony, cloud computing, high-definition mobile TV, etc.

When a signal is being transmitted over a wireless medium, it may be affected by Inter-Symbol Interference (ISI) which causes the signal to distort. In order to avoid this, signal scaling is performed. At the transmitter side, the signal is up scaled from baseband to intermediate frequency (IF) signal and transmitted. On the receiver side, the signal is transformed back from IF to baseband frequency. This down scaling operation is performed by a DDC.

In this paper, an efficient 4G Digital Down Converter has been designed and implemented. Simulation is performed in MATLAB to verify the functionality [1]. The design is then developed in VERILOG, simulated using the ModelSim simulator and then synthesized using the Xilinx Project Navigator.

The design of the filter chain forms an intricate part of the DDC in reducing the sampling rate and in performing low pass filtering to obtain the actual baseband spectrum [2]. The two widely known filters that can be used to design the filter chain are: the Finite Impulse Response (FIR) filter and the Infinite Impulse Response (IIR) filter. The IIR filters do not provide linear phase response and are not stable, since they are recursive in nature. They consume more power. On the other hand, the FIR filters, developed by Parks McClellan, are stable in nature, non-recursive and consume low power. They provide optimal filter coefficients using an indirect method. They provide linear phase response which implies that they have symmetrical coefficients. They are more suited for baseband, anti-aliasing and low pass filtering operations. Due to these advantages, FIR filters are used to design the filter chain of the DDC.

II. ARCHITECTURAL BLOCK DIAGRAM OF DIGITAL DOWN CONVERTER

A block diagram of the DDC is shown in Fig. 1. The major functional blocks constitute a mixer, an NCO and a filter chain [3]. Firstly, the received input signal is multiplied with the IF sine signal from the NCO. The output of the mixer is then processed through the filter chain, which performs low pass filtering to obtain the original baseband signal.

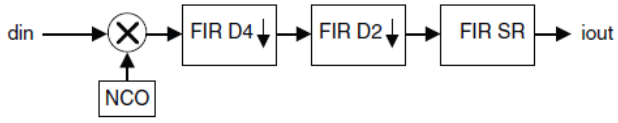

Fig. 1: Architectural block diagram of DDC

A. Design of NCO

The Numerically Controlled Oscillator has been implemented using the widely used, Look-up Table (LUT)

approach. The NCO produces a cosine signal having IF frequency. The mixer, upon mixing this signal with the received input signal, produces the baseband frequency signal, which is then fed to the filter chain.

B. Design of Filter Chain

The filter chain consists of three levels of filtering [3]. The first stage consists of a 35 tap FIR filter, followed by decimation by a factor of 4 (denoted as D4 in Fig. 1). The transition band for this filter is wide, i.e., it is not sharp. The second stage consists of a 63 tap filter, followed by decimation by a factor of 2 (denoted as D2 in Fig. 1). The transition band for this filter is moderate. The last stage contains a single rate 111 tap filter which provides a sharp transition band. The decimators are used to reduce the sampling rate.

III. FIR FILTER ARCHITECTURE

Let us consider an FIR filter with S filter taps. The existing architecture would require S number of multipliers to implement such a filter. This general purpose architecture is known as the "unfolded filter architecture". The proposed architecture, on the other hand, makes use of the symmetric property of the filter coefficients and provides a way to reduce the number of multipliers used. Thus, in a general case of an FIR filter with symmetrical coefficients, the number of multipliers required reduces to S/2, if S is even or ((S-1)/2) +1, if S is odd. This type of filter design is called the "folded filter architecture" [4]. An example of a 5 tap unfolded and folded FIR filter structure is as shown in Fig. 2.

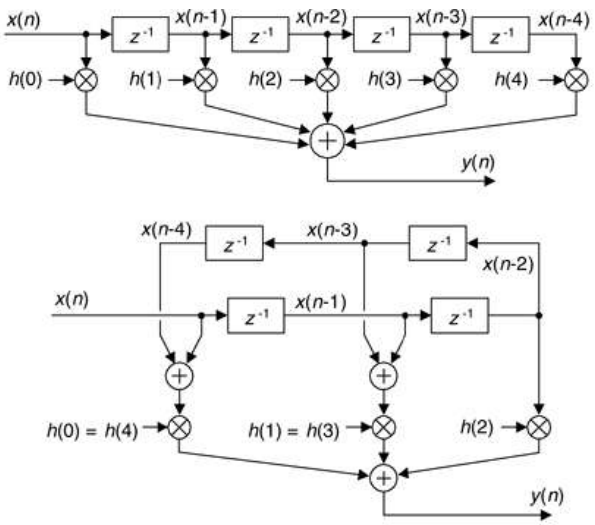

Fig. 2: Unfolded and Folded FIR structure

In this example, S = 5 multipliers are needed in the unfolded architecture, whereas only (S-1/2) +1 = 3 are needed for the folded. Multipliers are the ones that consume majority of the power and space. Each multiplier consists of around 200 full-adders. Thus, the unfolded architecture would require 5*200 = 1000 full-adders, while the folded architecture would just require 3*200 = 600 full-adders. This implies that the unfolded architecture has huge area requirement. The larger the on-chip area, the higher the power consumed. The folded architecture provides a way to reduce this area requirement by a significant amount. Lesser the area required, better the speed and lesser the power consumed.

IV. IMPLEMENTATION

The transmitter has been implemented as shown in Fig. 3. A message signal up scaled by performing interpolation. The interpolated signal is then mixed with the output of an NCO The resulting signal is the IF signal which is transmitted.

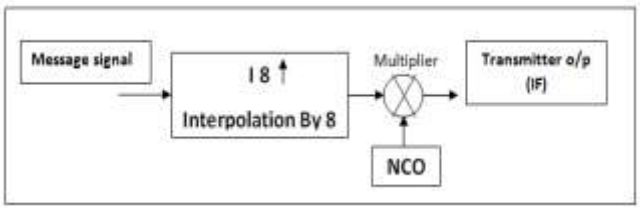

Fig. 3: Block diagram of transmitter

At the receiver side, the block diagram of the DDC that has been implemented is as shown in Fig. 4. The received IF signal is multiplied with the NCO output, and then the resulting signal is made to pass through the filter chain. The signal is passed through a 35 tap FIR filter, followed by decimation process by a rate 4. Next the signal is filtered by a 63 tap FIR filter, followed by decimation process by a rate 2. The resulting signal is then filtered by a 111 tap FIR filter to obtain the reveiver's output.

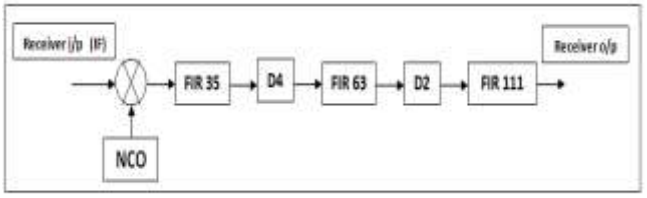

Fig. 4: Architectural block diagram of DDC at the receiver

The NCO has been implemented using the LUT approach. The filter chain has been implemented using both, the existing unfolded architecture and the proposed, folded architecture. The unfolded architecture makes use of a total number of 219 multipliers, which implies 219 * 200 = 43800 full adders. Whereas the folded architecture uses only 106 multipliers, i.e. 106 * 200 = 21200 full adders. This shows that the folded FIR architecture achieves reduction in area required by a significant amount.

V. SIMULATION AND RESULTS

The simulation of the DDC is performed in MATLAB to verify its functionality. The message signal considered at the transmitter and the IF signal to be transmitted, obtained by multiplying the interpolated message signal and the output of NCO are as shown in Fig. 5. The different stages of filtering: 35 tap, 63 tap and 111 tap, can be observed in Fig. 6 and 7.

Fig. 6 shows the output of the first 2 stages of filtering, where the transition from pass band to stop band is wide in the first stage and improves to a moderate transition band in

the second stage. A decimation operation is performed after each of these filtering operations to reduce the sampling rates. The output of the 35 tap filter is decimated by a factor of 4, i.e. every fourth sample is picked up and the rest are dropped. This decimated output is then fed into the 63 tap filtering stage, followed by decimation by a factor of 2, i.e. each alternate sample is picked up.

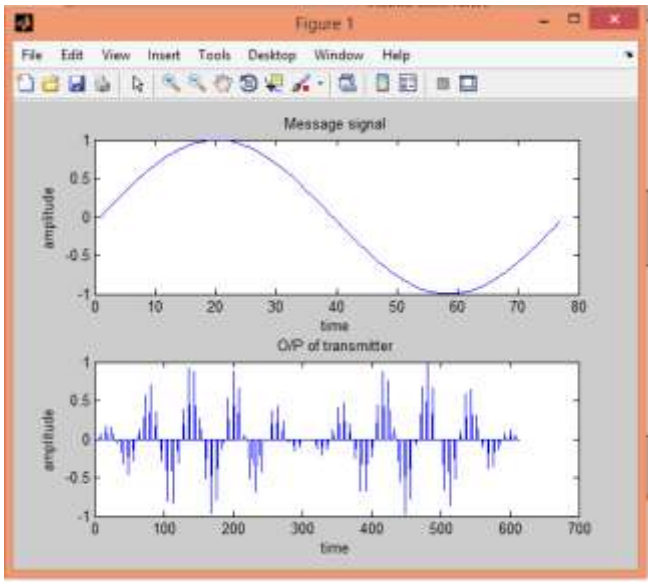

Fig. 5: Messgae signal and output of transmitter respectively

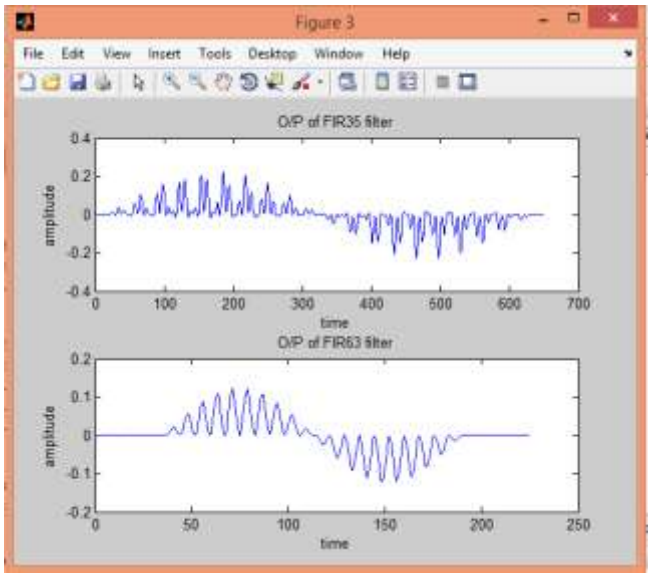

Fig. 6: Output of 35 tap and 63 tap filtering respectively

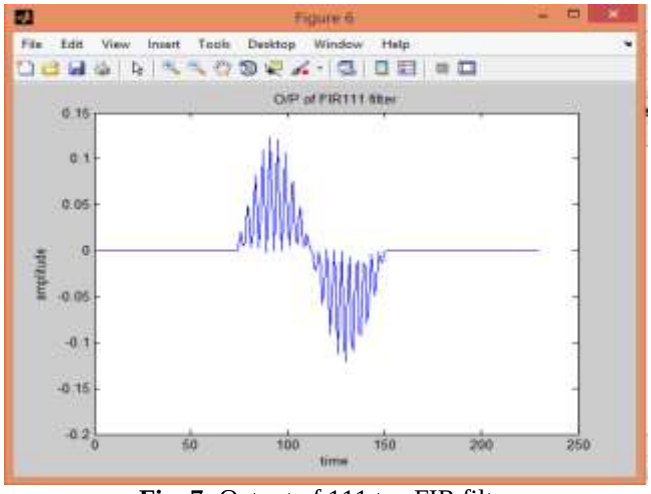

Fig. 7: Output of 111 tap FIR filter

Fig. 7 shows the output of the last stage of filtering, where the sharp transition band is obtained. This is the output of the DDC. This signal upon demodulation produces the original message signal that was transmitted.

The design is then developed in VERILOG using the ModelSim simulator. Both the unfolded and folded architectures are implemented. Upon synthesizing the two implementations using Xilinx Project Navigator, the results are obtained as follows:

- Disk Utilization Details:
  - Unfolded Architecture: Number of Slices: 55978 out of 2448 2286%
  - Folded Architecture: Number of Slices: 25097 out of 2448 1025%

On comparison of the results, we can see that the folded FIR architecture provides better area efficiency, compared to the existing architecture. The area requirement of folded architecture is less than that of the unfolded by 44.8%.

VI. CONCLUSION

An efficient 4G Digital Down Converter has been implemented using VERILOG Hardware Description Language. The filter chain of the DDC has been implemented using both, the existing architecture, i.e. unfolded architecture and the proposed folded architecture. On comparison of the results, it is seen that the folded FIR architecture achieves reduction in area requirement by 44.8% as compared to the unfolded architecture.

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