

IMAGE COMPRESSION ON FPGA AND TRANSFER USING ZIGBEE/I2C PROTOCOL

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Abstract

An Image is the pictorial representation of information which gives a visual perception. Processing of this image is an important parameter in its efficient transmission. Various techniques have been evolved in meeting this requirement. These techniques involve several hardware devices which can be a wired transmission or wireless transmission. This paper presents two of such techniques which can be implemented for compressed image transmission using Zigbee and I2C protocol.

Keywords—Wired transmission, Wireless transmission, Zigbee, I2C protocol, Image compression

1. INTRODUCTION

Image processing is performed for the efficient transmission of the information in a system. Efficiency can be determined in terms of noise free or error-free transmission, lossless transmission. The major components used in the proposed system include FPGA, Zigbee module and I2C protocol.

1.1 Image Compression

Compressing an image is one of the techniques used to reduce the size of an image in the case where a system operates with smaller size image and the requirement is to transmit the higher size images. In order to recover the original image decompression is to be performed where loss of information is to a less extent. DWT compression technique is performed to have a lossless transmission. The pixel values are reduced to a smaller number which can be done by down sampling in terms of rows and columns.

1.2 FPGA

FPGA boards are utilized to interface PC with the Zigbee module or implementing I2C protocol for the transmission of the image pixels of the compressed image. The compatibility with the type of FPGA is based on the module used for the transmission. Depending on the FPGA used, the software and the language used for programming differ.

1.3 Zigbee Module

This module consists of transmitter and receiver. The transmitter is connected at the sending side to FPGA and receiver at the receiving side where output is viewed. Communication between transmitter and the receiver is wireless.

1.4 I2C Protocol

The bi-directional two wire serial data bus protocol which manages the communication between the ICs within a

system and between the systems is called the Inter-IC bus or I²C bus. I²C prevents data corruption by performing a wired-AND operation as the I²C interface has open-drain or open-collector output.

2. HARDWARE IMPLEMENTATION

2.1 Using Zigbee Module

This section specifies implementation of image compression on FPGA and transmission using Zigbee module. The transmitter section is as shown in Fig 1.

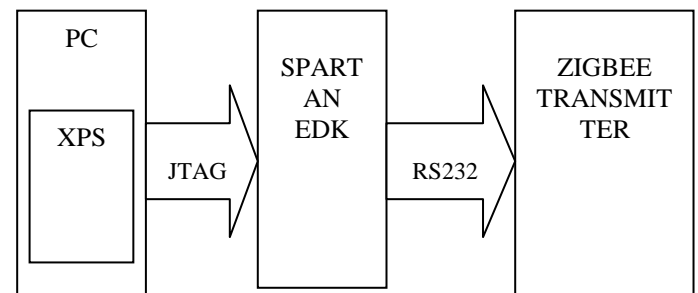


Fig 1 Transmitter

Spartan EDK FPGA kit is used which connects the PC to the zigbee transmitter. Xilinx Platform Studio is run on the PC which makes it compatible to the FPGA. The bit stream generated is downloaded on the SRAM of the board through JTAG. FPGA is connected to zigbee transmitter through RS232 connection. The image is taken from the PC and C file containing the program for the compression of image is added in the XPS software. The bit stream is generated and downloaded on to the kit.

The receiver is as depicted in Fig 2

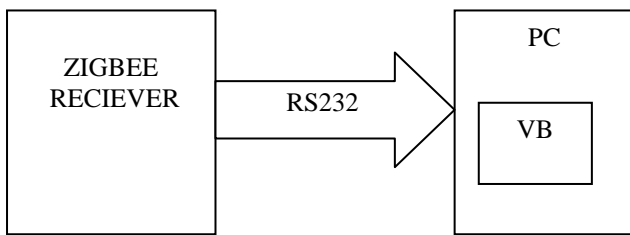


Fig 2 Receiver

The receiver block contains the Zigbee receiver and output PC. After downloading of the bit stream on to the kit, the transmission of the stream is done from the transmitter to Zigbee receiver. Using RS232, Zigbee receiver transmits the values to output PC where it is viewed using Visual basic.

2.2 Using I2C Protocol

The features of I2C protocol include:

- It requires only two bus lines; a serial data line (SDA) and a serial clock line (SCL).
- Each device connected to the bus is software addressable by a unique address and simple master/slave relationships exist at all times; masters can operate as master-transmitters or as master-receivers.
- multi-master bus including collision detection and arbitration to prevent data corruption if two or more masters simultaneously initiate data transfer.
- Serial, 8-bit oriented, bi-directional data transfers can be made at up to 100 kbit/s in the Standard-mode, to 400 kbit/s in the Fast-mode, to 1 Mbit/s in Fast-mode Plus, or to 3.4 Mbit/s in the High-speed mode.
- Serial, 8-bit oriented, unidirectional data transfers up to 5 Mbit/s in Ultra Fast-mode.

The blocks used in implementing the I2C protocol using FPGA is as shown in Fig 3

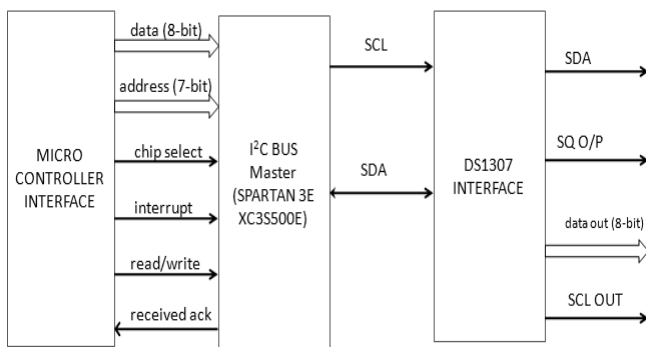


Fig 3 I2C protocol on FPGA

FPGA used which acts as I2C Bus master is Spartan 3E XC3S500E. The data bits and the address bits are provided by microcontroller interface where address is for specifying the unique address of the device to which the output should be received. The transmission is carried on using the 'START' and 'STOP' conditions depending on the SCL and

SDA of I2C protocol specification. The 'START' and 'STOP' conditions are as shown in Fig 4 and Fig 5 respectively.

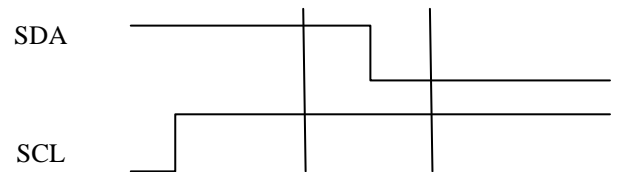


Fig 4 'START' sequence

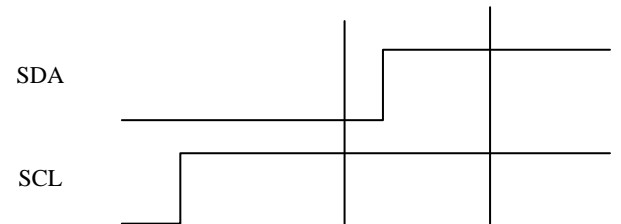


Fig 5 'STOP' sequence

The transmission of the data bits is done when START sequence is initiated. Depending on the address provided by the microcontroller, it sends the data to that slave having the specified address. This process is continued till the STOP condition is activated. Using the R/W, reading or writing of the information is done. The image compression coding is done on FPGA using VHDL programming and bit streams are generated which are received at the output using the DS1307 interface. The complete data transfer is as shown in Fig 6.

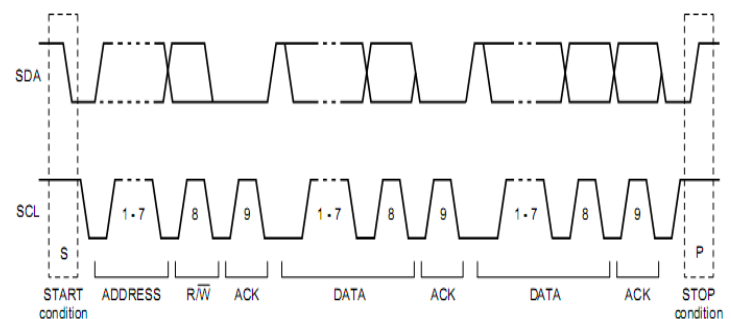


Fig 6 Complete data transfer

3. SPECIFICATIONS

The implementation of the image processing techniques using the Zigbee module and I2C protocol include the parameter of efficiency. The efficiency with which the transmission is completed depends on the specifications of the module or technique employed. There are advantages and disadvantages corresponding to the methodology used.

These specifications include special characteristic related to the process carried on or method incorporated in executing the procedure.

3.1 Zigbee Module versus I2C Protocol

The specifications of the two methodologies are listed as in Table 1.

Table 1 Specifications

Specification	Zigbee module	I2C Protocol
Transmission parameters	Separate transmitter and receiver sections	SDA and SCL signals
Type of transmission	Wireless	Wired
Range	Up to 50kms of distance	6 meters or 20 feet distance
Module	Wireless network with antenna mounted on it	Bus
Peripherals	Single transmitter and receiver are sufficient for the transmission	Several devices can be interfaced using the bus
Supply voltage	3.3 to 3.6 V	Input reference levels are set as 30% and 70% of VDD; VIL is $0.3V_{DD}$ and VIH is $0.7V_{DD}$
Interfacing unit	RS232	Microcontroller and DS1307
Data rate	250 kbps	The data on the SDA line must be stable during the HIGH period of the clock.
Transmission operating parameter	Transmission is performed at an operating frequency of 2.4 GHz	Transmission depends on START and STOP conditions.
Data transfer format	Image transmission done in the form of pixel values	Done in bytes of data where each byte has 8 bits
Supporting network topology	Point-to-point, Point-to-multipoint & Peer-to-peer	Master – slave connectivity
Transmission mode	16 Direct Sequence Channels	Depends on the speed of the bus

3.2 Limitations

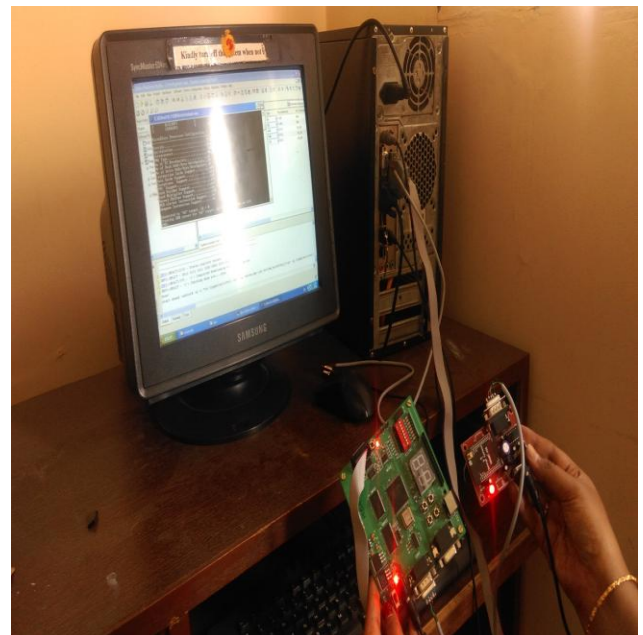
Every method that is considered has both pros and cons in its implementation. The proposed methods in the paper also have few limitations in the implementing process. Few such limitations are as shown in Table 2.

Table 2 Limitations

Zigbee module	I2C Protocol
<ul style="list-style-type: none"> Limited pixel values can be transmitted Changes with the change in the antenna specifications 	<ul style="list-style-type: none"> 7 bits are insufficient to prevent collision between addresses assignment of slave addresses is one weakness of I²C

4. RESULTS

The Zigbee transmitter with FPGA board is as shown in Fig 7. Fig 8 shows Zigbee receiver

**Fig 7** Sparten-3E kit with Zigbee transmitter

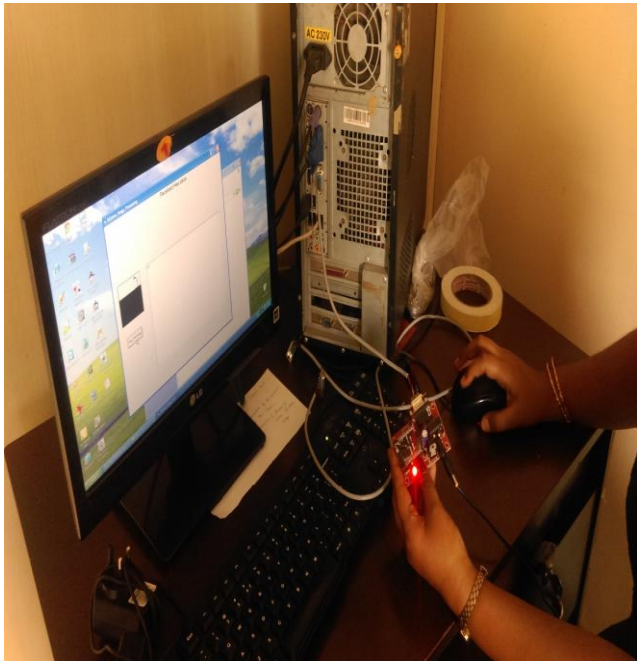


Fig 8 Zigbee Receiver

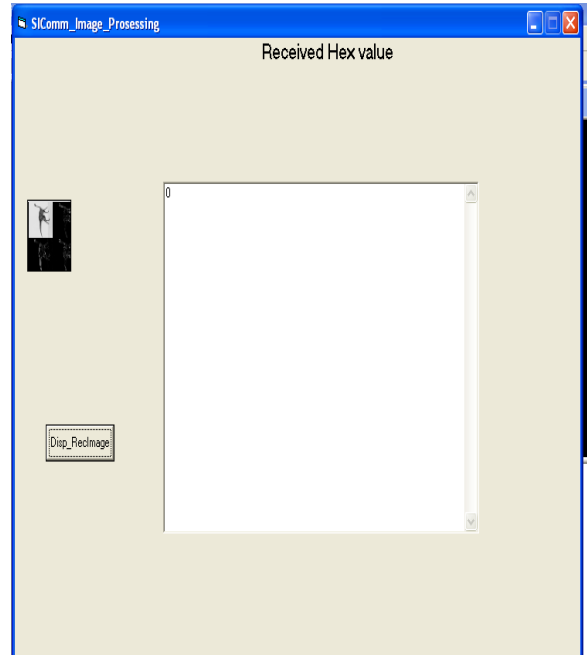


Fig 10 Output window

The output window is taken at the receiver using visual basic on the system. The input image taken is as shown in Fig 9 and the output window is depicted in Fig 10 which contains the compressed image.

Using I2C protocol, simulation results are taken with respect to the master and slave bus. The master transmitter is as given in Fig 11. Master receiver is depicted in Fig 12.

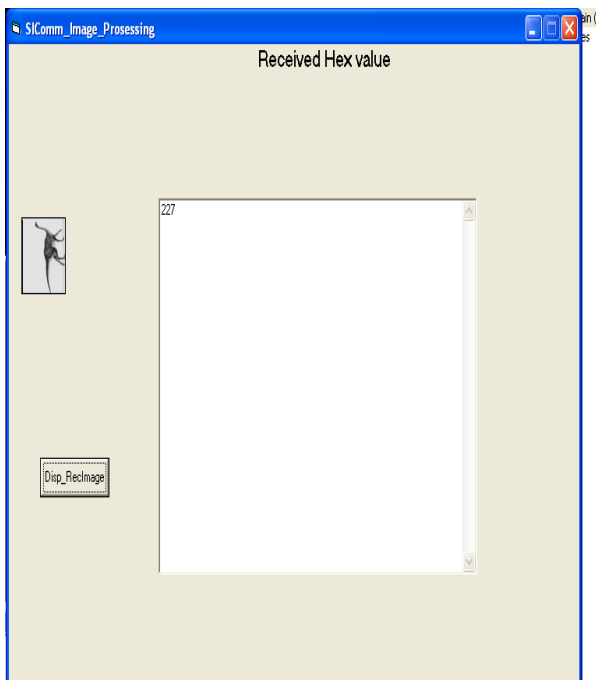


Fig 9 Input window

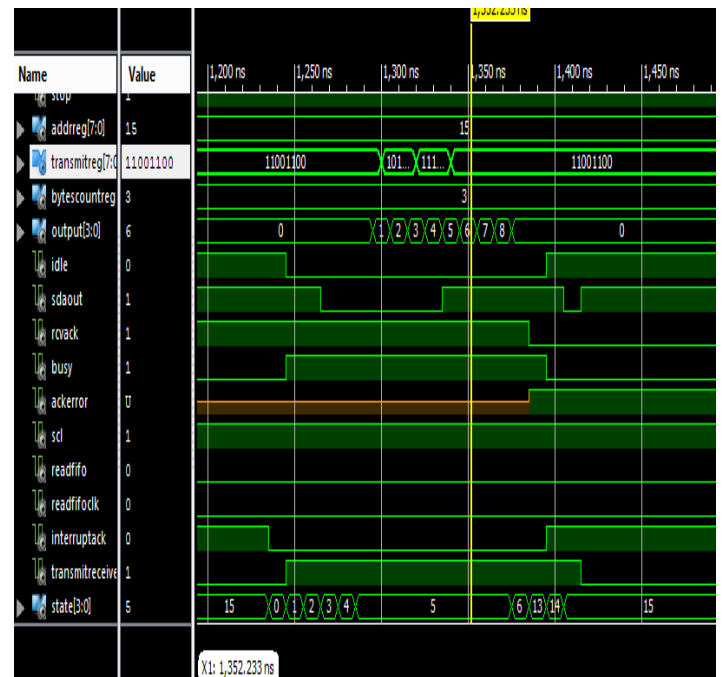


Fig 11 Master transmitter

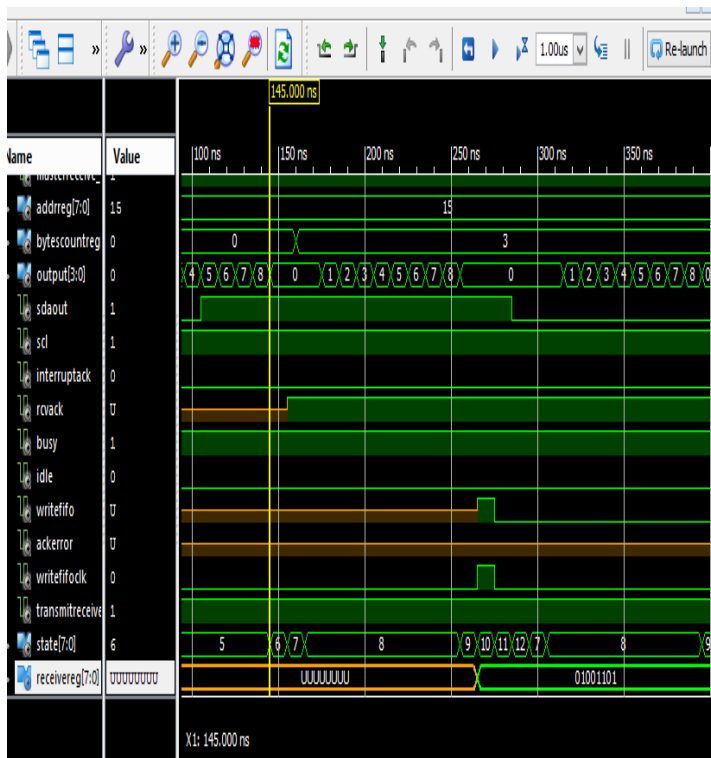


Fig 12 Master Receiver

5. CONCLUSION

The work proposed in the paper deals with the modules used in transmission of information using FPGA. Zigbee is a wireless network in which the transmitter and receiver are connected wirelessly whereas IC protocol uses set of protocols which defines the signals on which the transmission is carried on. I2C uses wired transmission using bus. Several devices can be connected to this bus and simultaneous transmission can be performed. Both these differ in speed and efficiency in transmission.

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