IMPLEMENTATION OF ARITHEMATIC OPERATIONS USING VEDIC MATHEMATICS

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Abstract

Vedic maths is the ancient Indian mathematics, it has 16 sutras for the calculations. These sutras can be used to solve very complex equation and operations. This paper seeks to present an integrated approach to implement the ALU using Vedic methods wherein the sutras are chosen and implemented for performing the basic operations like addition, subtraction, multiplication and logical operations. Sutras from vedic mathematics are selected according to the operations being performed and the verilog code is written and simulated for their implementation. The logical proof and explanation for the sutra's application is given in detail. These sutras are completely based on logical and rational reasoning. The sutras used in this paper for implementation of above mentioned operations are all for general case. The timing report is generated showing minimum period, input arrival time before clock, maximum output required time after clock and maximum combinational path delay.

Keywords— *Ekadhika, Sankalana, Ekanyuna, Purak, Vyavakalana, Urdhvatriyagbhyam*

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I. INTRODUCTION

Veda is a Sanskrit word derived from the root vid which means to know without limit. Swami Bharati Krishna Tirtha (1884-1960), former Jagadguru Sankaracharya of Puri culled a set of 16 sutras (aphorisms) and 13 sub-sutras (corolllories) from the Atharva veda. He developed methods and techniques for amplifying the principles contained in the aphorisms and their corollaries and called it vedic mathematics.

The basic mathematical operations are addition and subtraction which can further be used to implement multiplication and division respectively. Faster the addition/ subtraction higher will be the speed of the unit designed. For the same purpose, the carry save addition technique has been extensively used.

There are many other adders which provide other advantages like lower area overhead, eg: carry select adder. Most of the mathematical operations involve multiplication which is again all about adding the partial products. There are many multipliers used to meet the high speed criteria like Wallace tree multiplier and booth array multiplier.

In algorithmic and structural levels, many multiplication techniques have been developed to enhance the efficiency of multiplier which include the reduction of partial products or the different methods of addition of partial products, but the principle of multiplication behind all the methods is same.

2. IMPLEMENTATION LOGIC

Addition:

Addition is implemented using Ekadhika and Sankalana. These sutras are explained as follows:
a) Ekadhika means 'one more'
Eg: Ekadhika of 0 is 1
Ekadhika of 1 is 2

_ _ _ _ _ _ _ _ _ _ _
Ekadhika of 23 is 24

_ _ _ _ _ _ _ _ _ _ _
Ekadhika of 364 is 365_ _ _

b) Sankalana means 'addition'

Eg: 315 + 315 = 630.

Subtraction

Subtraction can be implemented using Ekanyuna, Purak, Vyavakalana and Ekadhika. This is explained as follows:

a) Ekanyuna means 'one less'

Eg: one less than 9 is 8.

b) Purak means 'complement'

Eg: complement of 1= 10-1= 9.

c) Vyavakalana means 'subtraction'

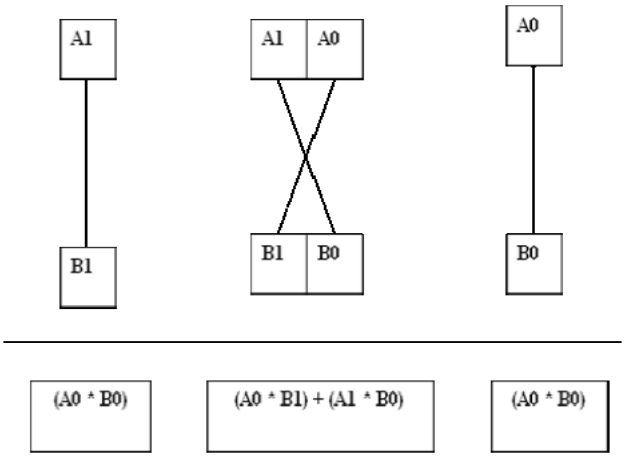
Eg: 315-100 = 215.

Subtraction can be directly performed as shown in Vyavakalana. But in binary subtraction, the second number's two's complement must be taken that is firstly complement second number using Purak and then add one to it using Ekadhika and then add the first number to two's complement of the second number using Sankalana.

Multiplication:

Multiplication is implemented using Urdhva triyagbhyam[2] sutra which is as follows:

Consider two numbers A and B which are two bits wide and are represented as A1A0 and B1B0. The multiplication is shown schematically below:



Logical Operations:

Consider two numbers A and B which are two bits wide, represented as A1A0 and B1B0. The operations are performed as follows:

AND logic

A AND B = {(A1 & B1), (A0 & B0)}

OR logic

A OR B = {(A1 | B1), (A0 | B0)}

NOT logic

NOT A = {~ (A1), ~ (A0)}

NAND logic

A NAND B = {~ (A1 & B1), ~ (A0 & B0)}

NOR logic

A NOR B = {~ (A1 | B1), ~ (A0 | B0)}

XOR logic

A XOR B = {(A1 ^ B1), (A0 ^ B0)}

XNOR logic

A XNOR B = {~ (A1 ^ B1), ~ (A0 ^ B0)}

3. OPERATION TABLE

Consider two inputs A and B, then the arithmetic operations performed on them are given as follows:

Operation	Description
Addition	A+B
Subtraction	A-B
Multiplication	A*B
AND	A&B
OR	A|B
NOT	~A or ~B
NAND	~(A&B)
NOR	~(A|B)
XOR	A^B
XNOR	~(A^B)

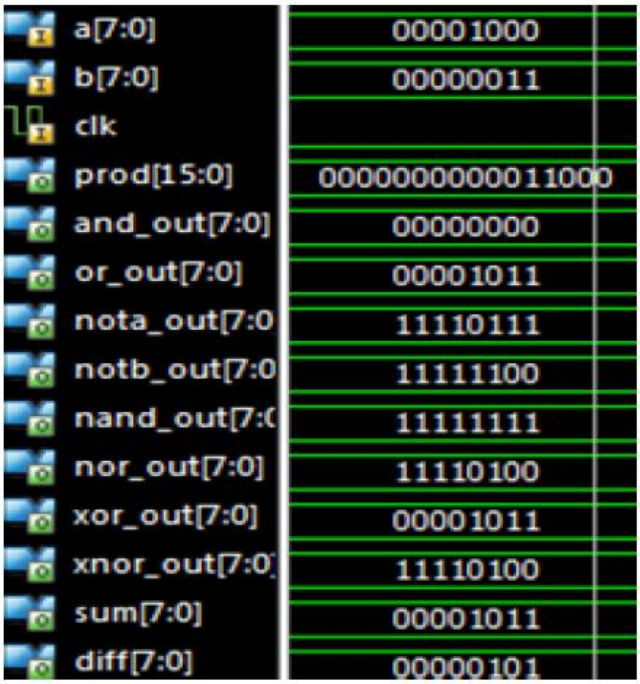
4. QUANTITATIVE RESULTS

After synthesizing and implementation of the design described above following timing report is obtained:

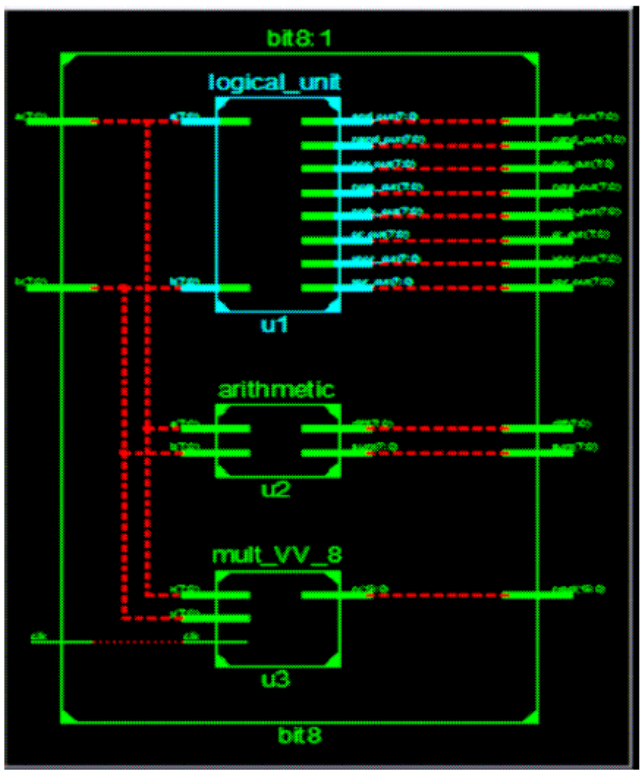
- Minimum period: **1.751ns.**
- Minimum input arrival time before clock: **5.075ns.**
- Maximum output required time after clock: **2.775ns.**
- Maximum combinational path delay: **5.853ns.**

5. SYNTHESIS AND SIMULATION RESULTS

5.1 Simulation Waveform



5.2 RTL Schematic



6. CONCLUSION

The vedic mathematics based methods are found to be very effective and are also considered to be faster ones compared to traditional methods of multiplication. These faster methods when implemented in DSPs result in faster units. Application of sutras proves to save the time and effort required to get the final result. Until one is perfect with the sutras and their applicable logic then these methods will become much easier for implementation. As the quantitative results show, the maximum combinational path delay for 8 bit design is 5.853ns. Further reduction in the delay can be achieved if a better adder structure for the partial product's addition is used.

REFERENCES

[1]. "A Novel Approach to Design High Speed Arithmetic Logic Unit Based On Ancient Vedic Multiplication Technique", Mr. Abhishek Gupta, Mr. Utsav Malviya, Prof. Vinod Kapse, International Journal of Modern Engineering Research (IJMER), Vol.2, Issue.4, July-Aug 2012 pp-2695-2698.
[2]. "Vedic mathematics" by Swami Bharati Krishna Tirtha, Vasudeva Sharana Agrawala Motilal Banarsidass, 1992.
[3]. "The power of vedic maths" by Atul Gupta.
[4]. "Design of high speed vedic multiplier using vedic mathematics techniques", G.Ganesh Kumar, V. Charishma, international journal of scientific and research publications, Volume 2, Issue 3, March 2012, ISSN 2250-3153.
[5]. www.xilinx.com
[6]. http://vedicmathsindia.blogspot.in