A NOVEL SDR TRANS-RECEIVER ARCHITECTURE FOR COMMUNICATION SYSTEMS ON FPGA

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Abstract

Usage of Software-Defined Radio (SDR) in digital communication systems can easily cater to sophisticated coding and modulation techniques, to meet the ever-increasing requirements of the wireless communication industry. Future generation of wireless communications will meet the requirements of Software Radio technology as it would provide the state-of-art design to complex radio designs. Software-defined radios are configurable devices in which the components can be reprogrammed to emulate various functionalities like data rate, modulation, filtering etc. Field programmable architectures provide a suitable platform to achieve such run-time reconfigurations of the components of the radio. The proposed design is implemented in SPARTAN3 FPGA by using Xilinx ISE 13.4 and verilog and simulated in modelsim 6.3f. The Chipscope pro Analyzer is used to view the execution results of FPGA.

Keywords—*Qudrature PhaseShift Keying, Direct freqency Synthesis (DFS), Raised Root Cosine (RRC), Low Pass Filter (LPF), Xilinx*

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1. INTRODUCTION

SDR is a process in which the components like baseband signal, carrier frequency, signal bandwidth, modulation; filtering, transmitter and receiver are implemented by software. Currently with the existing technology and developmental tools, SDR is able to implement complex communication systems comprising of many waveforms at many frequencies.

The basic notion behind is to seek the feasibility of getting the software as close to the antenna as possible, thus solving hardware problems by software. The advantage of this approach is that the equipment is more versatile and cost-effective. This paper illustrates the design and implementation of low frequency trans-receiver based on SDR legacy .Communication systems realized with

Application specific chips and system on chips like ASICs don't have sufficient programming capability and its functionality is very difficult to be changed or improved in the product development process.

Therefore, these chips are not suitable to the situation where the parameters are to be changed frequently. The low frequency trans-receiver based on FPGA provides ample flexibility in implementation and simple to upgrade. This practical approach has been adapted to implement the low frequency trans-receiver. Similarly, DFS is relatively a new technology of Frequency Synthesis and is gaining popularity as a method of generating sinusoidal signals and modulated signals in digital systems.

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2. BACKGROUND

Software defined radios constitutes a versatile platform for wireless communication solutions like cellular systems, global positioning systems, and military grade communications. The terminology of hybrid solution is also applicable to SDR approach as it applies to any wireless communication system implemented on Field Programmable Gate Array (FPGA) in conjunction with requisite RF system. The SDR is an emerging class of very cost effective, low power system since all hardware is physically programmed using software, re-design and reuse becomes relatively simple. Say, in case of any change in the requirements / specifications, the SDR is reprogrammed, updated and loaded back onto the FPGA, saving both cost and time instead of discarding old hardware.

The SDR is also emerging as a popular platform to achieve high quality communication by reconfiguring the radio modules without a need for expensive broadcasting equipment.

In addition to low cost, the SDR provides high processing capability, which means configurable higher data rates and modulation techniques. For such reasons, SDR is a rapidly advancing and expanding methodology, crossing all frontiers, a breakthrough in digital communication system design and implementation. Quadrature phase shift keying (QPSK) is a digital modulation scheme where each symbol is represented by a pair of bits, increasing data rate by a factor of two in a given bandwidth. Higher modulation schemes such as 8PSK and 16PSK sends three / four of bits per symbol, increasing data rates even further. A typical concern in wireless communication using QPSK modulation is carrier synchronization at the receiver and hence requires a Phase Lock Loop -based carrier recovery technique at the receiver.

2.1 QPSK Theory

Block Diagram

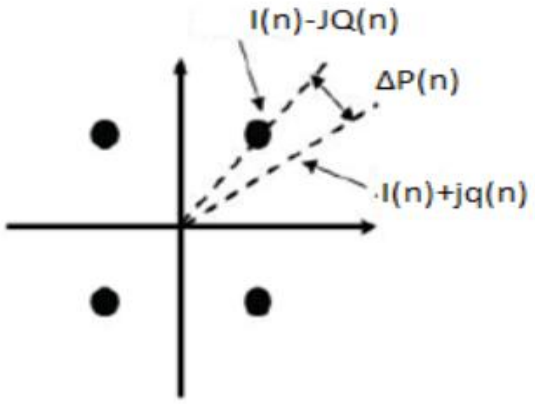

Fig 1

With QPSK, the binary data is converted into 2-bit symbols I, Q which are then used to phase modulate the carrier. Since four combinations containing 2 bits are possible from binary information (logical 1s and 0s), the carrier phase can be shifted to one of the four states and transmitted. The received signal is demodulated and the decoded data can be represented as a constellation diagram on an x-y plane in terms of symbols.

Fig 1 illustrates the possible symbols at 45, 135, 225 and 315 degrees respectively. Each symbol in the constellation represents two bits of information that are decoded based on their position in the constellation Frequencies.

The basic notion behind is to seek the feasibility of getting the software as close to the antenna as possible, thus solving hardware problems by software. The advantage of this approach is that the equipment is more versatile and cost-effective. This paper illustrates the design and implementation of low frequency trans-receiver based on SDR legacy.

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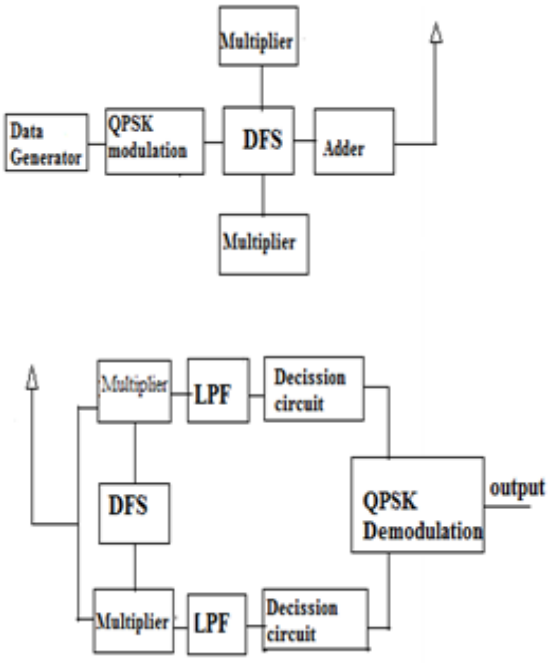

Fig. 2 QPSK Transmitter-Receiver scheme

Fig.3 Schematic of Low Frequency Trans-Receiver

The low frequency trans-receiver design is illustrated in Figure 3. A Pseudo-Random sequence of 32 bits at the rate of 50 KHz is converted from serial to parallel using a demultiplexer to get the In-phase (I) and Quadrature-phase (Q) components and fed to Unipolar to bipolar converter. The respective NRZ streams are shaped using raised cosine filters (roll off = 0.5) then multiplied with cosine and sine Carriers of 1MHz and added to give the modulated signal for transmission. As QPSK modulation requires 2 bits to effect phase changes, the symbol rate becomes 25KHz. The received signal is demodulated by multiplying it with the 1 MHz Carrier, filtered, and given to a decision circuit multiplexer and down sampled to retrieve the demodulated data.

2.2 Specification:

Hardware Requirement Specification:

- Minimum Intel Pentium IV Processor
- Primary memory: -2 GB RAM
- Spartan III FPGA
- Xilinx Spartan III FPGA development board
- JTAG cable, Power supply

Software Requirement Specification:

- Operating System: Windows XP with SP2
- Synthesis Tool: Xilinx 12.2.
- Simulation Tool: Modelsim6.3c.
- Language: Verilog

Here **Spartan 3** tools will use to work on this project, it has the operating speed of 100MHZ on board, and it also has soft processor **Micro Blaze.** And I working on tools like **Xilinx ISE 13.4** and also work on simulation software **ModelSim6.3c.**

3. PROJECT METHODOLOGY

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Block Diagram:

Design of SDR trans-receiver architecture is proposed which uses in digital communication system.

Logic Design:

In this project logic design will be use to transmitter includes generator, multipliers and adders mapping designs and for receiver includes demapping, filters decision circuits and multipliers.

Verilog:

To work on this project Verilog language will use for the implementation of Design of SDR trans-receiver architecture in Xilinx ISE 13.4.

Synthesis:

After combining, testing has to do, i.e whether the program is working properly or not, if yes it will continue with next process else it has to rewrite or correct. After correction again test the program, if its successfully working then it will be implement.

Implementation:

All the process till testing will implement in this step.

Physical Dumping:

In this step implementation of the project will dump into the FPGA.

Physical Testing:

Finally the project will be test in the FPGA kit.

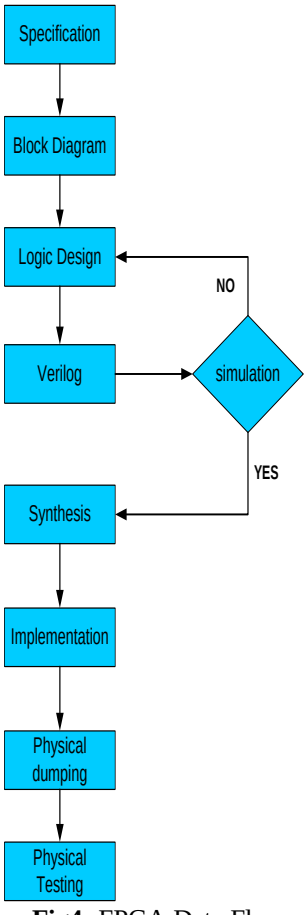

Fig4: FPGA Data Flow

Above flow graph shows the method or procedure of the project, and each block present in the flow graph is briefly explained above

4. RESULTS AND DISCUSSION

In addition to low cost, the SDR provides high processing capability, which means configurable higher data rates and modulation techniques. For such reasons, SDR is a rapidly advancing and expanding methodology, crossing all frontiers, a breakthrough in digital communication system design and implementation.

Increasing data rates even further. A typical concern in wireless communication using QPSK modulation is carrier synchronization at the receiver and hence requires a Phase Lock Loop -based carrier recovery technique at the receiver.

5. CONCLUSION

SDR of low frequency trans-receiver was successfully implemented on a single FPGA chip. The measured results show that transmitter input matches with the receiver output. Modelsim simulations were also carried out to gain insight to the problem at hand. The overall exercise is an excellent example of implementing a hardware problem in software. Also it provides a low cost, low power solution. FPGA implementation may further provide flexibility in customizing the design for different data rates, Modulation types, Carrier Frequency, Filter types etc making the design effectively reconfigurable. Future work would involve usage of error coding / decoding, carrier recovery algorithms, M-ry PSK modulation etc to deliver a scalable customized design.

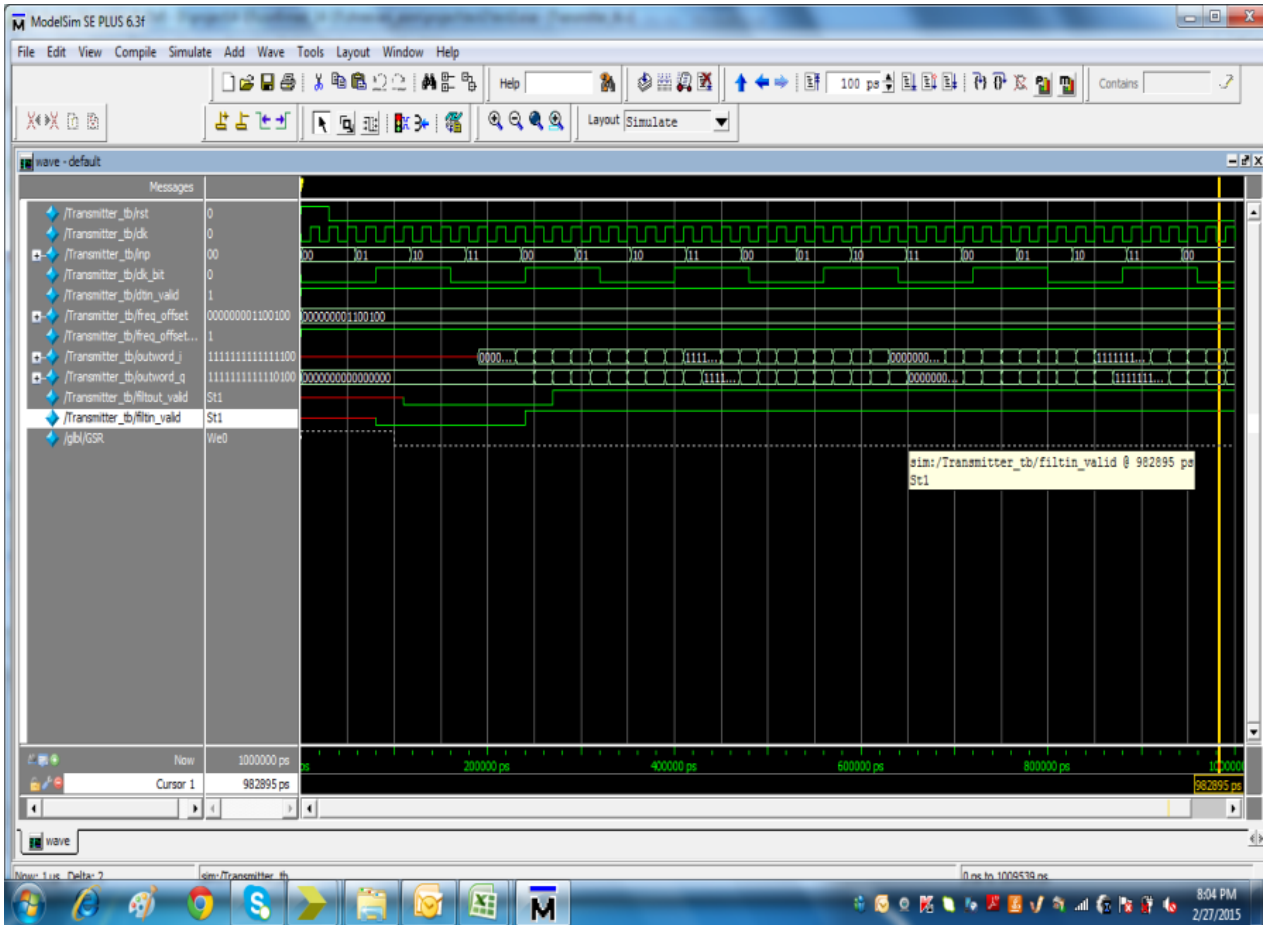

Fig 5: Transmitter Waveform

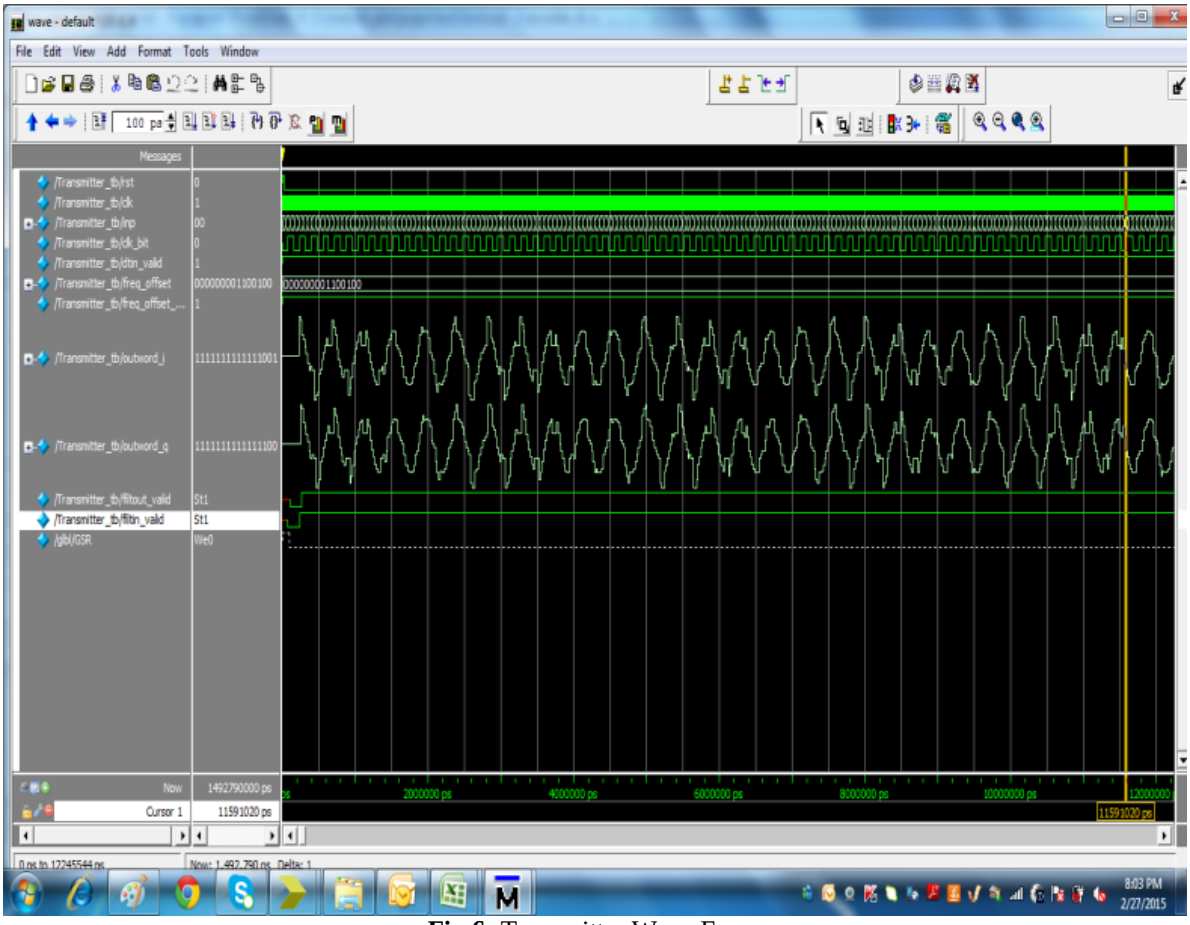

Fig 6: Transmitter Wave Form

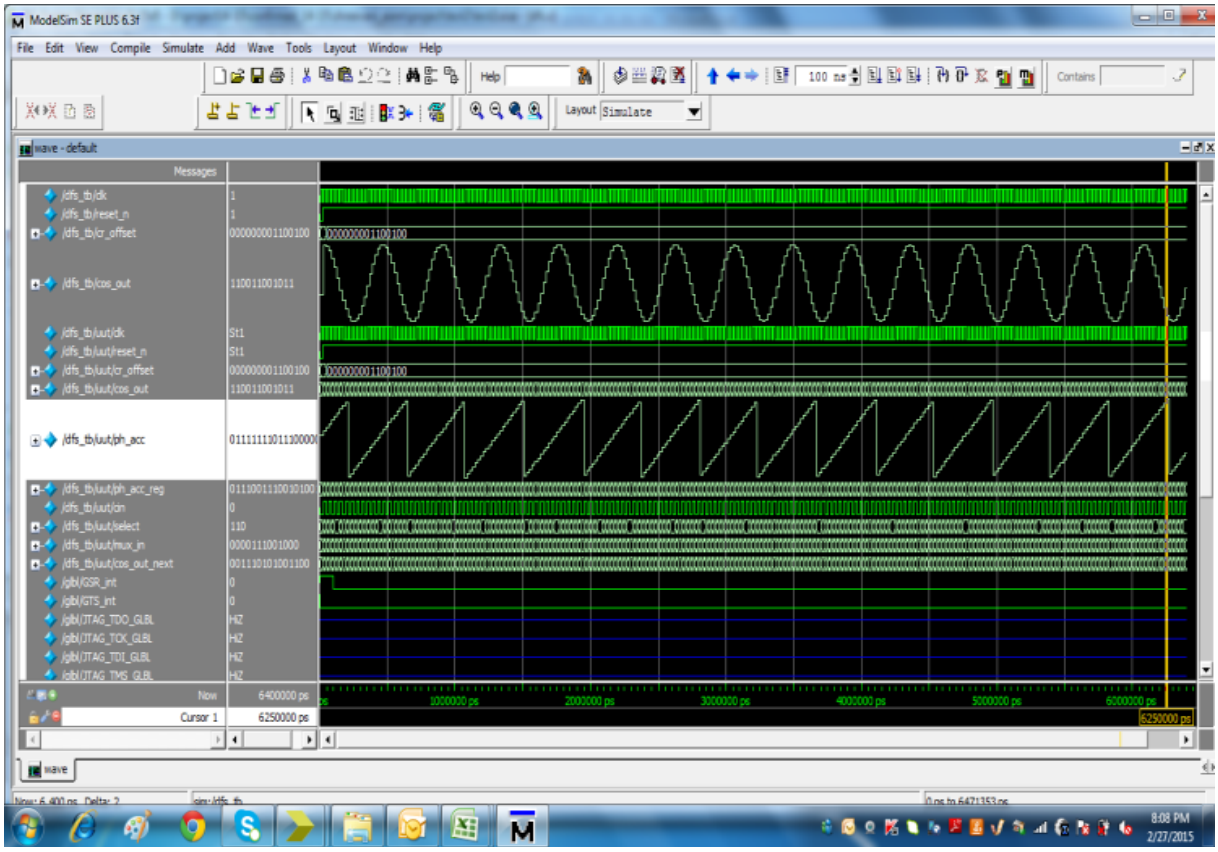

Fig 7 .dfs output

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BIOGRAPHIES

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