THE DESIGN & SIMULATION OF LOW NOISE AMPLIFIER FOR 1 -2.8 GHZ USING ALN SUBSTRATE

Rajesh V. Navagare[1], Kishor G. Sawarkar[2]

[1]*Dept. Electronics & Telecomm., MCT's RGIT, Mumbai, India*
[2]*Research Scholar at MCT's RGIT, MCT's RGIT, Mumbai University, Mumbai, India*

Abstract

In this paper, we have designed low noise amplifier using 2 stage Cascade topology. We have focused on intermediate matching network design of amplifier for low noise figure and selection of transistor PHEMT is based on noise figure as well as quiescent point required for 0 grid voltage so that amplifier will need only single DC supply i.e. Vdd. Depends upon different topologies used for LNA design with wide band requirement, we chose cascaded topology for good gain with low noise amplifier and optimized for greater bandwidth.

Practical inductors are bulky as well as counter intuitive elements for high frequency as they behave as capacitors and to reduce S11. Several windings in inductors make them resistive which increases noise by 0.2-0.4 dB. So we proposed inductor-less input matching network for both stages so that we can increase bandwidth as well as perfect match for low noise figure. This LNA is designed using Advanced Design System (ADS) software to provide 0.5 dB noise figure with power gain of 25 dB and 1-2.5 GHz Bandwidth. So it can be used an L-Band satellite modem that is used in an asset tracking application. Layout is designed using muruta manufacturing lumped components and Aluminum Nitride (AlN) substrate having high dielectric constant and high thermal conductivity.

Key Words: *LNA, PHEMT, ADS, AlN*

----------***----------

1. INTRODUCTION

In every RF receiver system LNA plays key role as our received signal is very weak. Using proper transistor and topology, LNA design for respective bandwidth as well as desired gain is crucial task. While increasing Gain-Bandwidth product, it's difficult to reduce factors like noise figure as well as return loss. Single stage amplifier design rarely meet this requirement [1]. So we moved towards multistage amplifier topology with quiet changes in intermediate stage design.

High electron mobility transistor (HEMT) provide low noise figure, high gain but moderate input return loss [2] i.e. S11. So our design approach works on noise figure as well as S11. As in [5], Ahmed H. Akgiray, has tested the noise performance of GaAs mHEMT and InP pHEMT transistors for both room temperature and cryogenic temperatures. Biasing is provided at Q-point where grid voltage is closer to 0 volt. So LNA circuit becomes less complicated with single DC supply.

Ioana Giangu and Valentin Buiculescu have proposed LNA design for two stage amplifier working in millimeter wave domain [3] in which intermediate stage design provide matching for S11 of second stage transistor to conjugate of S22 of first stage transistor.

When we referred muruta manufacturing component's datasheet, it was observed that for vary low value of inductor, resonant frequency is 6 GHz and it reduces as it's size increases where size is proportional to its inductance. Parasitic capacitance generated between two adjacent windings inside inductor separated by insulation limits inductive response up to 6 GHz frequency for small practical values and it is difficult to obtain very low noise figure with such inductors which introduce little resistive response too. So we figure out performance of practical inductor over noise figure as well as bandwidth. Increasing value of inductor

So proposed work introduced input, output and intermediate matching network design for low noise figure as well as return loss. Aluminum Nitride (AlN) substrate have high thermal conductivity as well as good dielectric properties, used for MLIN and MTEE.

2. SELECTION OF TRANSISTOR AND BIASING

Key element of HEMT is its Hetero-junction PN junction that uses different types of material either side of it. The most common materials used aluminum gallium arsenide (AlGaAs) and gallium arsenide (GaAs). We have chosen Avago's ATF-34143 which is a high dynamic range, low noise PHEMT housed in a 4-lead SC-70 (SOT-343) surface mount plastic package, as per requirements. Biasing is done as per Q-point requirement where Vgs is nearly 0 volt. So amplifier is biased at 4V, 40 mA. Fig.1 shows HEMT voltage current characteristics. Biasing is done using AVX CR series resistance of 59 KΩ having +/- 1% tolerance and inductor is tuned in series.

Desired matching topology of inputs of both transistors is only capacitor based, so selection of this transistor is done on basis of some properties like noise figure circle and S22. It helps us to minimize inductance required to be generated in our intermediate and input matching network.

3. AMPLIFIER DESIGN

Two ports of 50 Ω are connected either side of transistor and stability of single transistor is checked. As shown in Fig. 2.

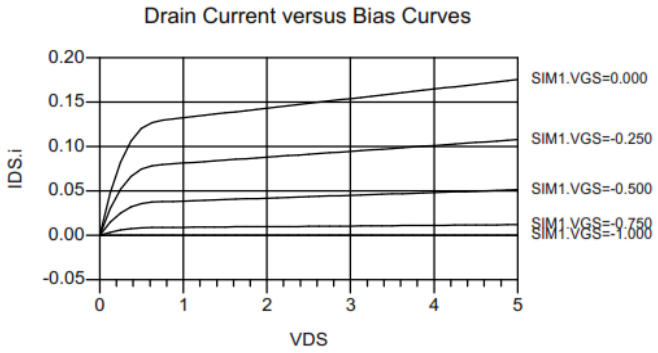

Fig -1: I-V curve characteristics for DC biasing

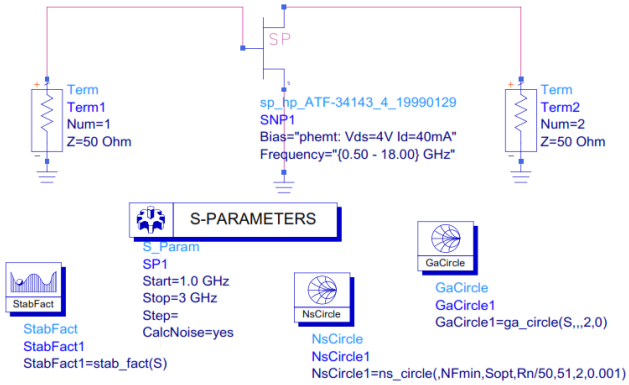

Fig -2: S-parameter simulation of ATF-34143

Performance of single transistor is checked based on S parameter. Fig. 3 shows power gain of ATF-34143 without any flat response whereas input return loss is not good as shown in fig. 4. In Fig. 5, it's observed that noise factor is below 0.6 dB but stability is needed to be achieved.

Series resistance in matching network can increase stability and decrese return loss but noise figure get affected so ignored that method. Instead of it, cascaded topology is prefered.

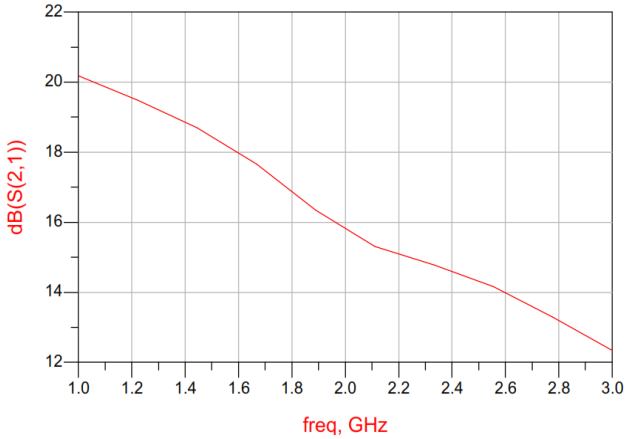

Fig -3: Power gain (S21) in dB

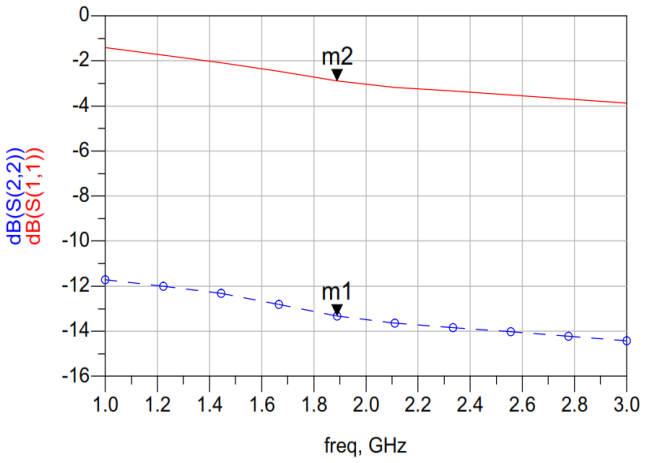

Fig -4: Return loss in dB

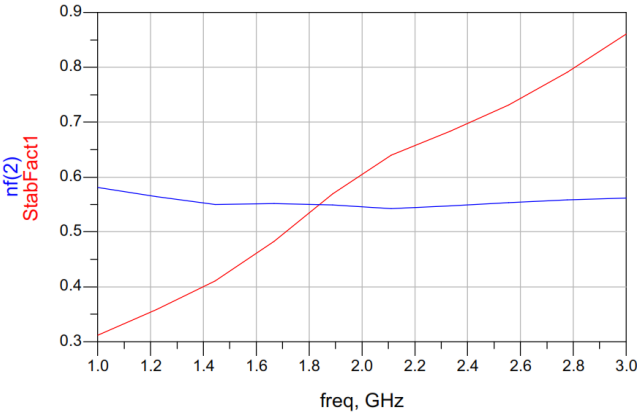

Fig -5: Noise figure (NF) and stability factor (K)

Intermediate stage can be designed by matching S11 of 2nd stage to S22* of first stage but this can introduce little change in noise figure so we have matched S22* to input impedance point which is common to noise figure circles varying with frequency, so that it will have low noise figure for greater bandwidth. Available gain circles intercept noise figure circles so we have ignored it.

Fig. 6 shows two impedances to be matched for intermediate matching network where m2 is S22 at 1.8 GHz and m1 is input impedance chosen for low noise figure. Obtained gain for single transistor is noticed to be 15 to 16 dB from available gain circles so available gain after cascading is assumed to be in range of 25 to 30 dB. But after insertion of MLIN and MTEE, performance is needed to improved using optimization. Also it will be challenging task as practical value of capacitors and inductors won't match with theoretical optimized values. These matching networks are implemented without using single resistor and lumped components are muruta manufacturing measurement based components.

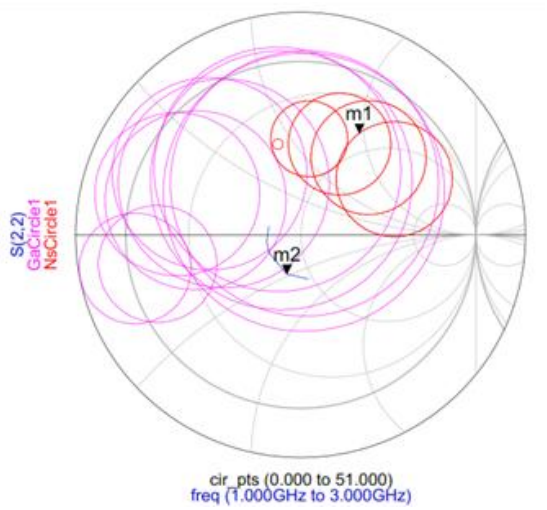

Fig -6: Available gain and Noise Figure circles with output reflection coefficient

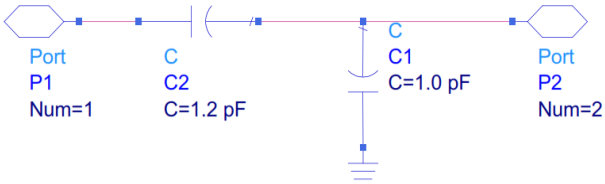

Fig -7: Intermediate matching network with ideal component

After using Smith chart utility tool available in ADS, matching network for intermediate stage is designed as shown in fig. 7 and optimized for flatness of S21 and then same procedure is applied for input side of first stage for low noise figure as well as low return loss. Quality factor of inductors matters lot while design constraints are noise figure as well as bandwidth, because vendor's inductors have some frequency constraints regarding their performance. As inductor's value increases its frequency use limited, so inductors are chosen from LQG series 11A case style where LQG11A12NJ00 is higher value of inductor chosen which works within 4 GHz and SMT GRH series Capacitors are used for implementation.

Noise figure introduced by 2 stage cascaded topology is given as,

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1}$$

Where, F1 and F2 are noise figure of two stages respectively and G1 denote gain of first stage. So overall noise figure is very low.

Designing T-network of L-C components at output stage will gives us following schematic of LNA as shown in fig. 8. AlN substrate have good dielectric properties for wideband application and high thermal conductivity. MLIN and MTEE are connected in the circuit and optimized. We analyzed performance of Thickness of substrate (H) for 15 mil, 20 mil, 25 mil and 30 mil and chose 20 mil for better S-parameter response. Relative dielectric constant (Єr) is 8.6, copper is conductor and loss tangent TanD is 0.004. Surface roughness is 0.002 mil. Optimization tool in ADS set parameters of substrate components for our desired goal. Vias are connected at grounds and three ports are introduced in layout.

Simulation of overall circuits gives good noise figure response up to 3.5 GHz as shown in fig. and flat response of power gain is obtained above 24 dB up to 2.8 GHz.

Rollet's stability constant (K) is obtained above 2 without using resistor in the circuit as shown in fig.

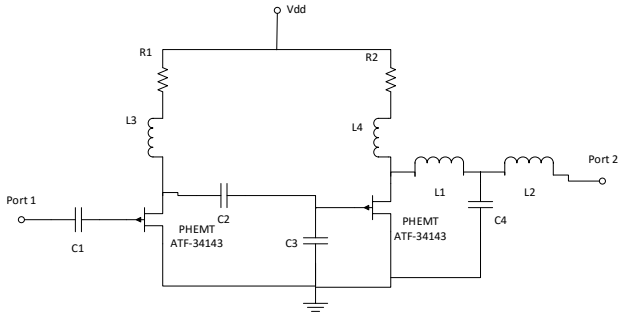

Fig -8: Schematic diagram of LNA

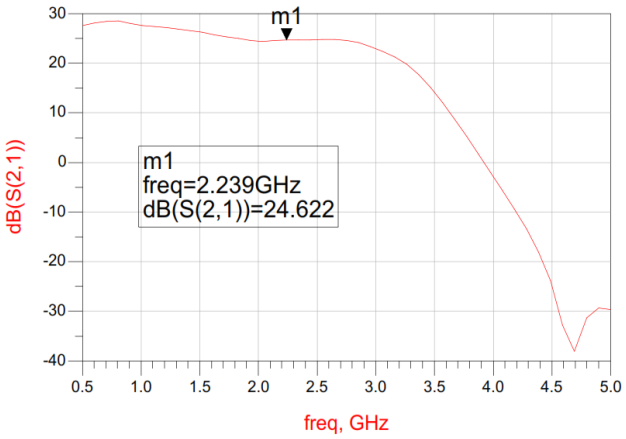

Fig -9: Power gain (S21) in dB

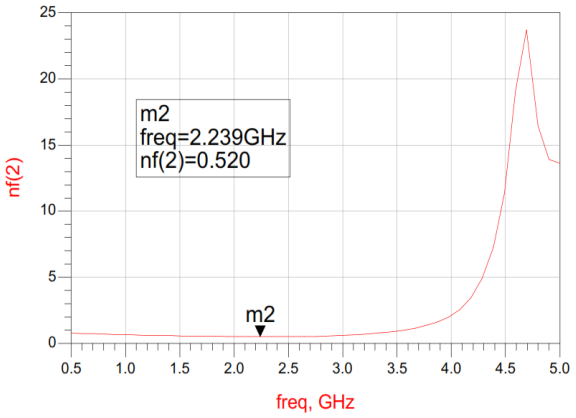

Fig -10: Noise figure in dB

Components are optimized to give VSWR less than 2 i.e. S11 and S22 less than -10 dB. Ultra low Noise figure is achieved by this LNA. Simulation of complete LNA with micro strip transmission lines are shown in fig. 13.

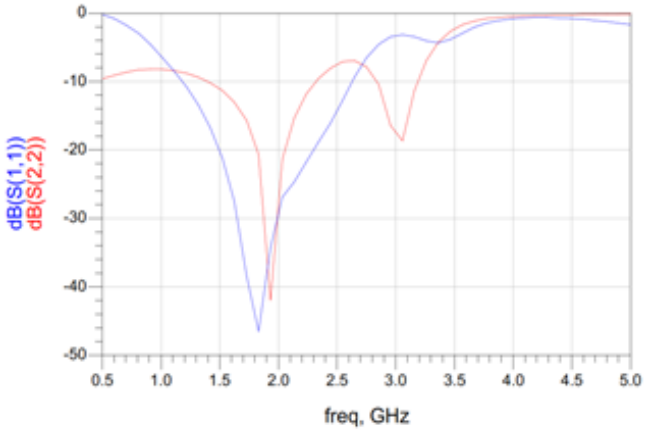

Fig -11: Return loss in dB (S11 and S22)

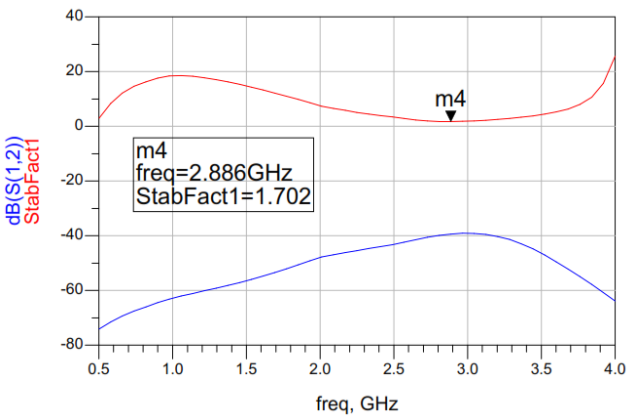

Fig -12: Stability Factor (K) Reverse Transmission Coefficient (S12)

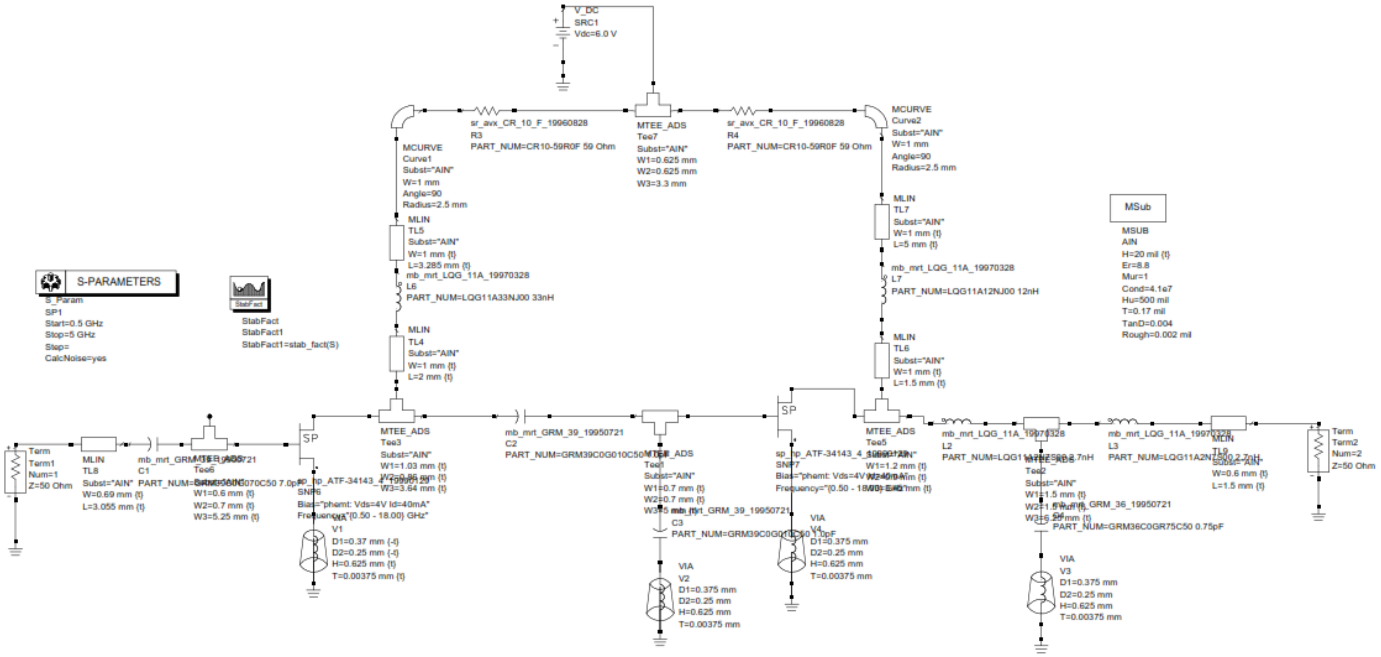

Fig -13: Simulation of schematic of complete LNA in ADS

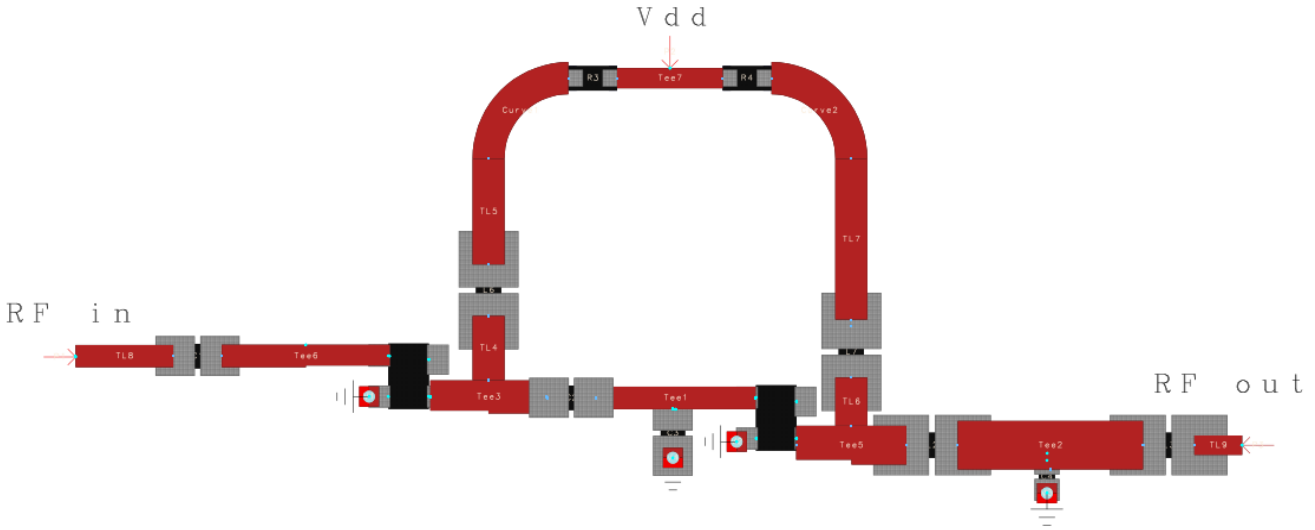

Fig -14: Layout of LNA

Fig. 14 shows bottom view of layout of designed LNA using ATF-34143 using AlN substrate made micro strip lines.

Simulation results shows that noise figure obtained is 0.5 dB from 1 to 2.8 GHz and maximum noise figure is 0.64 at 1 GHz. Input and output VSWR is less than 2 as S11 and S22 is less than -10 dB. VSWR is 2 to 3 in between 2.5-2.8 GHz. Reverse transmission coefficient is less than -40 and Stability factor is more than 2 for desired frequency band and for worst case, 1.7 at 2.8 GHz dB as shown in fig. 12.

Table 1 shows comparison of designed LNA to other proposed LNA. And it claims the advantage of low noise figure of 0.5 dB with power gain greater than 24 dB for 1 to 2.8 GHz which can be used in Satellite modem at Receiver section, Amateur radio, Surveillance radar, Mobile communication etc.

Table -1: Comparison between proposed work and related published work

References	Parameters		
	Bandwidth (GHz)	Noise figure (dB)	Power Gain (dB)
[7]	Single point at 1	0.6	17.49
[1]	Single point at 2.4	2.6	11.2
[6]	2-11	1.6-4	>25
[4]	11.7-12.7	1.7	15
[8]	2.1-2.5	1.9-2,6	11.9
[2]	0.6-1.2	0.56	35
This Work	1-2.8	0.52	>24

4. CONCLUSION

We have designed 0.5 dB low noise amplifier for 1-2.8 GHz frequency range using cascaded topology for gain of >24 dB and layout is designed using AlN substrate. Performance of circuit is observed to be improved due to capacitor based input matching network for both stages where good bandwidth as well low noise figure is achieved.

ACKNOWLEDGEMENT

This work is supported by MCT's Rajiv Gandhi Institute of Technology, Mumbai and also we would like to thank Dr. Udhav Bhosle, Principal of RGIT, Pramod K. B., PhD Student of JAIN University and Dr. Kushal Tuckley, Director R&D AGV System, Mumbai.

REFERENCES

[1] Yongguang Lu, Sh-hui Yang, Yinchao Chen, "Design and Simulation of LNA with the Frequency of 2.4 GHz," 978-1-4244-3709-2/10/$25.00 ©2010 IEEE.

[2] Pramod K B, Kumaraswamy H.V, Praveen K B, "The Design and Simulation of Radio Frequency Narrow Band Low Noise Amplifier with Input, Output, Intermediate Matching," 978-1-4799-0400-6/13/$31.00 ©2013 IEEE

[3] Ioana Giangu , Valentin Buiculescu, "Broadband Two Stages Low Noise Amplifier for Milimeter Wave," 978-1-4673-5672-5/13/$31.00 © 2013 IEEE Pg: 323-326.

[4] N.Ayaki, A.Inoue, T.Katoh, M.Komaru, M.Kobiki, K.Nagahama and N.Tanio, "A 12 GHz-Band Monolithic HEMT Low Noise Amplifier," CH2599-9/88/0000-0101 © 1988 IEEE.

[5] Ahmed H. Akgiray, Sander Weinreb, Rémy Leblanc, Michel Renvoise, Peter Frijlink, Richard Lai, and Stephen Sarkozy, "Noise Measurements of Discrete HEMT Transistors and Application to Wideband Very Low-Noise Amplifiers" IEEE transaction on microwave theories and techniques, vol. 61, NO. 9, SEPTEMBER 2013 Pg : 3285-3297

[6] Niti Mohan, Vaithianathan.V "Noise Analysis of the Input Matching Circuits for UWB Low Noise Amplifiers" at International conference on Communication and Signal Processing, April 3-5, 2013, India , 978-1-4673-4866-9/13/$31.00 ©2013 IEEE Pg : 545- 550.

[7] J.Manjula, S.Malarvizhi, "A 1GHz Current Reuse Low Noise Amplifier with Active Inductor Load" 978-1-4673-5090-7/13/$31.00 ©2013 IEEE Pg: 211-215.

[8] YANG Zong-shuai ,Niehai ,HAN Wen-tao , "A high-linearity S-band SiGe HBT low-noise amplifier design" 2013 International Workshop on Microwave and Millimeter Wave Circuits and System Technology , 978-1-4673-5504-9/13/$31.00 ©20 13 IE E E Pg: 308-311.

[9] A.P. Adsul, Dr. S.K. Bodhe, "A Low-Noise Amplifier Design for 3.1-10.6 GHz Impulse Radio Ultra Wideband Receivers." 978-1-4673-5090-7/13/$31.00 ©2013 IEEE Pg: 470-4

BIOGRAPHIES

R. V. Navagare is currently pursuing M.E. from Mumbai University in Electronics and Telecommunication. His Area of Interest is RF and Microwave Circuits Design and Implementation. He have done B.E. in Electronics and Telecommunication from Mumbai University.
E-mail: ray.revolution9@gmail.com

K. G. Sawarkar is currently working as Head of Electronics & Telecommunication engg. Dept. RGIT, Mumbai and Research Scholar in Mumbai University. His Area of Interest is Design of analog circuits , design of RF circuits and systemsHe has done his BE in Electronics under Amravati University and M.E from Mumbai University.
E-mail: sawarkarkishor@gmail.com