FAST SVM BASED 3 PHASE CASCADED FIVE LEVEL INVERTER

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Abstract

Introduction of nearest three vector algorithm is a major achievement in the area of space vector technology. Complexity and severe computations are still the drawbacks of SVM methods mainly for multilevel inverter applications. A fast SVM technique is introduced in this project which allows the calculation of switch time duration and the efficient determination of switching times based on the two level inverter scheme. SVM modulating waves are generated based on the two level system and then this modulating waves are compared with required number of carrier signals in order to generate the switching pulses for the inverter. Four triangular carrier signals are needed for a five level system in order to generate the switching pulses. Coordinates of the nearest three voltage vectors is not needed, so the complexity of the SVM technique can be reduced and it is the major advantage of the proposed technique compared with conventional SVM techniques used for multilevel inverters. A three phase five level cascaded H bridge topology is used here to verify the effectiveness of the proposed technique. MATLAB simulation and hardware implementation of the proposed system is done. From the analysis of both simulation and hardware it is clear that proposed SVM technique have more fundamental output and less THD than sinusoidal PWM technique.

Key Words: *Cascaded H bridge, Multilevel, Modulating wave, Space vector*

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1. INTRODUCTION

Power electronic system has improved much in recent days because of the development in power electronics and semiconductor technology. Earlier days deals with low power applications but now industrialization demands higher power equipment, which now needs the megawatt level. Simple two level inverter can be used only for low power ranges and for the applications with high power range demands new power electronic converters which can operate with higher voltage and current. For these reasons, a family of multilevel inverters has emerged as the solution for working with higher voltage levels [1]. The major advantages of multilevel inverter is with higher number of levels the output resembles pure sinusoidal characteristics and which reduces the total harmonic distortion. But with increasing the number of levels circuit complexity and number of switching devices is also increases.

The first multilevel inverter was introduced in 1975 and it is a cascaded inverter. Multilevel pulse width modulated inverter was introduced by Bhagavat and Stefanovic. There are different kinds of topologies for multilevel inverters that can generate a stepped voltage waveform and that are suitable for different industrial and power system applications [2]. Multilevel topologies reduces the voltage stress on the devices and improves ac side waveform of the inverter. Basically multilevel inverter topologies classified into diode clamped multilevel inverter, flying capacitor multilevel inverter and cascaded H bridge multilevel inverter. In the case of diode clamped inverter number of clamping diodes increases drastically with increase in levels and real power flow is difficult for single inverter. For flying capacitor inverter start up is complex because pre charging of capacitors are needed and a large number of capacitors are needed which are bulky and expensive. From the drawbacks of diode clamped and flying capacitor inverter it is clear that cascaded H bridge inverters are more suitable if there are number of dc sources are available [3].

There are different modulation schemes such as single pulse width modulation, multiple pulse width modulation, sinusoidal pulse width modulation, trapezoidal modulation, staircase modulation, stepped modulation, harmonic injection modulation, delta modulation etc. These techniques are usually used for two level system. Multilevel system uses techniques like multicarrier sinusoidal pulse width modulation, selective harmonic elimination technique and space vector modulation (SVM) technique [4]. SVM is an advanced computation intensive PWM method. SVM is based on a rotating reference vector and output vottage is obtained using nearest three voltage vectors of the reference vector. Switching sequence and the switching times are determined based on reference vector location.

Nearest three vector algorithm is the conventional space vector technique used for multilevel inverter. But this algorithm is feasible only up to three level, above three level calculations become very complicated [5]. This problem is eliminated by using a phase shifted based SVM [6] or by using an artificial neural network based SVM [7]. Major disadvantages of these techniques are reduction in the fundamental components in the output and complexity. So a new technique is need to implement which has less complexity for multilevel inverters.

This paper describes a new, simple, fast and scalable SVM technique for five level cascaded inverter topology.

2. SPACE VECTOR MODULATION

The concept of space vector technique is based on an anticlockwise rotating reference vector and output voltage is obtained using nearest three voltage vectors of the reference vector. When the reference vector moves from one region to another, there will be an abrupt change in output vector [8]. As a result the switching sequence and the switching times to be calculated corresponding to every change of the reference voltage location.

To understand the space vector modulation technique, consider a two level inverter circuit. Basic three phase two level voltage source PWM inverter consist of six switches is shown in Fig -1.

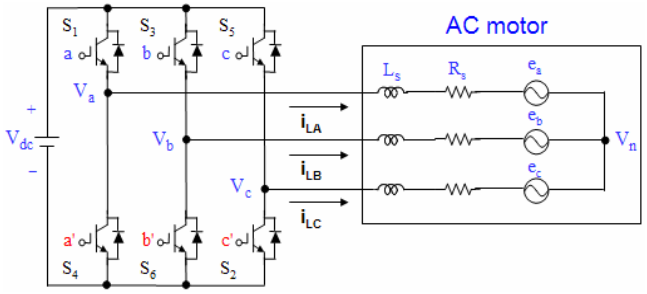

Fig -1: Three phase two level inverter

This circuit consist of 8 switching states out of which 6 are active states and 2 are zero state. At any time three switches are on in this circuit. Zero states are obtained when all the upper switches are on or all the lover switches are on. All 8 switching states are shown in Fig -2.

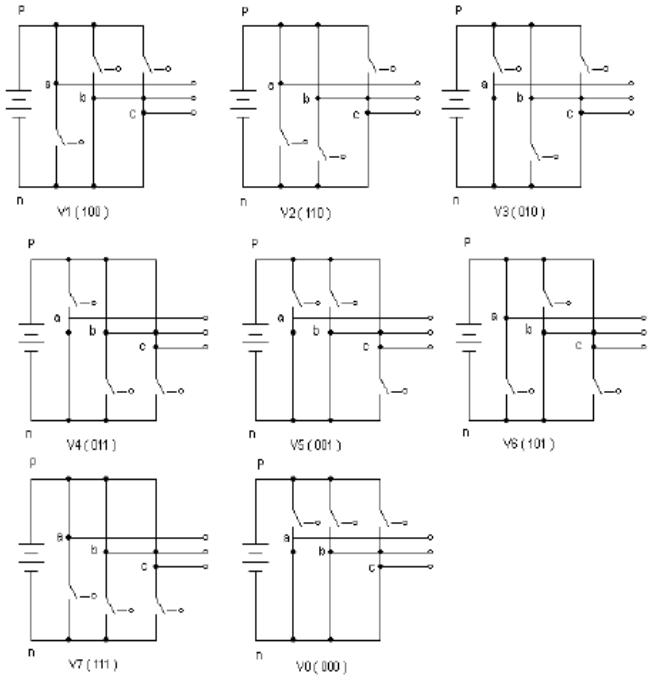

Fig -2: Switching states of two level inverter

First active switching state consist of switches S_1, S2 and S_6 are on is plotted on three phase coordinate is shown in Fig -3.

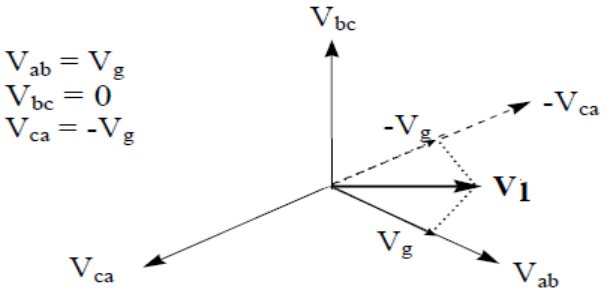

Fig -3: Space vector construction for switching state 1

Correspondingly the complete space vector diagram for all the switching states consist of 6 sectors are shown in Fig -4.

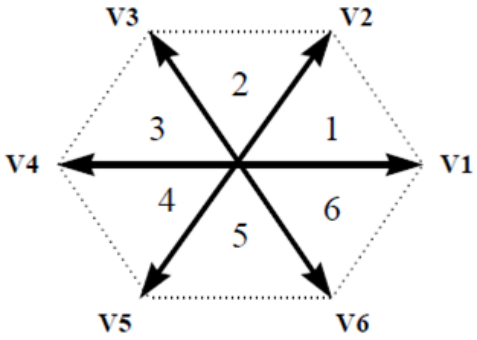

Fig -4: Voltage vectors in α-β plane

First step in SVM is 3 phase to 2 phase transformation. A rotating space vector which rotates in anticlockwise is obtained when 3 phase is transformed to 2 phase and which is shown in the Fig -5.

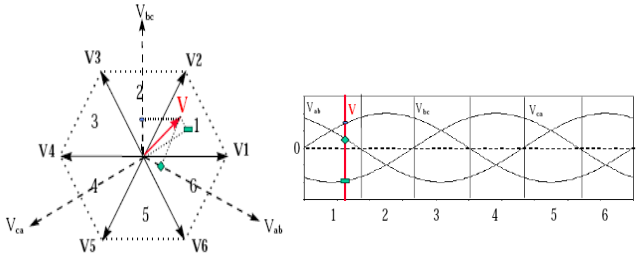

Fig -5: 3 phase to 2 phase transformation

The aim of SVM is to realize this voltage vector V for every instant. By switching between V_1, V_2 and zero switching state the voltage vector V can be realized. How long each vector is need to be switched is known as dwell time and dwell time calculation is the main step in SVM [8].

3. FAST SVM BASED CASCADED FIVE LEVEL INVERTER

Three phase cascaded 5 level inverter is selected to confirm the feasibility of the proposed SVM technique. A three phase cascaded five level inverter is shown in Fig -6.

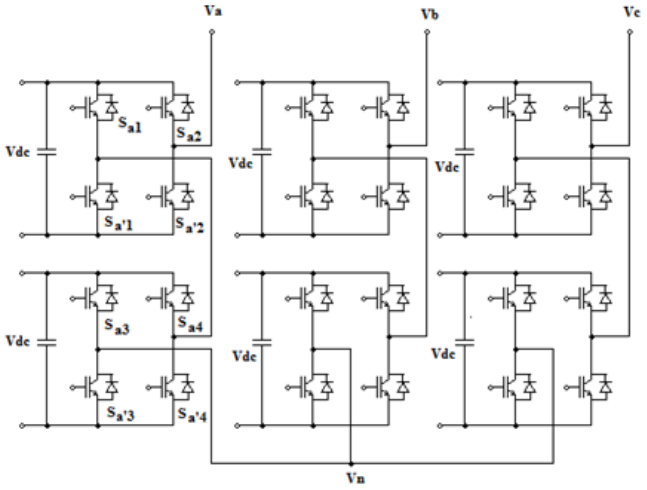

Fig -6: 3 phase cascaded 5 level inverter

By proper switching five level output can be obtained from the inverter shown in Fig -6. Switching states for the five level inverter is shown in Table -1. Here switches Sa'_1, Sa'_2, Sa'_3 and Sa'_4 are complimentary to the switches Sa_1, Sa_2, Sa_3 and Sa_4 respectively. Large redundancies are also there, that is same level can be implemented by using different switching sequences.

Table-1: Switching States for Cascaded 5 Level Inverter

Sa_1	Sa_2	Sa_3	Sa_4	OUTPUT VOLTAGE
1	0	1	0	2Vdc
1	1	1	0	Vdc
0	0	1	0	
1	0	1	1	
1	0	0	0	
0	1	1	0	
0	0	0	0	0
1	1	0	0	
0	0	1	1	
1	1	1	1	
1	0	0	1	-Vdc
0	1	1	1	
0	1	0	0	
1	1	0	1	
0	0	0	1	
0	1	0	1	-2Vdc

3.1 PROPOSED SVM TECHNIQUE

Space vector diagram corresponds to a two level inverter is shown in the Fig -7.

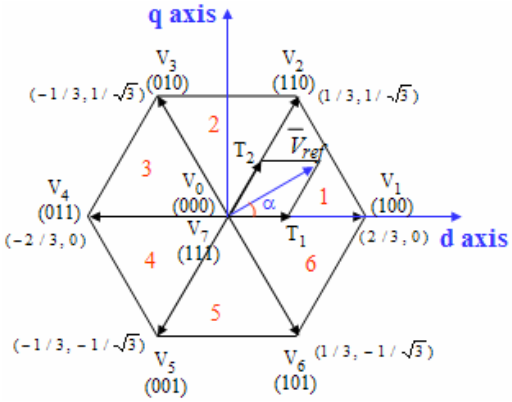

Fig -7: Space vector diagram

V_{ref} shows the rotating vector and SVM tries to realize this vector for every instant and it is done by switching nearest three vectors. Dwell time for each vector is needs to be calculated for this operation. In order for the dwell time calculation it is important to represent output voltage vector in d-q plane and is shown in the Fig -8. V_d, V_q and angle α is needed for dwell time calculations.

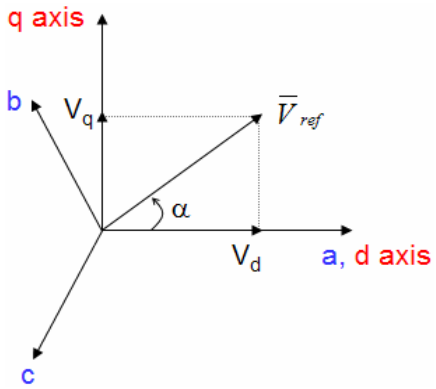

Fig -8: 3 Rotating vector in d-q plane

V_d, V_q and angle α is given by,

$$V_d = V_{an} - \frac{1}{2}V_{bn} - \frac{1}{2}V_{cn} \quad (1)$$

$$V_q = 0 + \frac{\sqrt{3}}{2}V_{bn} - \frac{\sqrt{3}}{2}V_{cn} \quad (2)$$

$$V_{ref} = \sqrt{{V_d}^2 + {V_q}^2} \quad (3)$$

$$\alpha = tan^{-1}\left(\frac{V_d}{V_q}\right) \quad (4)$$

Dwell times can be calculated based on the equations given below.

$$T_1 = \frac{\sqrt{3}T_Z V_{ref}}{V_{dc}}\left[sin\left(\frac{n\pi}{3} - \alpha\right)\right] \quad (5)$$

$$T_1 = \frac{\sqrt{3}T_Z V_{ref}}{V_{dc}}\left[sin\left(\alpha - \frac{(n-1)\pi}{3}\right)\right] \quad (6)$$

$$T_0 = T_Z - (T_1 + T_2) \quad (7)$$

Dwell times for three vectors is obtained and now the switching time for each transistor is need to be find out. Symmetrical switching sequence is selected for reducing the harmonics.

When the reference vector is in sector 1, the switching vectors are 100, 110 and 000(or 111). Sector 2 consist of vectors 010, 110 and 000(or 111). This can be represented with symmetrical switching sequence is shown in Fig -9. In symmetric sequence zero vector is divided into two and provides on both ends of the sampling time T_z.

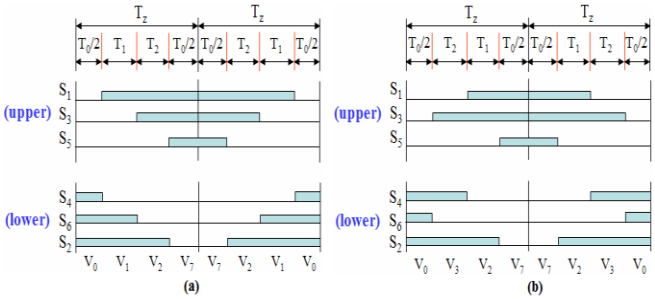

Fig -9: SVM switching pattern for (a) sector1 (b) sector2

Switching pattern for all the sectors can be determined and from this switching pattern switching time for all the transistors are determined and this switching times are used to generate SVM modulating waves. Switching time of each transistor is shown in Table -2.

Table -2: Switching Time for Each Switches

Sector	Upper Switches	Lower Switches
1	$S_1 = T_1 + T_2 + \frac{T_0}{2}$ $S_3 = T_2 + \frac{T_0}{2}$ $S_5 = \frac{T_0}{2}$	$S_4 = \frac{T_2}{2}$ $S_6 = T_1 + \frac{T_0}{2}$ $S_2 = T_1 + T_2 + \frac{T_0}{2}$
2	$S_1 = T_1 + \frac{T_0}{2}$ $S_3 = T_1 + T_2 + \frac{T_0}{2}$ $S_5 = \frac{T_0}{2}$	$S_4 = T_2 + \frac{T_0}{2}$ $S_6 = \frac{T_0}{2}$ $S_2 = T_1 + T_2 + \frac{T_0}{2}$
3	$S_1 = \frac{T_0}{2}$ $S_3 = T_1 + T_2 + \frac{T_0}{2}$ $S_5 = T_2 + \frac{T_0}{2}$	$S_4 = T_1 + T_2 + \frac{T_0}{2}$ $S_6 = \frac{T_0}{2}$ $S_2 = T_1 + \frac{T_0}{2}$
4	$S_1 = \frac{T_0}{2}$ $S_3 = T_1 + \frac{T_0}{2}$ $S_5 = T_1 + T_2 + \frac{T_0}{2}$	$S_4 = T_1 + T_2 + \frac{T_0}{2}$ $S_6 = T_2 + \frac{T_0}{2}$ $S_2 = \frac{T_0}{2}$
5	$S_1 = T_1 + \frac{T_0}{2}$ $S_3 = \frac{T_0}{2}$ $S_5 = T_1 + T_2 + \frac{T_0}{2}$	$S_4 = T_1 + \frac{T_0}{2}$ $S_6 = T_1 + T_2 + \frac{T_0}{2}$ $S_2 = \frac{T_0}{2}$
6	$S_1 = T_1 + T_2 + \frac{T_0}{2}$ $S_3 = \frac{T_0}{2}$ $S_5 = T_1 + \frac{T_0}{2}$	$S_4 = \frac{T_0}{2}$ $S_6 = T_1 + T_2 + \frac{T_0}{2}$ $S_2 = T_2 + \frac{T_0}{2}$

SVM modulating waves can be generated by using these switching times. SVM modulating waves then compared with corresponding number of carrier signals in order to generate switching pulses for the inverter. Five level inverter uses 4 triangular carrier signals. Modulating signal and switching pulse generation is shown in the simulation

4. SIMULATION STUDIES

Space vector technique usually consist of following steps

- Coordinate transformation
- Sector determination
- Dwell time calculation
- Switching point determination
- Triangular carrier comparison with switching points
- Switching pulse generation

Triangular carriers are used in the simulation with frequency 5KHz.

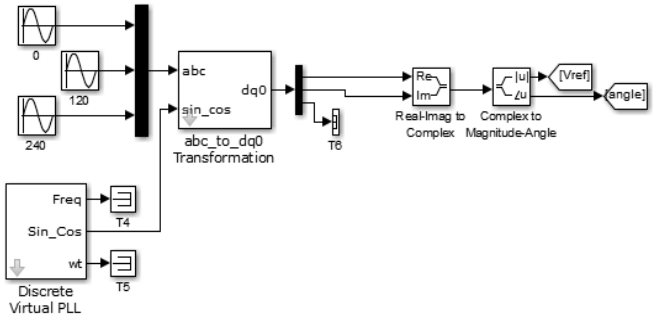

Fig -10: Coordinate transformation

Three phase quantity is converted to two phase here. From the angle α, sector is determined is shown in Fig -11.

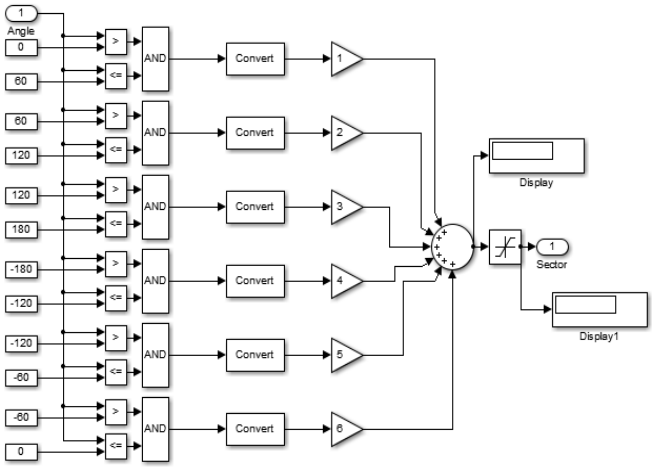

Fig -11: Sector determination

From V_{ref} and angle SVM modulating wave generation is shown in Fig-12.

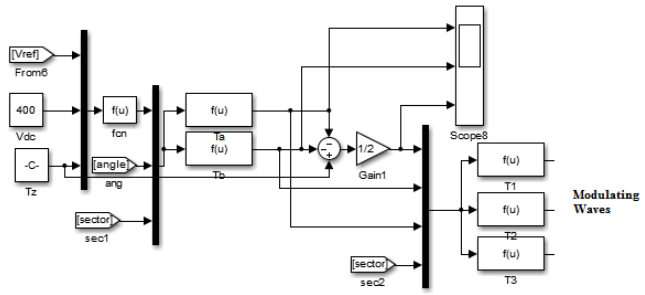

Fig -12: SVM modulating wave generation

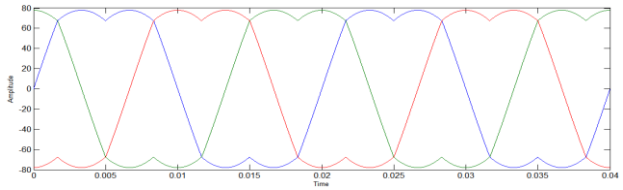

Fig -13: SVM modulating wave

Three phase SVM modulating wave is shown in Fig -13. This modulating wave is compared with four triangular carrier signals in order to generate switching pulses. Switching pulse generation for one leg of three phase inverter is shown in Fig -14.

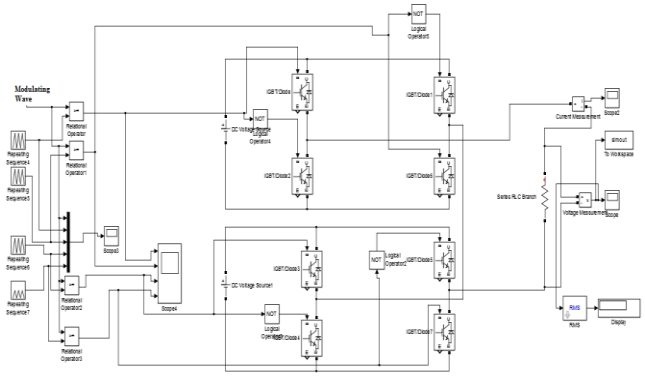

Fig -14: Simulation diagram of 5 level SVM

Output line to line voltage is shown in Fig -15 and it shows more sinusoidal characteristics.

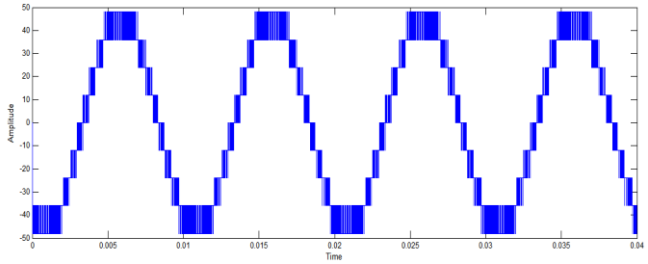

Fig -15: Output line to line voltage

Phase voltage is shown in Fig -16.

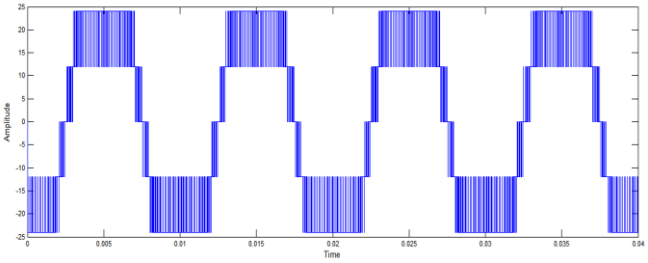

Fig -16: Output phase voltage

Input voltages to the dc sources are 10V each. Simulation is also done with sinusoidal PWM (SPWM) and the comparison of SVM with SPWM is shown in Table -3.

Table -3: Comparison of SVM with SPWM

Characteristic	SPWM	SVM
Line Voltage THD	17.11%	13.29%
Phase Voltage THD	38.37%	28.56%
RMS Line Voltage	32.13V	35.41V
RMS Phase Voltage	15.07V	20.19V

From the table it is clear that for SVM, RMS output is high and THD is less than that of SPWM. It shows the superiority of SVM over SPWM

5. HARDWARE

Hardware section consist of following,

- Power supply section
- Control pulse generation
- Driver circuit
- Main circuit

Hardware setup of one leg of the inverter needs 8 dc sources and it is provided by a single input multiple output flyback converter as shown in Fig -17 [9].

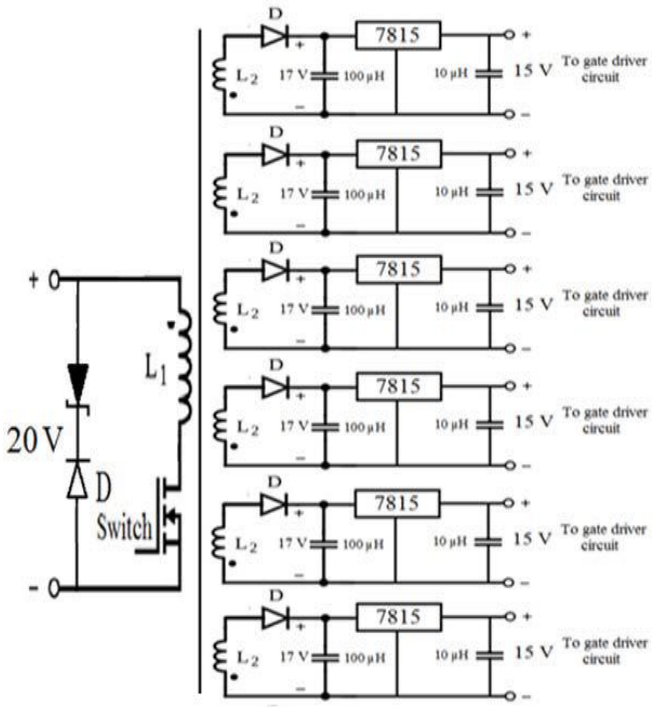

Fig -17: Single input multiple output flyback coverter

Control pulses are generated by using ARDUINO MEGA 2560 controller. Digital outputs from MATLAB can be directly downloaded to ARDUINO and then it provides these pulses from corresponding pins whenever 5V supply is connected to ARDUINO.

ARDUINO output is only 5V and it can't be used directly to MOSEFET's because power electronic switches needs 15V or above for proper operation. So a driver circuit is used consist of TLP250 which provides isolation and feasible voltage level at the gate source terminal of the switch. Complete hardware diagram is shown in Fig -18.

Fig -18: Complete hardware

Five level output voltage obtained across the resistive load as seen in DSO is shown in Fig -19. With the same hardware output of sinusoidal PWM is also checked. When shifting from SVM to SPWM only control pulse changes, so no change in hardware required. Cascaded five level inverter operation with both SVM and SPWM is compared.

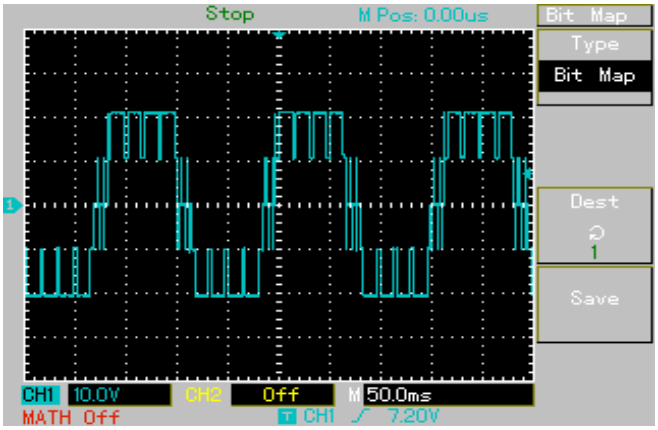

Fig -19: 5 level Output

Comparison of SVM and SPWM on cascaded five level inverter with various modulation index is shown in Table -4.

Fig -18: Comparison of SVM with SPWM

Modulation Index	SPWM	SVPWM
1	15.88V	17.5V
0.9	14.32V	16.8V
0.8	12.24V	13.93V
0.7	10.66V	12.55V
0.6	8.93V	10.65V
0.5	6.71V	8.95V
0.4	5.89V	7.43V
0.3	5.25V	6.62V

This comparison is graphically shown in Chart -1.

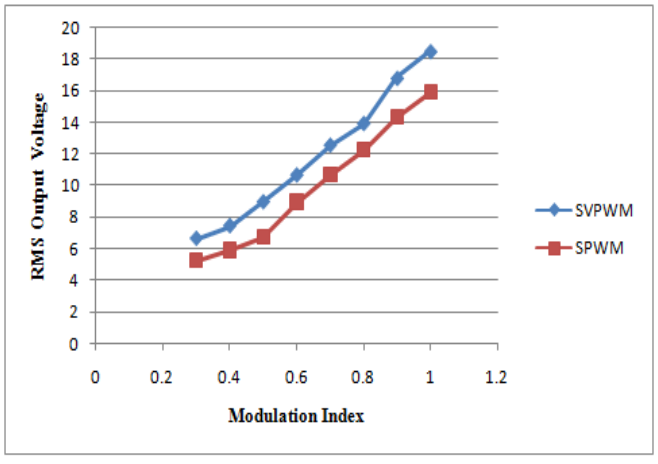

Chart -1: Plot of modulation Index V/S RMS output

From this graph it is clear that RMS output voltage is high for SVM than SPWM for all modulation index. Fundamental output is high for SVM and it is a better alternative for sinusoidal PWM.

6. CONCLUSIONS

Space vector modulation technique is an advanced technique and it needs more attention to reduce the complexity in calculating the SVM variables. The proposed SVM technique reduces the computational burden of SVM calculations. The proposed SVM method can be scaled in a straightforward manner as the number of inverter levels is increased. The nearest three vectors are not needed to be calculated, so the complexity is reduced. The proposed method is based on generation of SVM modulating wave. After generating the modulating wave the proposed method is similar to the multicarrier sinusoidal PWM technique. Major difference is the use of SVM modulating signal instead of sinusoidal signal. From the simulation studies and hardware analysis it is clear that THD is less for proposed system than that of sinusoidal PWM and RMS output voltage is also high for the proposed system.

But the proposed system performance is not good as in the case of conventional SVM technique. Conventional SVM technique is not feasible above three level. So in future SVM technique having advantages of both is need to develop.

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