CASCADED H-BRIDGE MULTILEVEL INVERTER IN A THREE PHASE ELEVEN LEVEL

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Abstract

This paper essentially concentrates on the design and implementation of a unique topology for a three phase eleven level cascaded H-bridge multilevel cluverter by employing different kinds of switching schemes. The basic purpose of this paper is to enhance the number of voltage level at the output without addition of any complexity to power circuit.
The main advantages of this proposed topology is to scale down the THD and reducing electromagnetic interface EMI generation and high voltage with very close to sine waveform. In this paper, severel kinds of carrier pulse width modulation techniques are proposed as which scale down the total harmonic distortion and improve the out voltage from the proposed topology and POD modulation techniques reduce the THD. A number of H-bridge arranged in cascaded to increase the voltage level with the different switching schemes analyzed in this paper. It is observed that this new topology can be recommended to three phase eleven level cascaded H-bridge inverter for the best and optimum performance over the conventional methods. This performance in optimized in the eleven level of inverter.
Improving the fundamental waveforms and reducing the total harmonic distortion by using 60 IGBTs and switching is arranged by a topology in cascaded manners.
The simulation model is produced by MATLAB2009 software version.

Key Words: *Cascaded H-bridge multilevel inverter, different phase pulse width modulation, total harmonic distortionTHD, EMI*

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1. INTRODUCTION

A multilevel inverter is a semiconductor based power electronic device that is used for high-power high-voltage applications such as Uninterruptible power supplies and flexible FACTs. Whereas conventional two level inverter have some limitations in high-power and maximum - voltage applications through switching losses and power ratings [1-2]. Multi-level power conversion is allowed for more than two voltage levels to achieve smoothen and minimum distorted dc to ac power conversion and it can generate a multiple-step voltage waveform with less

distortion, less switching frequency and higher efficiency. The stepped waveforms are fabricated by multiple voltage levels produced by the appropriate connection of the load. This connection is performed by the appropriate switching in the power semiconductors. To obtain a quality output voltage waveform they require high switching frequency along with different pulse-width modulation strategies [3]. Multi-level inverter provides several advantages over two-level inverter so improve the output voltage waveform, minimized (dv/dt) voltage strain on the load and also reduces electromagnetic interference troubles, but it has some demerits. One of the most obvious demerit is the requirement of higher number of power semiconductor switches. Every switch requires a gate driver circuit, therefore maximize the complexity and size of the entire circuit [4]. Lower voltage rated switches can be used in multi-level inverter rather of greater number of semiconductor switches which can be minimized cost of the semiconductor switches as compared to two level inverters.
The multilevel cascaded H-bridge (CHB) inverter shown in Figure 2.1 is one of the popular inverter topologies for high-power applications due to its high voltage operating capability, low dv/dt with reduced total harmonic distortion (THD) and modular structure for reduced manufacturing cost [5]. The conventional modulation schemes for the CHB multi level inverter including carrier based sinusoidal modulations with phase opposition disposition techniques (PODPWM) [6, 7]. The level-shifted modulation schemes have a good THD profile, but suffer from unbalanced power distribution [8-10], whereas the phase shifted schemes are simpler but produce higher THD[8]

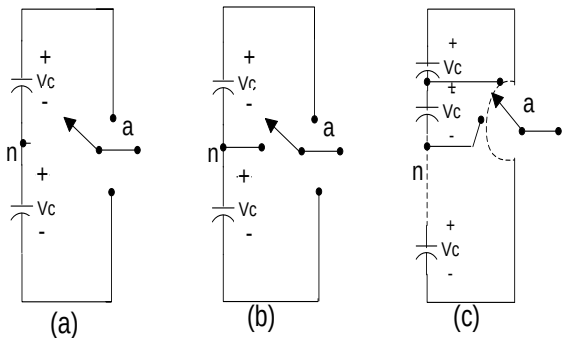

Figure 1: one phase leg of inverter (a) two level (b) three level (c) n-levels

1.1 Equivalent Representation

An equivalent representation of one phase leg of inverter with different levels shown in figure 1, and power semiconductors is represented by ideal switches with several of positions [3].

There are different conventional multi-level inverters topologies are neutral point- clamped, flying capacitors (capacitor clamped), and cascaded H-bridge (CHB). In 1981 Nabae

Phase opposite disposition PWM scheme offers great advantages such as improved output voltage waveforms, lower EMI, and minimized THD in comparison of other PWM switching schemes.

2. PROPOSED TOPOLOGY

This topology requires sixty semiconductor switches and fifteen isolated dc voltage sources Vdc shown in fig 2.1

OPERATION OF THREE-PHASE ELEVEN-LEVEL INVERTER ARRANGED IN CASCADED MANNER

Operation of the three-phase eleven-level inverter with CHB topology is easily explained with the help of fig. 1.2

Whenswitches

S1,S2,S6,S8,S10,S12,S14,S16,S18,S20,S21,S22,S26,,S28,S30,S32,S34,S36,S38,S40,S41,S42,S46,S48,S50,S52,S54,S56,S58,S60 are turned on the output voltage will be "Vdc" (i.e., level 1). The output voltage will be "+2Vdc" (i.e., level 2) when switches S1, S2, S5, S6, S10, S12, S14, S16, S18, S20, S21, S22, S25, 26, S30, S32, S34, S36, S38, S40, S41, S42, S45, S46, S50, S52, S54, S56, S58, S60are turned "on". Similarly output voltage will become "5Vdc" (i.e. level5). When switches S1, S2, S5, S6, S9, S10, S13, S14, S17, S18, S21, S22, S25, S26, S29, S30, S33, S34, S37, S38, S41, S42, S45, S46, S49, S50, S53, S54, S57 and S58.

When the switches S2, S4, S6, S8, S10, S12, S14, S16, S18, S20, S22, S24, S26, S28, S28, S30, S32, S34, S36, S36, S38, S40, S42, S44, S46, S48, S50, S52, S54, S56, S58 and S60 "on" the output voltage is zero (i.e., level 0).

S3, S4, S7, S8, S11, S12, S15, S16, S19, S20, S23, S24, S27, S28, S31, S32, S35, S36, S39, S40, S43, S44,S47,S48,S51,S52,S55,S56,S59 and S60 turn negative half cycle can be generated across load. The voltage blocking capacity for every switch is Vdc [2]. The operation of this topology can also be easily understood by mode of operation of single-phase eleven-level inverter shown in figure 2. Each voltage source "Vdc" is required 100V. There are eleven sufficient switching modes in generating the multistep levels for a eleven-level inverter.

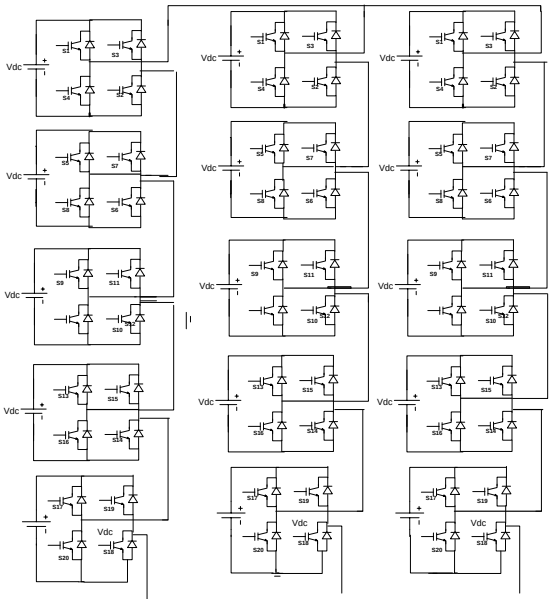

Figure 2.1: cascaded arrangement of three phase eleven level multilevel inverter

3. MODULATION STRATEGIES

There are different pulse width modulations with different phase relationships.

- Phase disposition pulse width modulation (PD PWM):- In phase disposition pulse width modulation strategy, where all carrier waveforms are in same phase.
- Phase opposition disposition pulse width modulation (POD PWM):- pulse width modulation (PS PWM**)**:- Fig.3.1 shows the carrier Phase-opposition pulse width modulation strategy. In phase opposition disposition pulse width modulation strategy, where all carrier waveforms above zero reference are in phase and below zero reference are 180^0 out of phase.
- Alternate phase opposition disposition pulse width modulation (APODPWM):- In alternate phase opposition disposition PWM scheme, every carrier waveform is out of phase with its neighbor carrier by 180^0
- Phase-shifted A carrier phase shifted PWM for multi-level inverter is utilized to generate the stepped multi-level
- output voltage waveform with lower % THD. In proposed, before implementing the Multicarrier PWM Techniques, the gating signals of multi-level inverter switches are generated by comparing sinusoidal reference wave with triangular carrier waves (N-1=3) with 120^0 phase displacement and a constant value at specific intervals of time

3.1 FFT analysis of a three phase nine level inverter CHB) shown below.

This performance in enhanced in the eleven level of inverter Improving the fundamental waveforms and reducing the total harmonic distortion by using 60 IGBTs and switching is arranged by a topology in cascaded manners

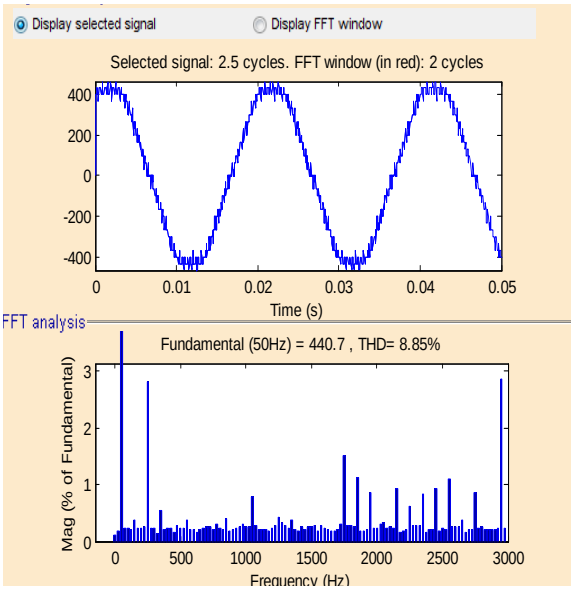

Figure .2: PWM output voltage and harmonic spectrum in three phase nine level CHB inverter (Modulation index1.2)

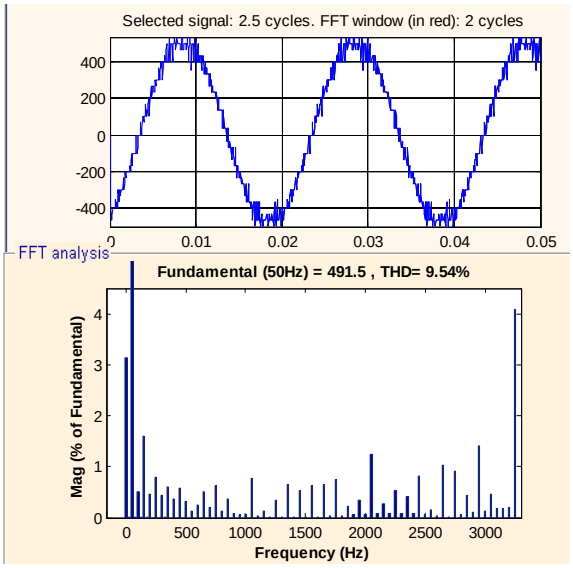

Figure 4.2: PWM output voltage and harmonic spectrum in three phase eleven level CHB inverter (Modulation index 1)

TABLE I: NUMBER OF COMPONENTS:- The number of required components for single-phase eleven level inverter is shown in Table I

Inverter type	**NPC**	**Flying capacitor**	**cascade**	**Proposed**
Main switches	2(N-1)	2(N-1)	2(N-1)	(N-1)+4
Main diodes	2(N-1)	2(N-1)	2(N-1)	(N-1)+4
Clamping diodes	2(N2) (N-1)	0	0	0
DC bus Capacitor/Isolated supplies	(N-1)	(N-1)	3(N1)/2	(N-1)/2
Flying capacitors	0	(N-1) (N-2)/2	0	0
Total numbers	(N1) (2N+1)	(N1) (N+8)/2	11/2 (N-1)	(5N+11)/2

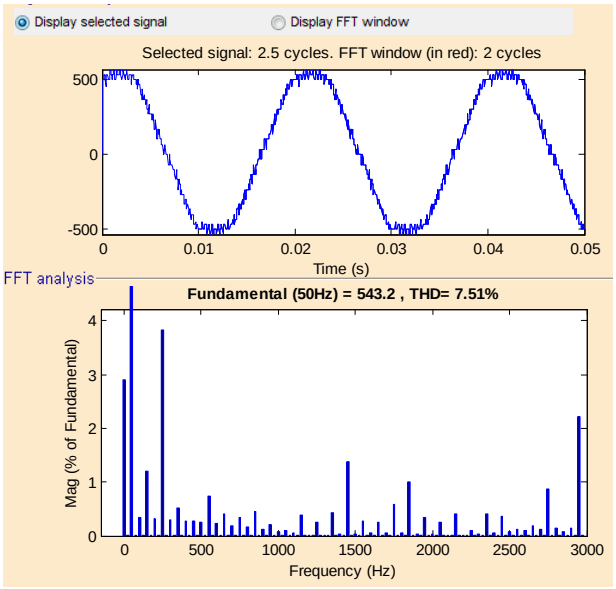

Figure 4.2: PWM output voltage and harmonic spectrum in three phase eleven level CHB inverter (Modulation index 1.2)

4. CONCLUSION

Multi level cascaded H bridge inverters from 7- levels to 11-levels have been simulated using MATLAB/Simulink. The following conclusions can be made from the analysis. If number of level increases, the THD content approaches to small value as gestate. Hence it eliminates the requirement of filters. Though, THD decreases with increase in number of levels, some lower or higher harmonic contents persist prevalent in each level. These will be more dangerous in induction drives. Hence the future work may be focalized by applying closed loop control with suitable harmonic elimination.

TABLE 2: Percent THD comparision for different level and different M.I

MODULATION INDEX	PWM %THD FOR 11-LEVEL	PWM %THD FOR 9-LEVEL
0.92	13.29	15.76
0.95	12.10	14.76
0.99	11.31	13.28
1	9.54	12.73
1.2	7.51	8.85

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