A FOUR-WAY AUTOMETIC TRAFFIC CONTROL SYSTEM WITH VARIABLE DELAY USING HDL

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Abstract

Traffic congestion is a severe problem in this new era of growing vehicle population in all the developing countries. This is a bold signal to the modern age technology for a major improvement and innovation in the existing traffic control system. The most widely used traffic control system uses a simple time-based system and it works on a time interval basis. It is an automatic system but for modern age random and non-uniform traffic, it is inefficient. The advance automatic systems use the image processing technology or advance communication system to communicate and route. It might be used in the developing countries but it is very much complex and expensive too. The practical implementation of this advance traffic control system is also arduous in countries like India.

In this paper, a low cost, real-time, system-on-chip (SoC), application specific automatic traffic control system has been proposed and implemented for four way traffic and the delay between two states can be changed manually, depending upon the density of the traffic. It is being implemented using Hardware Description Language (HDL) on a Field Programmable Gate Array (FPGA) chip without using any other hardware resources or high level languages. The physical attribute of an FPGA chip, being compact in size and low in power consumption, makes it an ideal platform for the implementation. The complete architecture of the proposed traffic control system has been designed using Finite State Machine (FSM) based approach and it contains three different modules. The modules are System Initialization Module (SIM), Signal Generation Module (SGM) and Delay Control Module (DCM). The architecture is completely synthesized for Spartan 3E xc3s500e-4-fg320 FPGA with only 1% of the total logic utilization. Result obtains from a practical set-up of a four-way traffic system, where the signals are controlled by the proposed controller and the toy cars and the density of the traffic has been controlled manually.

Key Words: *Traffic controller, Four-way traffic system, FPGA, HDL, and FSM.*

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1. INTRODUCTION

The population growth is growing in an alarming rate in the developing countries. With this growing population, the number of vehicle is also increasing. This point out to the disastrous increment in traffic density causes the congestion in traffic and calamity in its controlling system. The traffic congestion is one of the most challenging factors in most of the cities of the developing countries. It causes many critical problems and also brings the human life under a serious question. To a traveler, congestion means the lost of time and productivity, trade opportunities, frustration, delays and increase in cost. To solve congestion problem is feasible only by improving the traffic control system by replacing the present day system with some new innovation and/or modification.

According to the W. Wen paper [1], a growing body of evidence proves that simply expanding a road infrastructure cannot solve traffic congestion problems. In fact, building new roads can actually compound congestion, in some cases, by inducing greater demands for vehicle travel – demands that quickly eat away the additional capacity.

The saturating density of the traffic now points to the need of advance intelligent traffic signal systems to take place instead of the conventional manual and time based traffic control system [2]. But the advance traffic control system uses the image processing based density identification for routing of traffic [2]. This process is inefficient till date in some situation like rain, fog, dust etc. The other conceptual system is based on interaction of vehicles but it is not practically possible to implement this time of system in countries like India where the number of vehicles exceeds 100 million on road [2], [8].

In light of the above, this paper proposes a low-cost, real-time, System-on-Chip (SoC), application specific, automatic traffic control system to control a four-way traffic system. In this proposed traffic control system, the delay between two states can be varied manually, depending upon the density of the traffic. The manual control of the delay has been chosen to avoid the error or inefficient results and impairment of the system due to the environmental obstacles and implementation – maintenance problems in countries like India.

The rest of the paper is organized as follows. Section 2 describes the FPGA based implementation of the proposed traffic controller – its architecture, execution process and operational description. Section 3 presents the hardware specific implementation and synthesis details for the target Xilinx Spartan 3E xc3s500e-4-fg320 FPGA development platform. Experimental results for the dummy four way traffic system are described in section 4 and section 5 concludes the paper.

2. PROPOSED FPGA BASED CONTROLLER

This section initially describes the basic characteristics and operation of a four-way traffic system and then introduces the proposed controller in rest of the section.

2.1 Four-Way Traffic System

Four-way traffic system is a process of controlling the traffic in the junction point of four lanes. Signals are there in each lane to control the traffic. Red signal is used to stop the traffic. At the same time, the green signal allows the traffic to move on straight, left and right simultaneously for that particular lane in which the signal is given. Before changing the signal to the other lane, a warning is given by blinking/glittering the yellow light. Chronologically, the traffic is cleared in the same way as mentioned for the other lanes, so that the traffic will be cleared smoothly and systematically, without interrupting others. These systems are controlled automatically and supervised by a traffic supervisor in this proposed system.

Fig -1 represents a generic model of a four-way traffic system. The lanes are numerically numbered in the diagram. When the traffic of north-south i.e. 1-3 is opened, the traffic signal of east-west i.e. 2-4 is closed. So, the traffic of 1-2 can easily move on and the traffic of 2-4 stands still as the signal is closed. As it is a four-way traffic system, the traffic of 3-1 and 4-2 works in same manner as the traffic of 1-3 and 2-4 respectively.

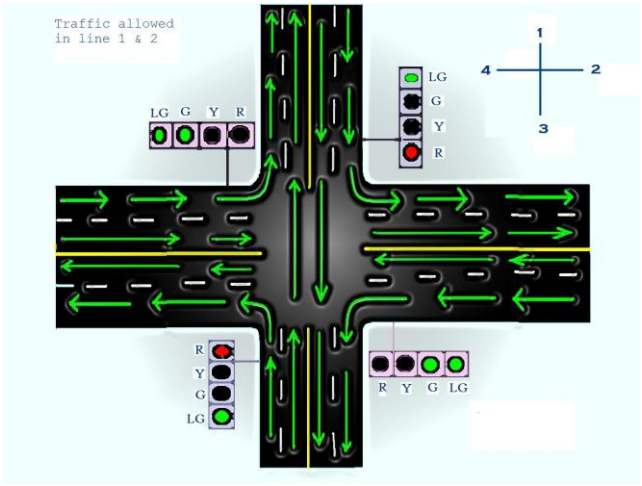

Fig -1: Generic diagram of a four-way traffic system

2.2 Architecture of the Proposed Traffic Controller

The workflow of the proposed traffic controller is based on the initialization of the system followed by the signal generation and delay calculation. The modular architecture of the proposed traffic controller is shown in Fig -2 and state diagram of the overall control flow is depicted in Fig -3. This state diagram is working as the backbone of the proposed traffic controller. The complete architecture has been implemented using VHDL.

As we observed from the above mentioned flow sequence and internal architecture, the proposed traffic controller is divided into four different modules. They are System Initialization Module (SIM), Signal Generation Module (SGM) and Delay Control Module (DCM). A System Control Unit (SCU) is also there along with these modules to control the activities of each modules and flow of respective driving signals. SCU operates based on the FSM depicted in Fig -3.

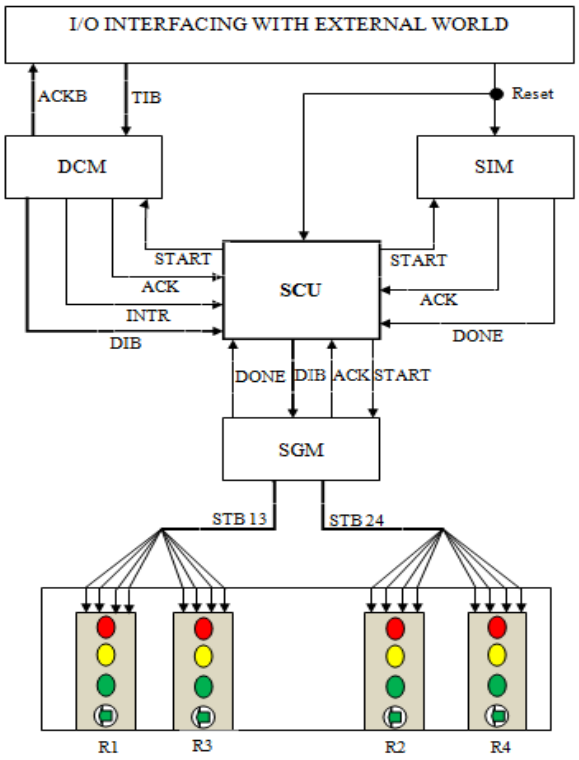

Fig -2: Internal architecture of the proposed controller

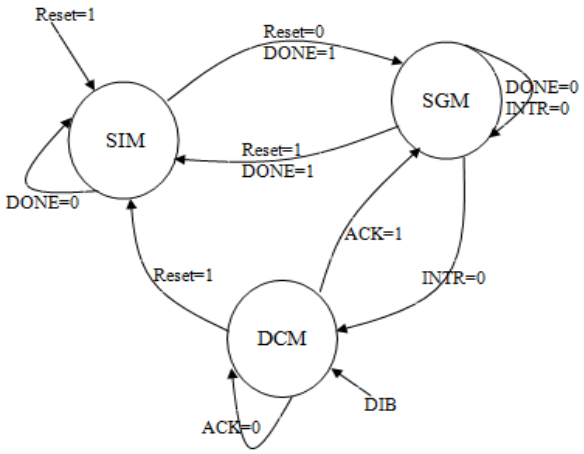

Fig -3: State diagram of the proposed controller

Each of the modules and SCU contains several control signals. The controller communicates with the external world through Reset, TIB (Traffic Input Bus) and ACKB (Acknowledgement Bus) signals and it communicates with the traffic signals through the two STB (Signal Transmission Bus) specified for lane 1, 3 and lane 2, 4. As lane 1 and lane 3 works similar in every particular session, so, the signals are also same for them. This is true for lane 2 and 4 also. Different signals are connected to the bus which

is specified for them. The other required power supply lines are externally connected to every traffic signals stands.

2.3 Operation of the Proposed Traffic Controller

The flow of execution and communication between every module and the signals are described in this subsection.

Reset signal is the driving signal of this proposed controller. When SCU gets the Reset signal asserted, it activates and transfers the control to SIM. SIM then polls the Reset signal continuously and when it gets that signal de-asserted, it then informs the SCU by making the ACK signal high and transfers the control to SCU by asserting the DONE signal. After receiving the DONE signal, SCU then initiates the entire modules with their signals and activates the DCM and SGM by asserting the START signal. After successful activation of those modules, the SCU receives the ACK signal asserted from those individual modules. If it does not receive the ACK signal, then again the SCU starts reactivating those modules.

The DCM polls and receives the TIB signal input from external world, calculate the delay from it, and produce the result to SCU through DIB (Delay Input Bus) line. The TIB bus takes the number of traffic per unit time as input from the external world. This signal is controlled manually. There is two TIB bus for two individual lanes (one is for lane 1 and 3 and another is for lane 2 and 4) to track the number of traffic in that particular lane and generate delay to the particular DIB line. There is two DIB bus for that consecutive lanes. Therefore, depending upon the input number, the delay has been generated. There is a delay chart given in Table -1, which is followed by DCM to generate delay for every DIB inputs. DCM asserts the INTR signal every time the delay has been changed. The SCU then initiates the SGM again with the new delay given by DCM.

Table -1: Delay Calculation Table

Number of Vehicle/unit time	Value of Delay in Sec
1	10
2	8
3	6
4	4
5	2
Greater than 5 (>5)	1

In this paper the maximum number of vehicles is taken as 5/unit time to make this proposed system simple and feasible for a simple demonstration.

The SGM is the module which generates the signal for each traffic polls and integrates the received delay through DIB with the signal generation process. This signal generation process follows a sequence depicted in Table -2. The term R, Y, G denotes the three different traffic lights red, yellow and green respectively. The LG stands for the left-turn green signal which allows the vehicles to move to the left direction. Other signals work as per the standard convention.

The signal generation process works in four steps as depicted in Table -2. They are S1, S2, S3 and S4. The first state S1 enables the red signal (R) for lane 1 and 3 and green signal (G) for lane 2 and 4. Other signals remain de-asserted except LG. S2 makes the yellow signal (Y) enabled for lane 2 and 4. The other entire signals remain same as S1. After this, S3 turns G on for lane 1 and 3 and asserts R for lane 2 and 4. This also turns the other entire signals off in this state. Then in S4, Y becomes asserted for lane 1 and 3 and the other signals remain unchanged during this state. The LG signal remains asserted for all the states except in S2 and S4 for lane 2 and 4 and lane 1 and 3 respectively. This signal actually allows the traffic to move on to the left direction. There is no obstruction with the left turn movement of a vehicle for which, this signal remains on for all the steps. But it only turns off for those steps where Y is asserted.

The delay value is assigned in between two states. This delay actually informs the SGM about how much time the SGM should give to a particular state to be executed. End of this delay time denotes a change in states which implies a change in the light in the traffic signal stands.

Table -2: Signal Generation Table

States	Lane 1 and 3				Lane 2 and 4			
	R	Y	G	LG	R	Y	G	LG
S1	1	0	0	1	0	0	1	1
S2	1	0	0	1	0	1	0	0
S3	0	0	1	1	1	0	0	1
S4	0	1	0	0	1	0	0	1

3. HARDWARE BASED IMPLEMENTATION

To explore the feasibility of the proposed architecture, the FPGA based controller was implemented with the help of synthesizable VHDL. The target development platform is based on Spartan-3E (xc3s500e-4-fg320) FPGA chip. The four traffic polls of the dummy four-way traffic model have been connected with the target FPGA board using 6-pin cable to control the LEDs.

The design was successfully synthesized using Xilinx ISE version 14.1 for the Spartan-3E XC3S500C target device and then it was compiled and built for implementation. This process consists of translating, mapping, placement and routing of the signals. For the design implementation process, no partition was specified and the design was translated and mapped successfully. All signals were placed and routed successfully as well; all the timing constraints were met. 1% of the total logic slices on the device were utilized for this implementation. Brief description of the resource utilization during implementation is given in Table -3. The available logic slices available for the target Xilinx Spartan 3E FPGA board is 4656 (from the synthesis report generated after synthesis).

Also from that synthesis report of the proposed traffic controller, the number of logic slices used is 50 out of 4656 i.e. 1% of the total logic slices available for the target Spartan 3E FPGA board.

Table -3: Resource utilization during implementation

Logic Blocks	Number of Logic Blocks
Adder/Subtractor	1
Registers	31
Flip-Flops	31
LUTs	92
Clock Buffer	1

4. EXPERIMENTS AND RESULTS

The proposed traffic controller has been designed to minimize the traffic congestion and maintain streamline flow of the vehicles in a four lane traffic system. The controller has been tested by going through different case studies and the results have been verified using two types of test units. They are described as follows.

- **On-board LEDs**: The Spartan 3E target FPGA board contains 8-bit output unit with 8 on-board LEDs [9]. The output traffic signals of the implemented controller for lane 1 and 2 have been mapped to that 8-bit output port (each traffic poll has four different signals and the signal generation states for lane 3 and 4 are same as the states for lane 1 and 3 respectively) to verify the effectiveness of the proposed controller.

- **Dummy Four Lane Model**: A dummy model has been introduced to verify the efficiency and effectiveness of the proposed controller. Some toy cars have been placed to verify the changes of traffic signal with the changes in delay.

The proposed traffic controller has been verified through the above mentioned two test units. The case studies involve testing of the implemented controller with different delay value by manually changing the number of vehicles in that particular road. Fig -4 shows the output of the traffic controller for signal generation state S1 through the on-board 8-bit output unit. The TIB signal has been mapped to the input switches available in the target Spartan 3E FPGA board, so that, this can be manually changed. Table -4 depicts the time taken by the controller to change the signal generation states with the changing delay function in terms of the number of vehicles. Different values are given as the number of vehicles in the implemented traffic controller to validate the efficiency and effectiveness for the real world manual delay control. Consecutively, Fig -5 shows the S2 signal generation state output, Fig -6 shows the S3 output and Fig -7 shows the S4 signal generation state output. All this results are recorded using the 8-bit on-board LED output unit of the target Spartan 3E FPGA board.

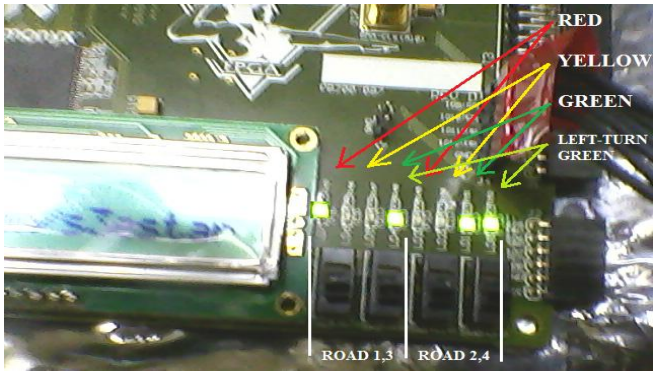

Fig -4: Traffic Controller Output for S1

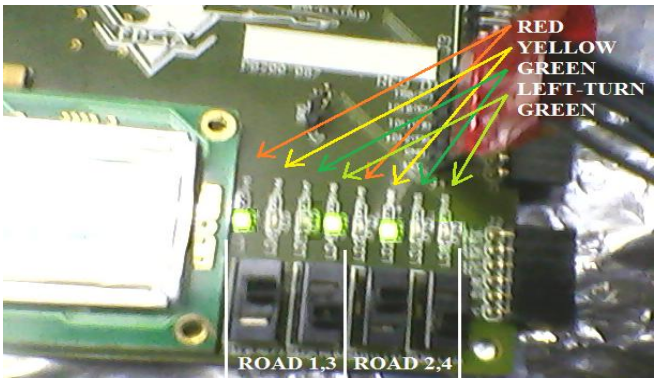

Fig -5: Traffic Controller Output for S2

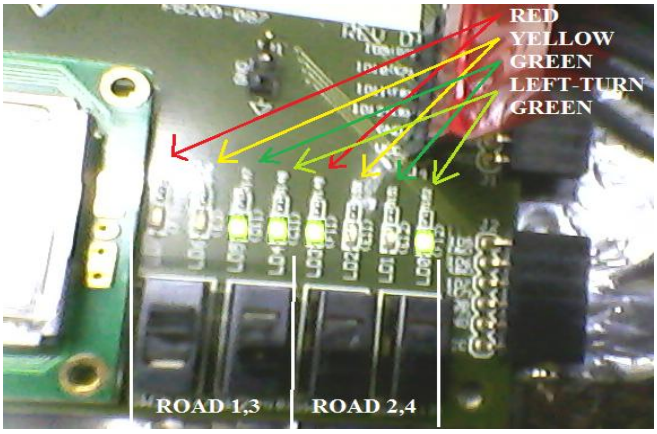

Fig -6: Traffic Controller Output for S3

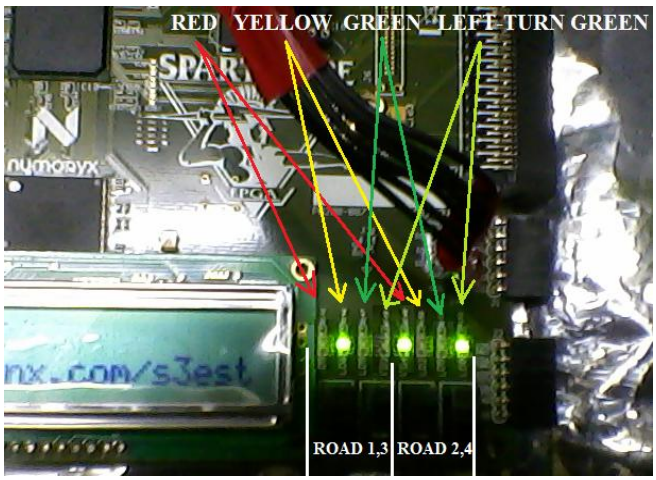

Fig -7: Traffic Controller Output for S4

Table -4: Change of Delay with Number of Vehicle

Number of Vehicles (/minute)	Delay (in second)
1	10
4	4
9	1
3	6
5	2

The dummy model of a four way traffic lane has been shown in Fig -8. This system is also tested for different delay by generating different delay values. The graphical representation of the delay for different number for vehicles has been shown in Chart -1.

Fig -8: Entire Model with Active Traffic Signal

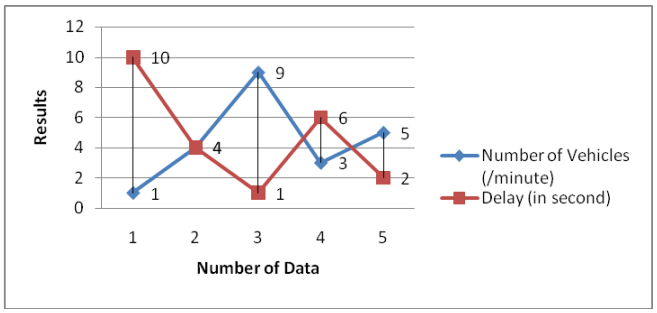

Chart -1: Variation of Delay with Vehicles

5. CONCLUSIONS AND FUTURE WORK

This paper proposes an on-chip design and implementation of a traffic controller to control and minimize the congestion of traffic in a four-way traffic system. To control the congestion in rush hours, a delay module has been integrated with the proposed controller to vary the delay between the appearances of two signal states (red → green) for every individual lane. This also minimizes the congestion by generating variable delay when one lane is almost traffic free and another is full of vehicles.

Future work will involve the extension of the proposed traffic controller in more wide sense. This paper focuses on the four lane traffic control and the manual control of the delay; however this approach can be extended to control the traffic for more than four lanes or the variable number of lanes. The delay can be calculated automatically by the controller from the vehicle count. The further modification can be incorporated by changing the proposed architecture as well as the design can be implemented in other high-end target platform with a very minor modification in configuration procedure.

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BIOGRAPHIES

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