

SERIAL INTERFACE MODULE FOR ETHERNET BASED APPLICATIONS

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Abstract

The introduction of Field Programmable Gate Arrays (FPGAs) which includes thousands of logic gates has made it feasible to prove specific software function on the particular hardware. This reduces the design time and the execution time and makes the embedded system to respond faster as a real time system. This paper serial interface module for Ethernet based Applications deals with the Study and the implementation of the Tri-mode Ethernet Media access control (TEMAC) which is present in the FPGA core. The Virtex-5 FPGA supports the 10Mbps, 100Mbps as well as 1000Mbps but in this paper contains the implementation of 1000Mbps (1Gigabit bits per second) data transfer rate. This project basically deals with communication established between the FPGA core and the PC. The IP core is interfaced with its transceiver module and communicated to the PC using Ethernet medium. The communication established is verified by interfacing the FIFO and the UART VHDL codes to the TEMAC IP core present on the Virtex-5 FPGA. The result at each module is verified on the Chipscope pro analyzer and the packet transmitted from FPGA to the PC is verified on the Wireshark software.

Key Words: FPGA, Ethernet, TEMAC core, and Gigabit.

1. INTRODUCTION

Ethernet is a type of network cabling and signaling specifications developed by the XEROX in late 1970. Ethernet uses a communication model called datagrams to get the messages across the network. The Ethernet datagram is of the form of self-reliant packets of information. An Ethernet package consists of source address, destination address, field & type of data, data length etc.

1000BaseT, 10GBaseT are the different standards of Ethernet. The number thousand stands for the speed, "1000" are 1000 mega bits per second i.e. 1 Giga bit data is transmitted per second."Base" stands for the baseband signal which uses single carrier frequency so that all devices connected to the network can have the knowledge of all transmission carried out."T" stands for the twisted cable pair. The Ethernet supports for half-duplex as well as full duplex mode. In half-duplex mode when two or more computers attempt to send the data at a time a collision occurs thus introducing error in the transmitted data where as in the full-duplex mode the point-to-point communication is established between the devices thus reducing the collision effect.

1.1 Gigabit Ethernet

Due to the speedy development of the electronic and the network technologies, the systems with the combination of the integrated electronic technology with the network technology are progressively increasing its share. To achieve high speed of data transmission these systems has to

be connected to various hosts. There are different speeds of the data transmission i.e. 10Mbps, 100Mbps and 1000Mbps, 10 Gbps. As the world is running behind the speedy devices most preferred is the Gigabit data transmission (1000Mbps and 10Gbps).

The two necessary reason for the Gigabit Ethernet :

- Speedy systems and faster backbones.
- To produce low cost products Gigabit Ethernet can be used. Using Gigabit, user has a freedom in selecting the products, interoperability, and backward compatibility. Applications like network operating systems and network management supports Gigabit.

1.2 IEEE 802.3 Ethernet Standard.

The most widely preferred networking standards are Local Area Networks (LANs) and the Wide Area Network (WANs) is due to the details available from IEEE 802.3 (Ethernet) networking standards. This networking standard provides the flexibility and the vendor neutrality through the Ethernet system. The recent computers contain the Ethernet cards which helps to connect device directly to the network. These Ethernet cards may support the data transmission of 10Mbps, 100Mbps and 1000Gbps. Because of these inbuilt cards it is easy to connect to the network and upgrade the system. Since the FPGA supports 10Mbps, 100Mbps, 1000Mbps, the MAC design can be used as low cost, high performance embedded controller system.

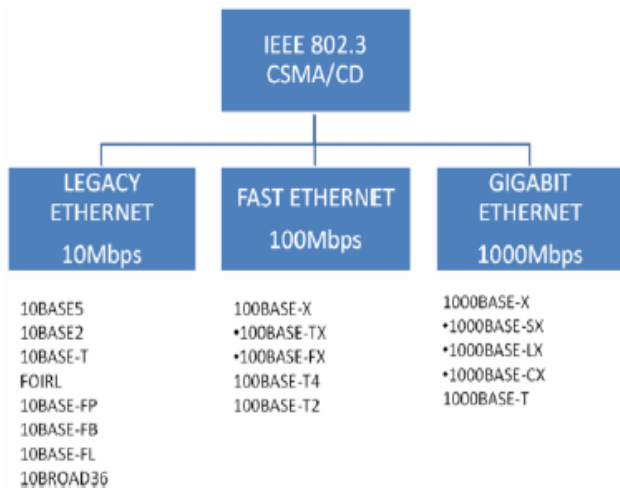


Figure 1. 802.3 IEEE Ethernet standards

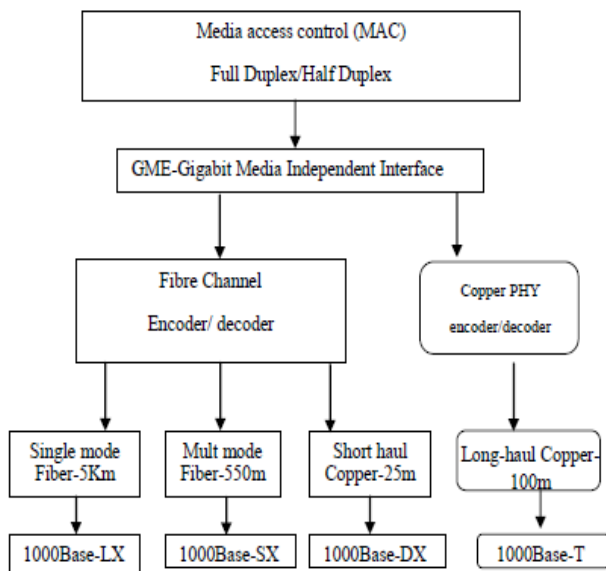


Figure 2. Gigabit Ethernet standards

1.2 Proposed work

In this paper, Serial interface module for Ethernet based applications deals with the building standard interfacing module for the serial communication of data from FPGA (transmitter) to the PC (receiver) and from PC(transmitter) to FPGA (receiver) using Virtex-5 FPGA. The data is transmitted through a Ethernet cable using a SFP module . This design is implemented by using a FIFO and UART programs written in VHDL language to verify the communication established from FPGA to PC and the result is observed in Wireshark software in the form of data packets, whereas the communication from PC to the FPGA is established by a ping command. This ping command helps to transmit certain packets to the FPGA and the data transmitted from the PC can be observed on the Chipscope Pro analyser.

2. SYSTEM DESIGN

2.1 Block diagram

The figure 3 shows the block diagram of the proposed work which include VIRTEX-5 FPGA, which includes Tri-mode Ethernet Media Access controller (TEMAC).

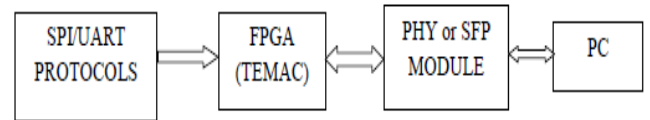


Figure 3. Block diagram

The data received from the SPI or UART protocol is transmitted to the transmit engine which converts the received data into frame format by adding the preamble, start frame delimiter (SOF), and adding pad bits. In the receive engine of the TEMAC the padded bits are removed from the pad format. The PHY or the SFP module is the transceiver which is interfaced with the TEMAC through the serial Gigabit Media Independent Interface (SGMII) at one end and other end is interfaced to the receiving device which is PC or FPGA.

2.2 Implementation Of TEMAC Core

Figure 4 illustrates a typical application for the TEMAC core with 10/100/1000 Mb/s. The TEMAC core is generated from the ISE Xilinx 14.6 tool which consists of the Ethernet MAC transceiver interfaces with the PHY implemented by an external SGMII. The external SGMII is connected to an Ethernet PHY device, which performs the BASE-T standard at 1Gb/s. The Ethernet MAC has an inbuilt Ethernet core along with Ethernet wrapper and the GTP 1000Base-T wrapper then finally to the Rocket I/O transceiver for the SGMII interface with the Phy. The Four-wire Ethernet cable is used as a media for the FPGA and the PC communication. This Figure 4 explains about the duplex way of communication between PC and the FPGA. When the FPGA communicates with the PC the result is observed on the Wireshark, whereas the PC to FPGA communication is carried out by using the ping command on the PC. The result is obtained on the Chipscope pro analyser. The design is verified by using the FIFO code as well as the UART code. To minimise the problem of low speed data transmission, a 16bit UART is written to verify the core configuration.

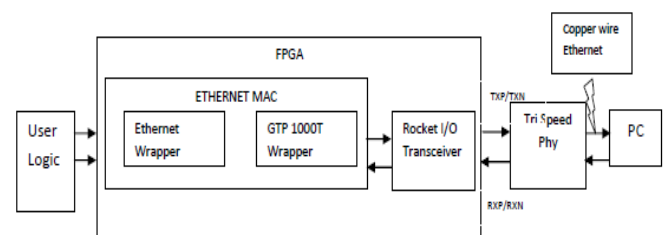


Figure 4. Implementation of TEMAC core

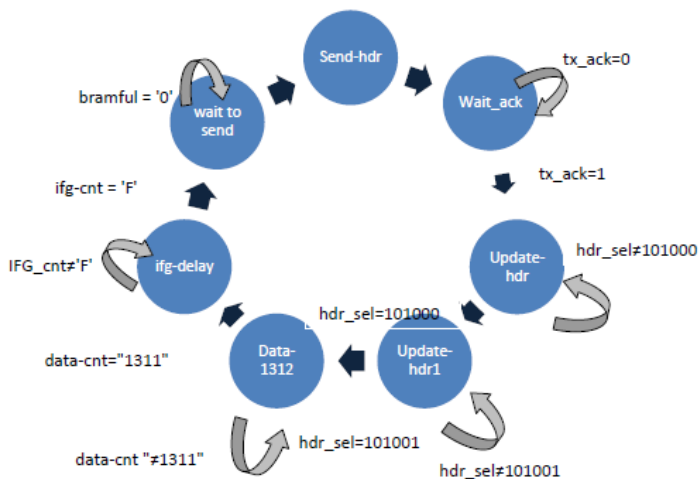


Figure 5. State diagram of reading the data from the block RAM the block RAM

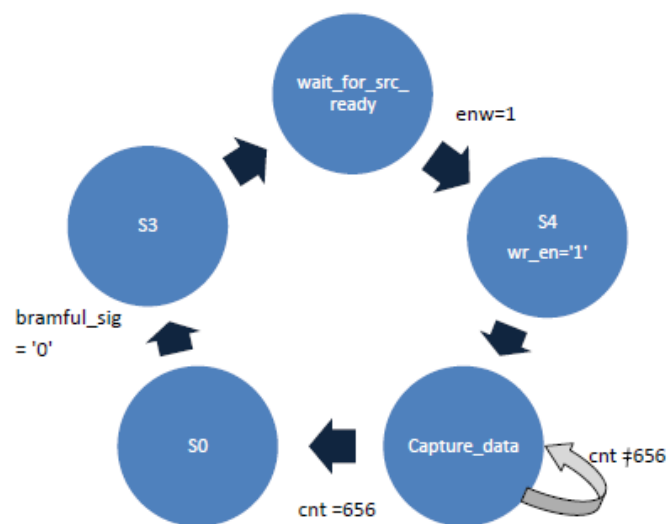


Figure 6. State diagram of writing the data to the block RAM

The state diagram shown in figure 5 explains about the data read from the block RAM by adding the header and the required delay. This state diagram has 7 states and explanation of the each state is understood from the state diagram. The state diagram in the Figure 6 explains about the States required to write the FIFO/UART data to the BRAM which is 16 bit wide.

3. RESULTS & DISCUSSION

This proposed design is verified by XILINX 14.6 simulator. The results are represented by the waveform as shown below. The hardware used is the Virtex-5 and the analyzing the same using the Chipscope pro analyser.

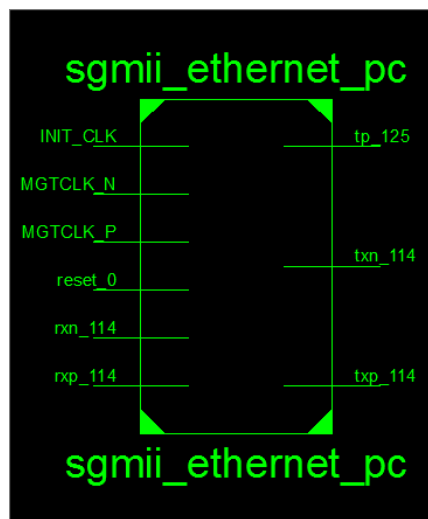


Figure 7: RTL Schematic of the top module

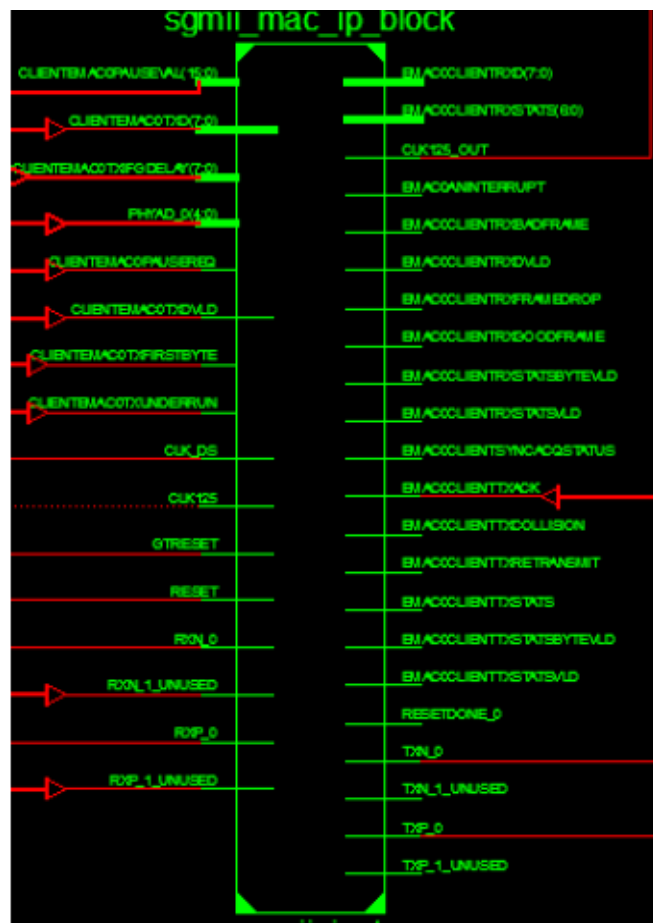


Figure 8. SGMII IP core

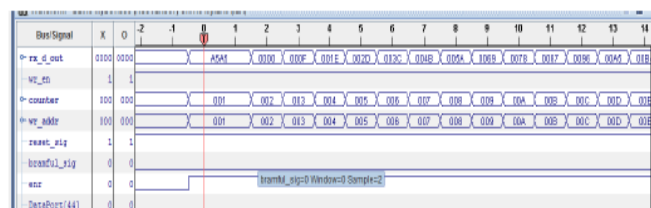


Figure 9.a FIFO Data written to the BRAM

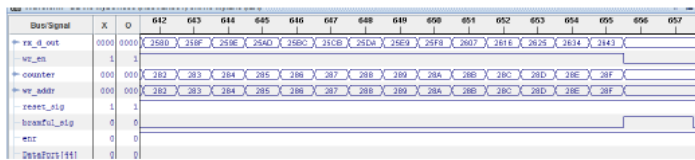


Figure 9.b. Data written to the BRAM block

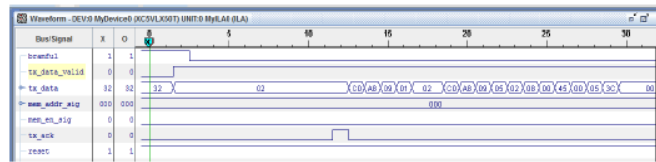


Figure 10.a. Header packet read from the BRAM block

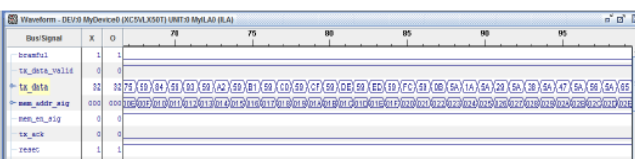


Figure 10.b. Data read from BRAM

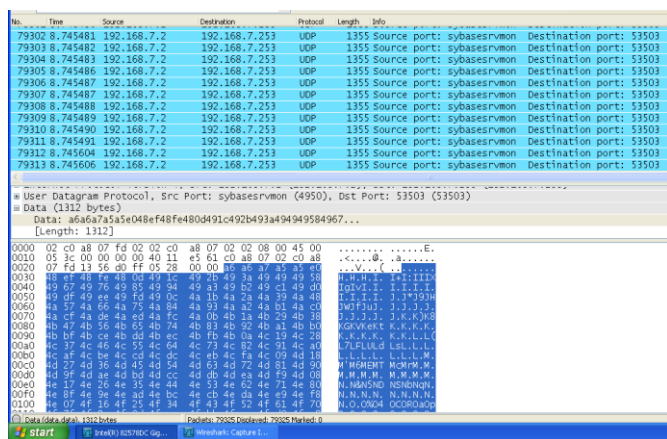


Figure 11. FIFO Data packet received in Wireshark Software

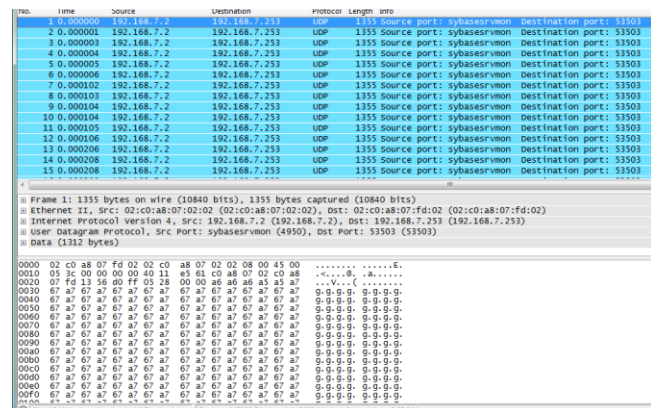


Figure 12. UART data received on the wireshark

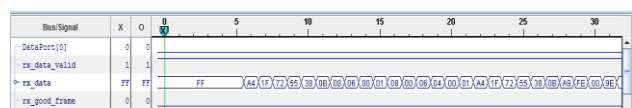


Figure 13. The data received from PC to FPGA using Ping command

The Figure 10.a explains about the header data read from the Block RAM and the Figure 10.b explains about the data packet read from the Block RAM. The figure 11 explains about the data packet read from the FPGA to the PC observed on the wireshark software. Instead of the FIFO code the UART code is used and the result obtained is as shown in figure 9. Figure 13 shows the data received from the PC to FPGA using ping command.

4. CONCLUSIONS

This paper deals with building a standard interface module for the serial communication between the devices. With the existing MAC IP core. The communication is established between FPGA and the PC. The FIFO module is used for the verification of the communication established between the FPGA and the PC. Data from the FIFO is written to the block RAM. The data read from block RAM is transmitted through the twisted copper Ethernet cable to PC, the same is repeated for UART also. The Wireshark software is used to view the data packet in the UDP format. The duplex communication has also been established between the devices through the ping command.

ACKNOWLEDGEMENT

This paper is acknowledged to my faculty members at DELOPT as well as my family members.

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BIOGRAPHIES



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