COMPARATIVE ANALYSIS OF LECTOR AND STACK TECHNIQUE TO REDUCE THE LEAKAGE CURRENT IN CMOS CIRCUITS

Mansi Gangele[1], K. Pitambar Patra[2]

[1]*M.Tech Scholar, Department of ECE, RKDF Institute Of Science & Technology,RGPV Bhopal, M.P., India*
[2]*Assistance Professor, Department of ECE, RKDF Institute Of Science & Technology, RGPV Bhopal, M.P., India*

Abstract

CMOS is the latest technology available in today's world. And the biggest advantage of this technology is it does not consume any power. So the total power consumption is dependent on its leakage power. Since leakage exists in the circuit even if it is in stand by state i.e. the state in which gate of the circuit is not getting power supply. So the power loss in the circuit is high. And that's why our major concern is to reduce the leakage current in the circuit. Varieties of different techniques are available to reduce the leakage current and still continue to derive more, better techniques. In this paper two different techniques LECTOR and STACK technique which are based on the same principle have been comparatively analyzed.

Keywords: *Delay, Leakage current, Lector technique, Stack technique.*

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1. INTRODUCTION

As we are using nano design in the CMOS technology threshold voltage is decreasing because of which leakage current is exponentially increasing.

$$I_O \alpha (e^{-qVt/\eta KT})$$

To reduce the leakage current so many techniques are available at the cost of other parameters such as dynamic power, reliability, delay etc. which in turn affects the switching performance of the circuit. We use these techniques as per our requirement. LECTOR and STACK techniques are the two techniques which reduce the leakage power without increasing the dynamic power.

In this paper LECTOR technique is implemented on logic gates NAND & NOR and half adder, half subtractor and decoder. And then this technique is compared to the STACK technique.

2. RELATED WORK

Many techniques have already been discussed to reduce the leakage current in the nano scale design in CMOS circuits. In the paper entitled 'Design of Leakage Power Reduced Static RAM using LECTOR' published by B. Dilip, P. Surya Prasad, *Dept. of ECE, MVGR College of* Engineering, *Andhra Pradesh, India in journal* (IJCSIT) International Journal of Computer Science and Information Technologies, Vol. 3 (3) LECTOR is a technique for designing CMOS circuits in order to reduce the leakage current without affecting the dynamic power dissipation, which made LECTOR a better technique in leakage power reduction when compared to all other existing leakage reduction techniques. This paper presents the analysis for leakage current in Static RAM implementing LECTOR technique.

In another paper entitled 'Reduction of Leakage Power in CMOS Circuits Using Stack Technique' by Mansi Gangele & K. Pitambar Patra *Department Of ECE, RKDF Institute Of Science & Technology, Bhopal/ RGPV Bhopal, M.P, India* published in International Journal of Modern Engineering Research (IJMER), 5(5):1-8, 2015 STACK technique is proposed.

According to M. D. Powell, S.-H. Yang, B. Falsafi, K. Roy, and T. N. Vijaykumar, "Gated-Vdd: A circuit technique to reduce leakage in deep submicron cache memories," in *Proc. IEEE ISLPED*, 2000, pp. 90–95, Power gating technique uses additional transistors, called sleep transistors, which are inserted in series between the power supply and pull-up (PMOS) network and/or between pull-down (NMOS) network and ground to reduce the standby leakage currents. The sleep transistors are turned on when circuits are in active mode and turned off when circuits are in standby mode. By disconnecting the logic networks from the power supply and/or ground using sleep transistors, this technique reduces the leakage power in standby mode.

3. METHODOLOGY & IMPLEMENTATION

3.1 Stack Effect

When any state has more than one OFF transistors in the path from power supply to ground then it is less leaky as compare to the state which has only one OFF transistor in the same path. And this effect is known as Stack effect. Stack technology and Lector technology both are based on this effect

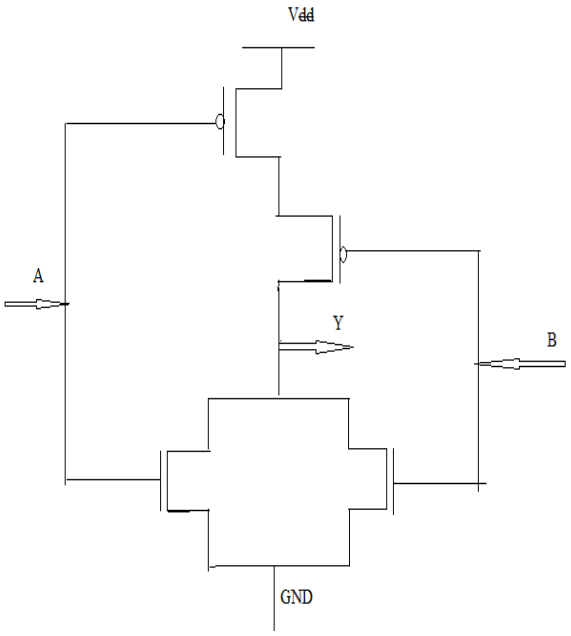

Fig-1: CMOS NOR GATE

Fig-1 shows the CMOS nor gate. It has two PMOS transistors which are connected in series and two NMOS transistors which are connected in parallel. And the combination of both PMOS and NMOS transistors are connected in series and output is taken from the joint node.

3.2 Stack Technique

Stack technique is the technique where instead of each and every one PMOS or NMOS transistors two PMOS or NMOS transistors of half width are used respectively. These two transistors either PMOS or NMOS are connected in series.

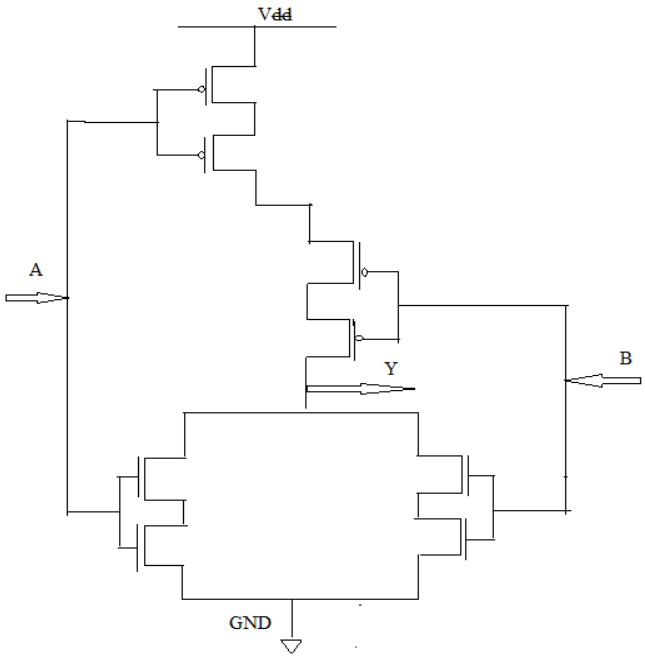

Fig-2: STACK NOR GATE

Fig-2: shows the circuit diagram of Stack based two input NOR gate. Basically in simple CMOS NOR gate two PMOS and two NMOS transistors are used but In this Stack NOR gate four PMOS and four NMOS are used.

3.3 Lector Technique

Basic principle behind this technique is stack effect only. In this technique two extra transistors (one PMOS and one NMOS) are introduced between pull down and pull up network. These two transistors are self controlled transistors and are called Leakage Control Transistors (LCT). The gate of each LCT is controlled by the source of other. And because of this kind of arrangement one of the LCT always remains in its near cut off region.

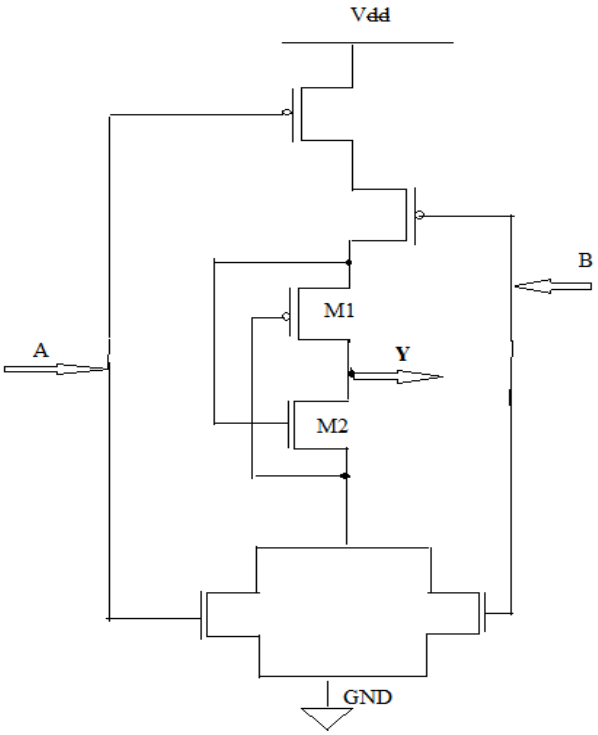

Fig-3: LECTOR BASED NOR GATE

Fig-3: shows the circuit diagram of Lector based two input NOR gate. In this circuit 'A' and 'B' are input nodes and 'Y' is output node. Two PMOS transistors are connected in series and two NMOS transistors are connected in parallel. And two series connected transistors M1 (PMOS) and M2 (NMOS) which are Leakage Control Transistors (LCTs) are connected between pull down and pull up network. Gate terminal of M1 is connected to source of M2 and gate of M2 is connected to source of M1.

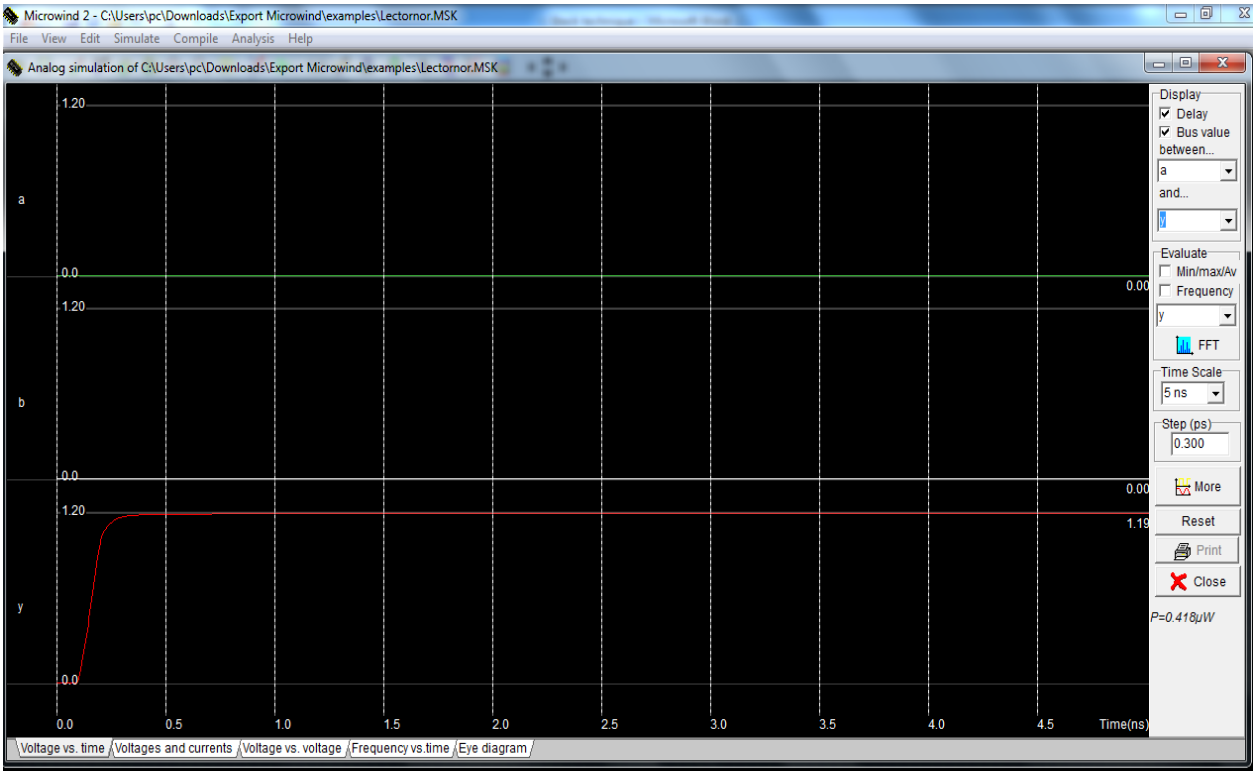

Fig-4: Timing simulation of Lector based nor gate

Table1: Static power, Total power and delay of NAND NOR & AND gate and their Lector and Stack gates

GATE TYPE	*STATIC POWER (µW)*				*TOTAL POWER(µW)*	*DELAY (ns)*
	(0,0)	**(0,1)**	**(1,0)**	**(1,1)**		
NAND	0.185	0.252	0.185	1nw	2.094	0 .029
LECTOR NAND	0.391	0.391	0.399	0nw	1.871	0.033
STACK NAND	0.248	0.278	0.173	0nw	1.333	0.101
NOR	0.358	0.165	0nw	0nw	2.017	0.013
LECTOR NOR	0.418	0.418	0nw	0nw	1.946	0.074
STACK NOR	0.342	0.166	0nw	0nw	1.195	0.044
AND	0.643	0.761	0.688	0.119	6.407	0.024
LECTOR AND	0.971	0.983	0.991	0.342	5.015	0.059
STACK AND	0.769	0.719	0.810	0.148	3.878	0.097

Fig-4 shows the analog simulation of Lector based NOR gate. In this circuit output 'Y' is high when both the inputs 'A','B' are low. And as shown in the simulation static power at this time is 0.418µw. Total power is 1.946 µw.

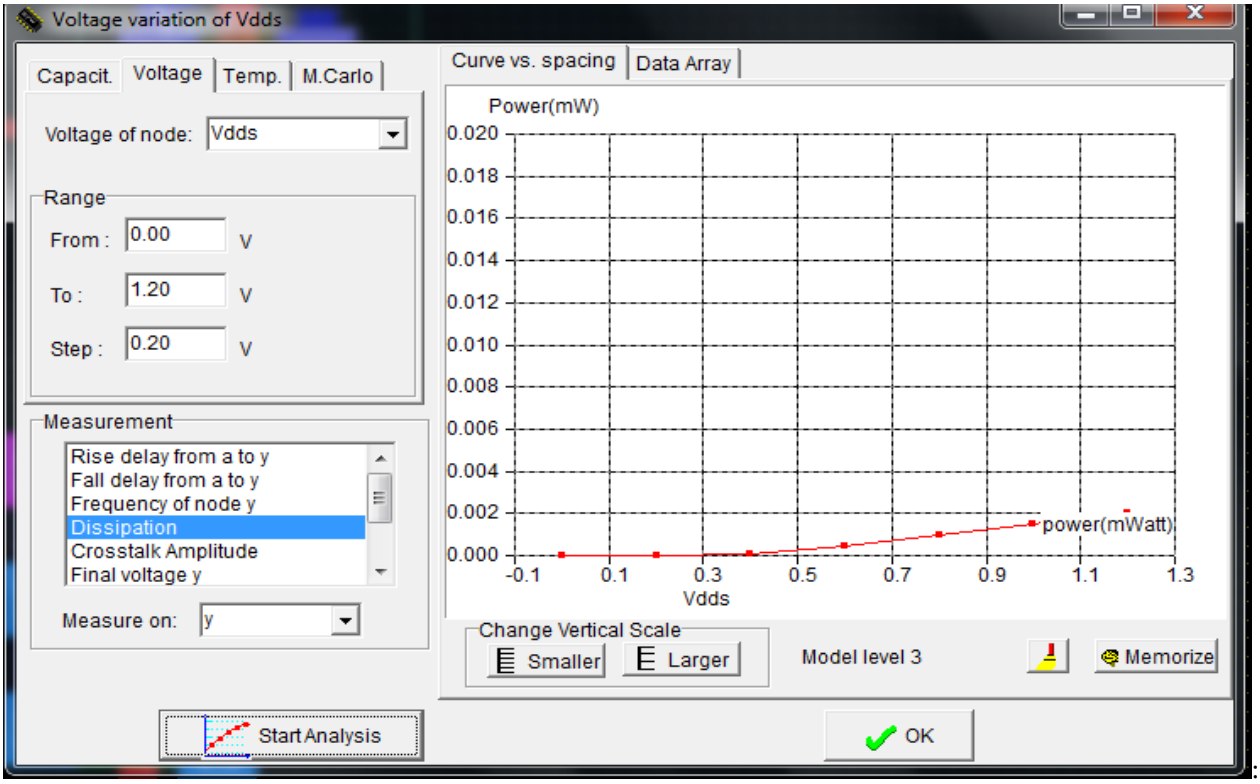

Fig-5.1: Power supply (V_{dds}) Vs Dissipated power

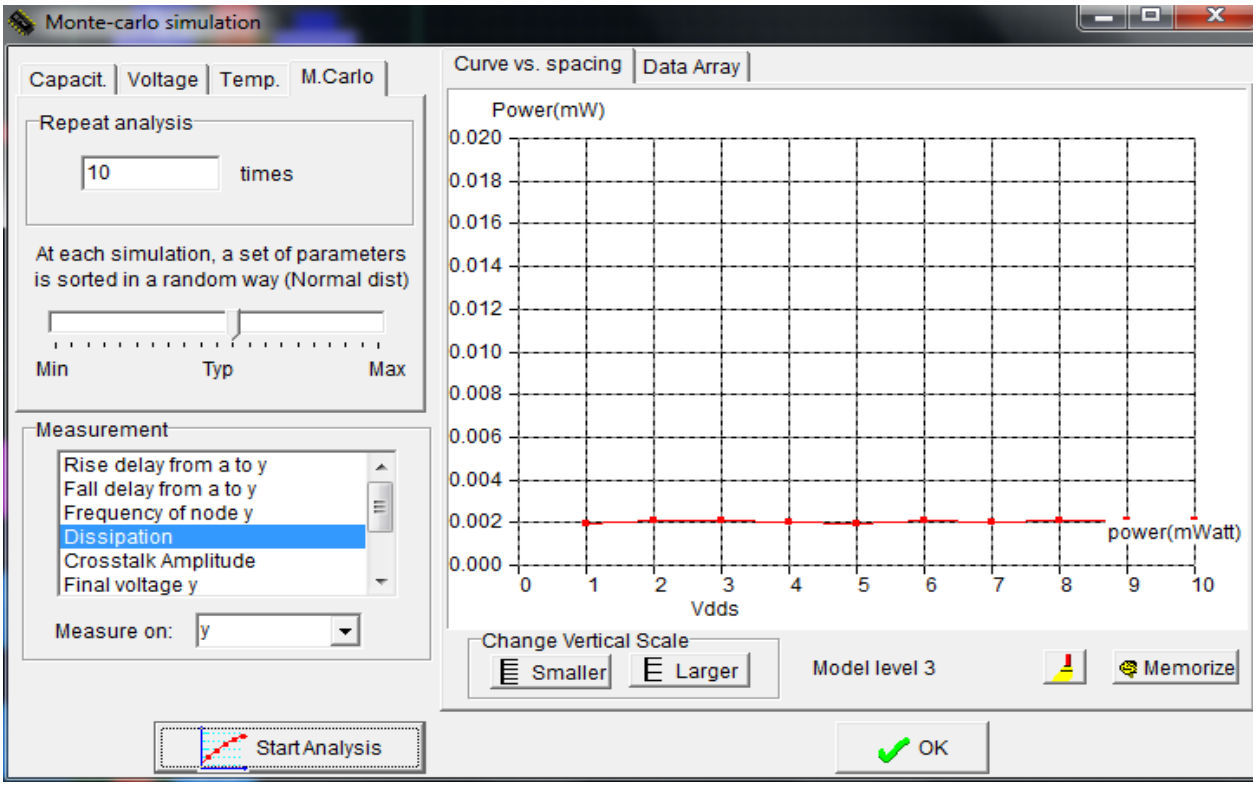

Fig-5.2: Monte Carlo simulation of power dissipation

In the above figures graph power supply v_s dissipated power and other is M. carlo simulation of power supply Vs dissipated power respectively is shown. From node 'A' to 'Y' power is very negligible i.e.0.002mw and same is the power in M.carlo simulation.

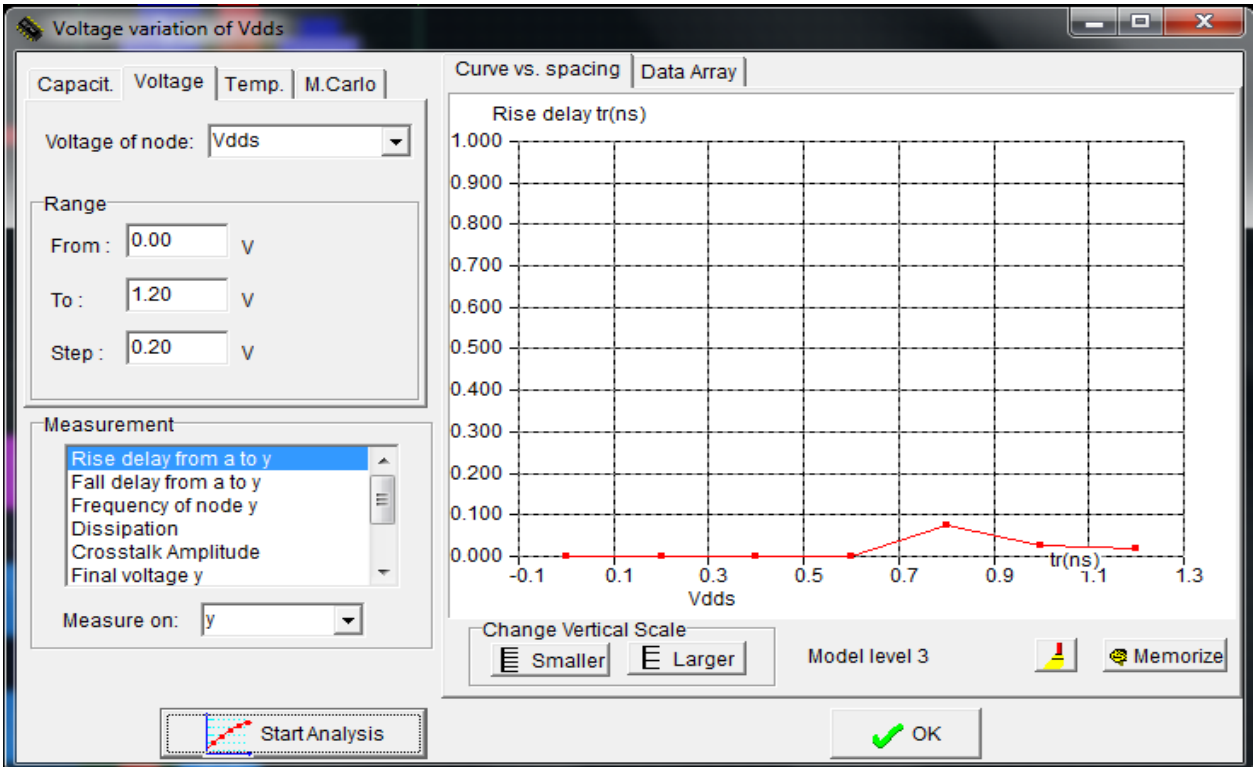

Fig-6: Power Supply (V_{dds}) Vs Rise delay

In the above fig. graph Power supply Vs Rise delay is shown. And the delay from node 'A' to 'Y' is 0.074.

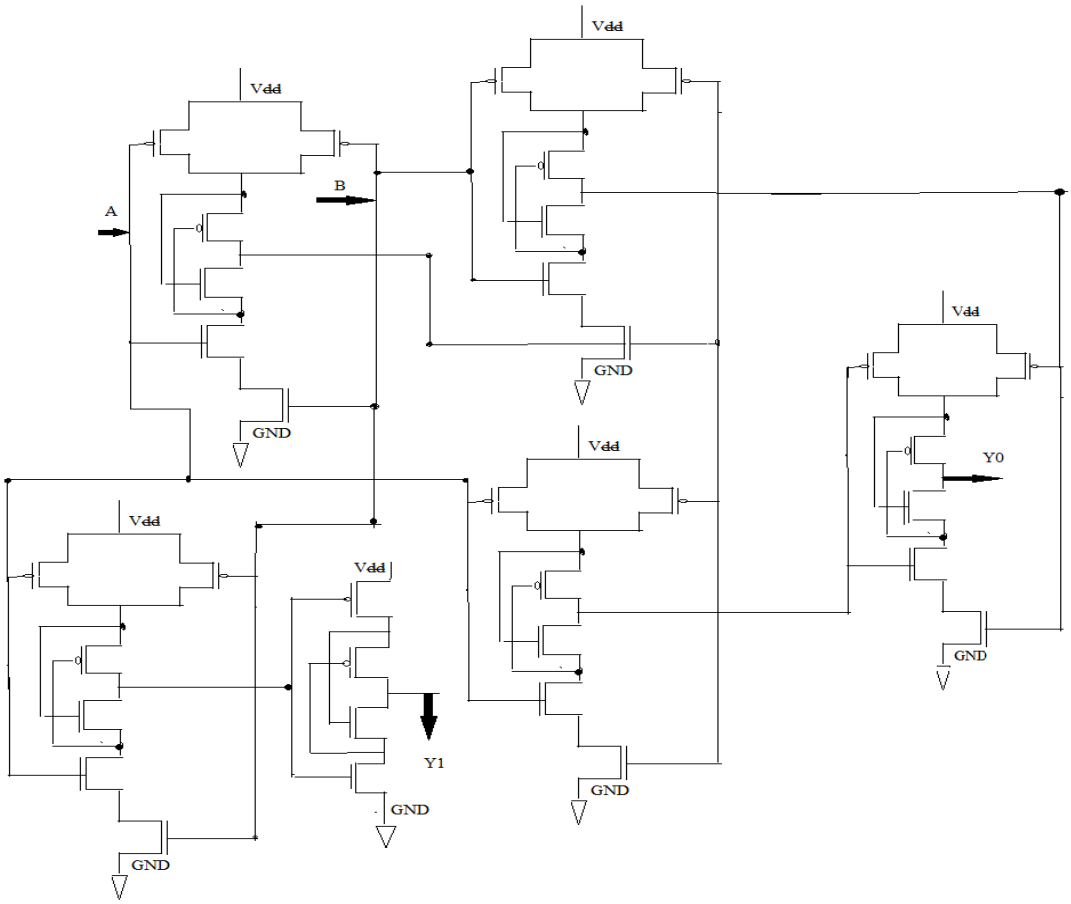

Fig-7.1: Lector based half adder

Fig-7.1 shows the circuit diagram of Lector based Half adder with 'A' and 'B' are the input nodes and 'Y0' and 'Y1' are the output nodes. And the layout of this circuit is given below in Fig-7.2. Y0 is the sum of two binary digits and Y1 is the carry. Total power of above shown figure is 17.379 µw.

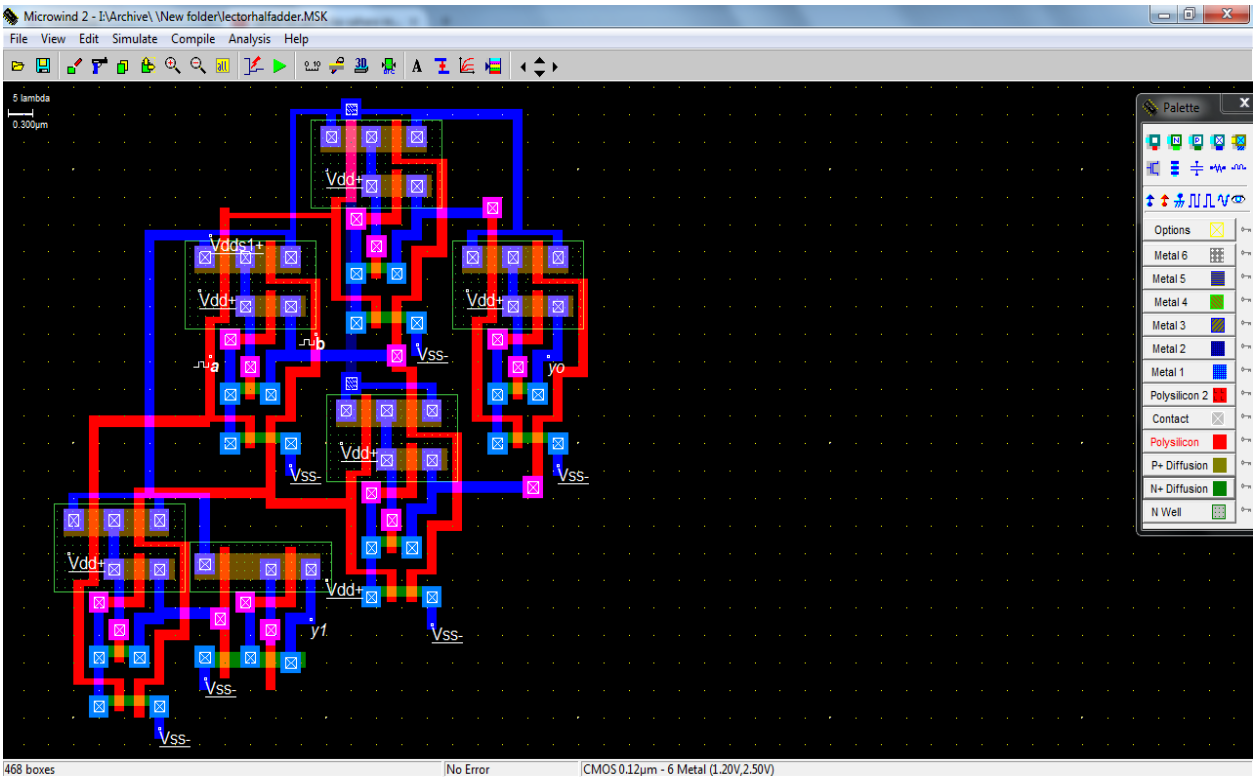

Fig-7.2: Layout: Lector based half adder

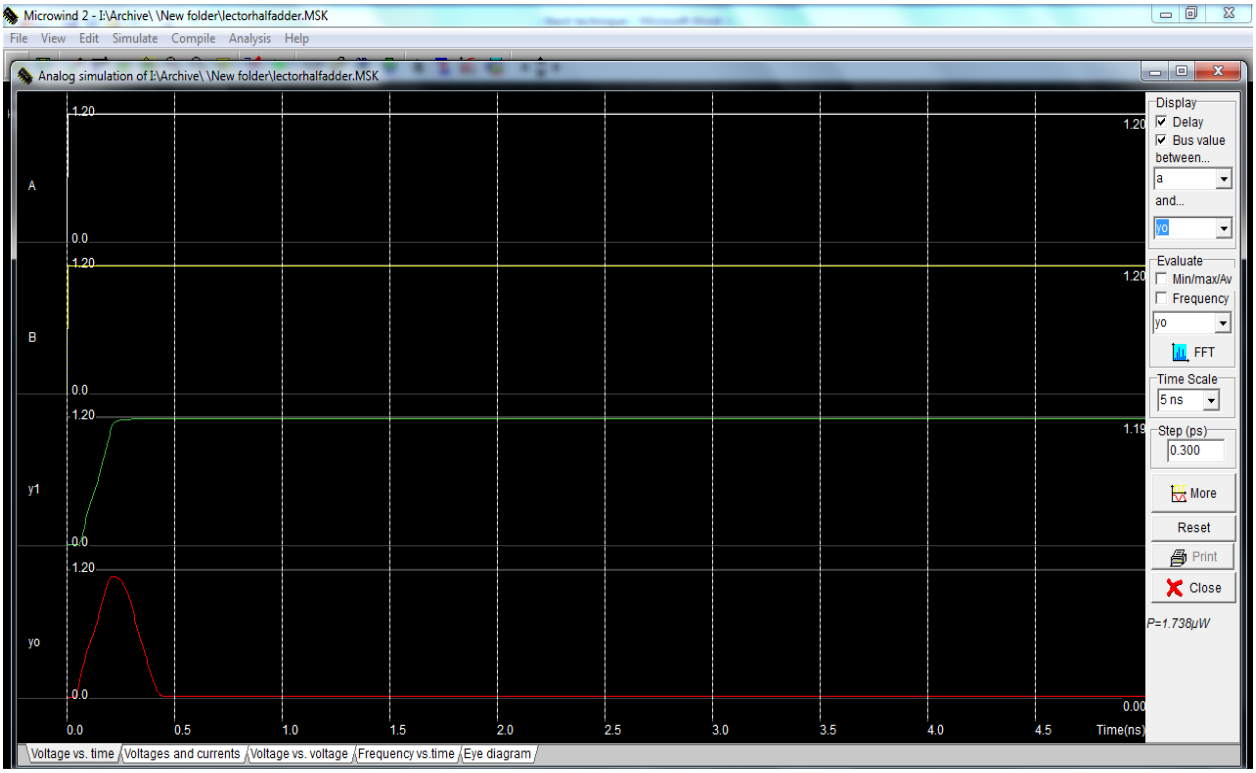

Fig-8: Timing simulation of Lector based Half Adder

Fig. shows the timing simulation of Half adder. In the given simulation input 'A' and 'B' are given 1so, the outputs are

Y0= sum of input A and B;
= sum of 1 and 1 (1 & 1);
= 1+1; = 0;

Y_1= carry of input A and B
= carry of the addition of 1 and 1; = 1;

So, the output (Y0, Y1) are (0,1) which is shown in simulation. And total power in this case is 1.738 µw.

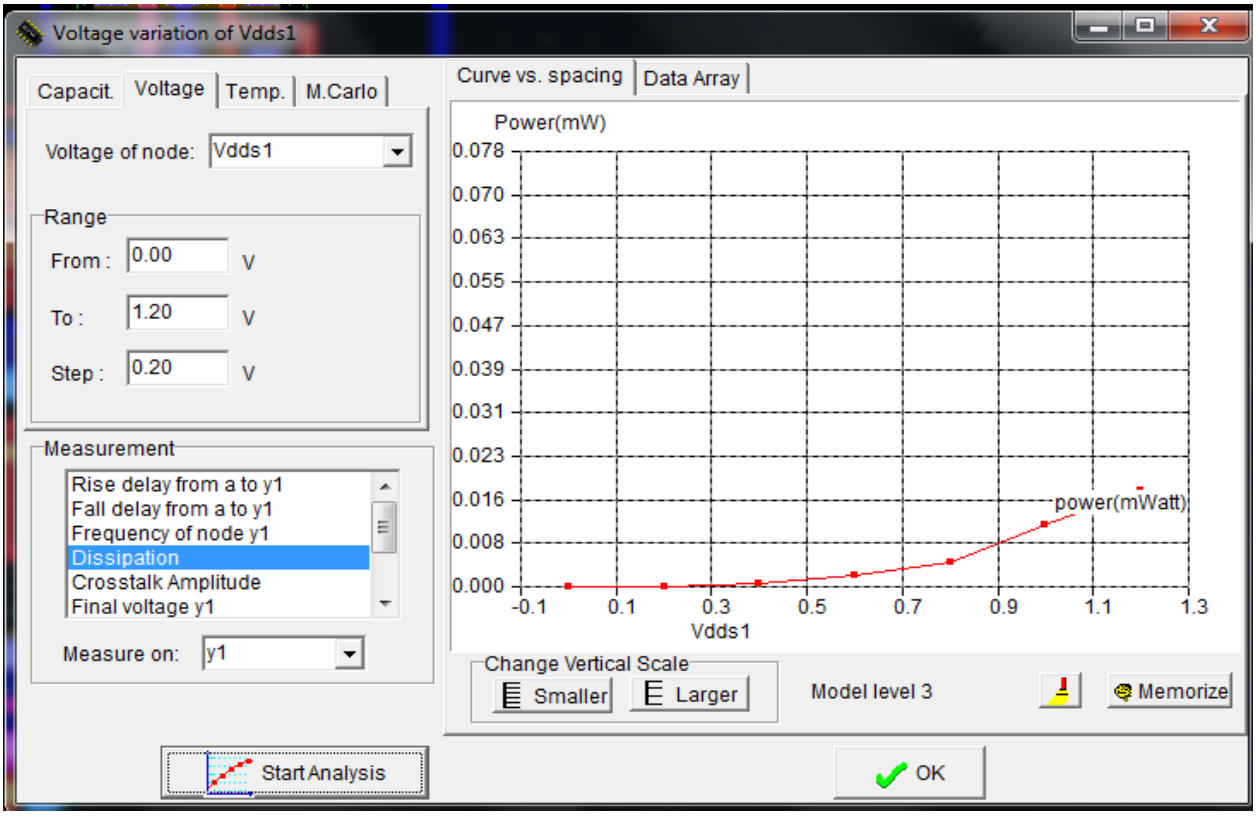

Fig.-9.1: Power supply Vs Dissipated power for Output Y_1

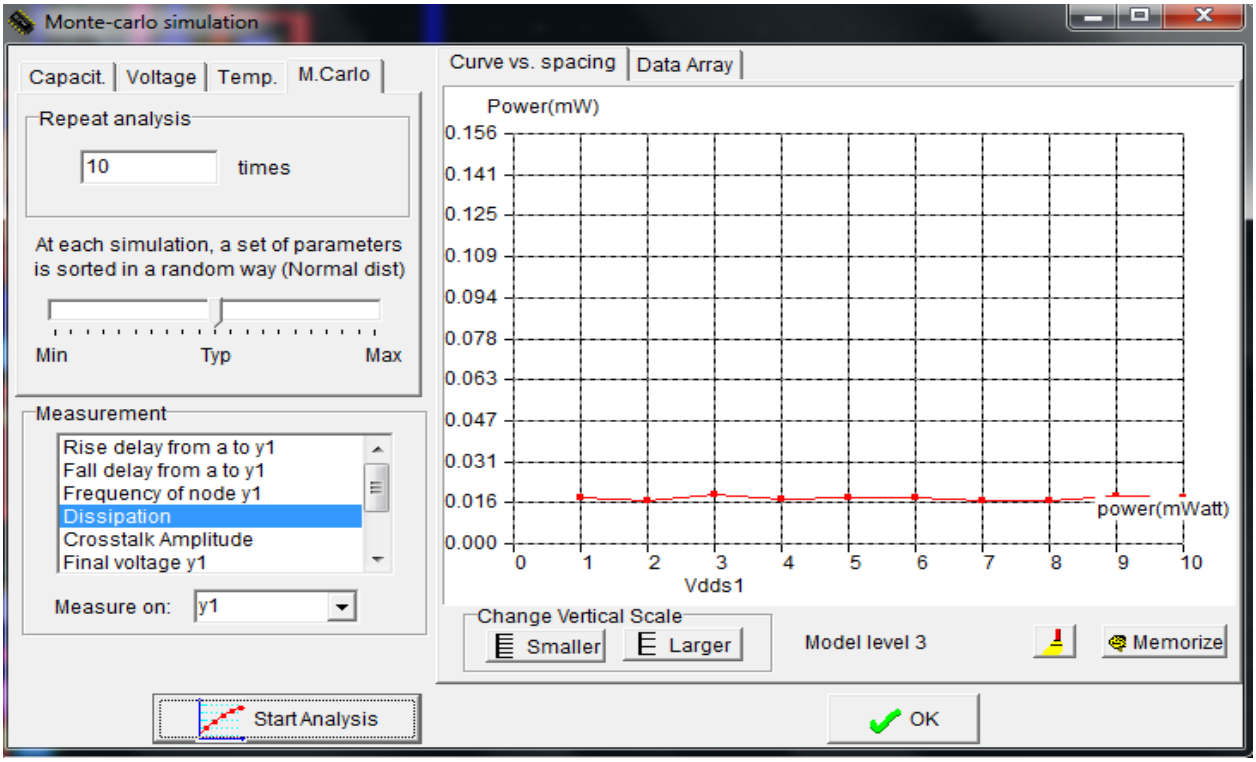

Fig-9.2: Monte Carlo power dissipation simulation for output Y_1

Both the above graph shows the graph between power supply and power dissipation for Output Y_1.Fig 9.1 Shows that dissipated power of half adder for output Y1 is 0.017mw which is similar for Y0 there is not any remarkable difference.Fig.9.2 shows the Monte Carlo power dissipation simulation for output Y1 of half adder. And it is also exactly same i.e. 0.017mw.

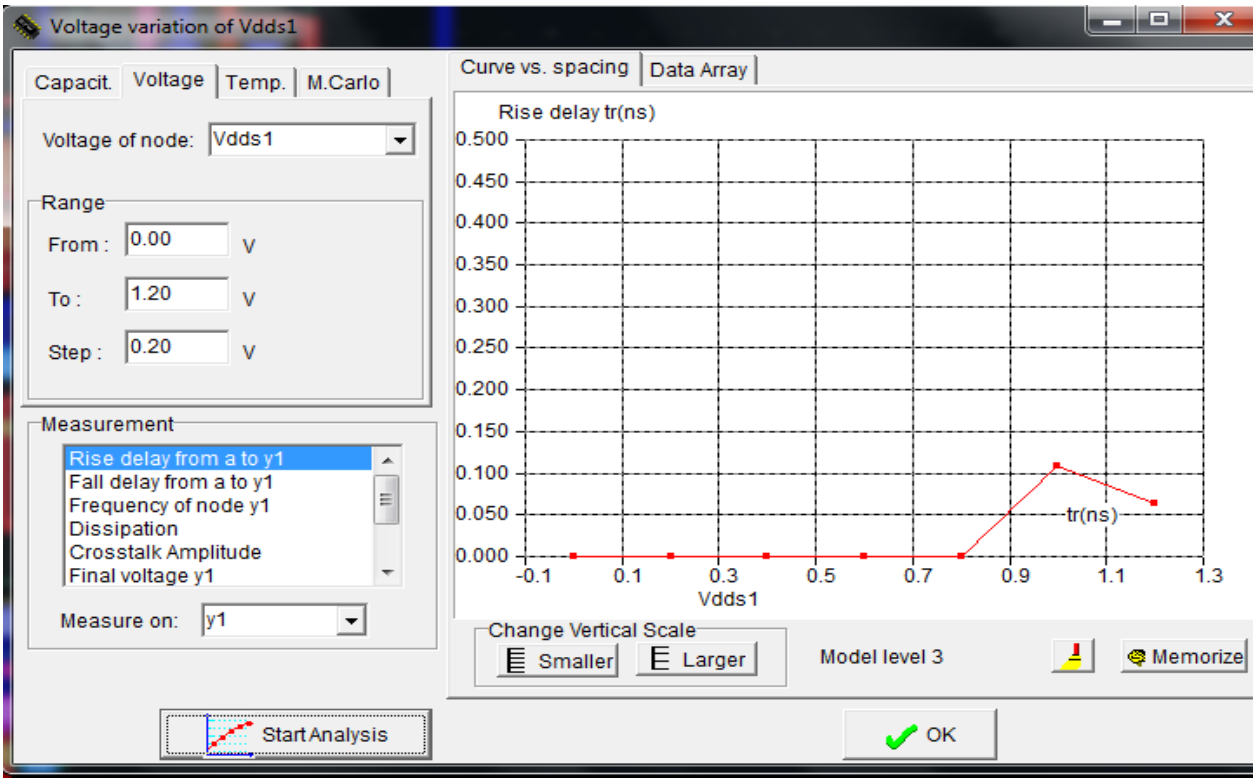

Fig-10: Power Supply Vs Propagation delay for Output Y_1

Fig-10 shows the graph between Power supply and propagation delay for output Y1 of half adder. And propagation delay for Y1 is 0.109ns. The propagation delay for output Y0 is 0.143ns.

Table2. Power Dissipation and Propagation Delay of different circuits

CIRCUIT TYPE	*POWER DISSIPATION(mw)*				*PROPAGATION DELAY (ns)*			
	Y_0	Y_1	Y_2	Y_3	Y_0	Y_1	Y_2	Y_3
STACK HALF ADDER	0.013	0.013	--	--	0.029	0.091	-	-
LECTOR HALF ADDER	0.017	0.017	--	--	0.143	0.109	--	--
STACK HALF SUBTRACTOR	0.012	0.012	-	--	0.052	0.293	--	--
LECTOR HALF SUBTRACTOR	0.016	0.016	--	--	0.168	0.259	--	--
STACK DECODER	0.028	0.028	0.028	0.028	0.493	0.472	0.087	0.406
LECTOR DECODER	0.029	0.029	0.029	0.029	0.425	0.322	0.673	0.625

In the Table1 the values of Static power, total power and delay of logic gates NAND, NOR & AND gate and their respective stack logic gates and lector logic gates are given . The values of logic gate and their respective stack logic gates are taken from the paper **Reduction Of Leakage Power In CMOS Circuits Using Stack Technique by** Mansi Gangele & K. Pitanbar Patra published in International journal of Modern Engineering Research (IJMER), 5(5):1-8, 2015.It can be seen that both the techniques LECTOR and STACK have reduced the leakage power.

In the Table2 Power dissipation and propagation delay of Half Adder, Half Subtractor, and Decoder is calculated and given in table. In all these circuits stack technique and lector technique are used. All these circuits have four output nodes and Power dissipation from a single node to different output nodes is almost constant for each circuit. Maximum worst case power dissipation for Stack Half Adder is 0.013mw, for Lector Half Adder is 0.017mw, for Stack Half Subtractor 0.012mw, for Lector Half Subtractor 0.016mw and for stack Decoder 0.028mw and for Lector Decoder is 0.029. Propagation delay from a single node to different output nodes is also calculated. Maximum delay from a specific node for Stack Half Adder is 0.091ns to node Y_1 Similarly the maximum delay for Lector Half Adder is 0.143ns to output node Y_0, for Stack Half Subtractor is 0.293ns to node Y_1, for Lector Half Subtractor is 0.259ns to node Y_1 and for Stack Decoder is 0.493ns to node Y_0 and for Lector Decoder is 0.673ns to node Y_2. Again the values of Stack circuits are taken from the same paper.

4. CONCLUSION

It is clear from both the tables that while using Stack technique we can save 40% power but in this case delay is increased by 250 to 300%. And using Lector technique power can be saved by 10 to 15% and delay is increased in this case also but in this case delay is increased 150%.

So, from both the tables it is clear that Stack technique saves more power as compare to Lector technique. But it delays the output more as compare to Lector technique. So we can use the technique accordingly as per our requirement as if we want to get fast output but little leakage is tolerable than we use Lector technique and we want to save the power and bit delay is tolerable than use stack technique. But this is the case only for small logic gates. It can be clearly seen in table2 that for Half adder, Half subtractor and for Decoder in stack technique leakage current as well as propagation delay both are less as compare to Lector technique. So it can be said for big circuits Stack is better option.

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