

# DESIGN OF LOW POWER IMPROVED MEDIANFILTER CORE FOR NOISE REDUCTION IN IMAGE

Vinothini M<sup>1</sup>, Syed Ibrahim B<sup>2</sup>, A.Kavitha<sup>3</sup>

<sup>1</sup>PG Scholar, ECE Department, Chettinad College Of Engineering, Karur, India

<sup>2</sup>Senior Assistant Professor, ECE Department, Chettinad College Of Engineering, Karur, India

<sup>3</sup>Professor and Head, ECE Department, Chettinad College Of Engineering, Karur, India

### Abstract

In digital image processing, image restoration is a prime factor which is often able to perform some kind of noise reduction on the image. Reduction of impulse or salt & pepper noise is done by non – linear filtering technique such as the median filter. Here the median filter is designed basically using the comparator and the multiplexer. So, it is essential to develop a new design technique to reduce the power consumption in the median filter. Thereby the comparator and multiplexer used in the median filter is designed using various styles of full adder with help of the cadence 0.18nm technology.

**Keywords:** Multiplexer, Full Adder (FA), Comparator, Power

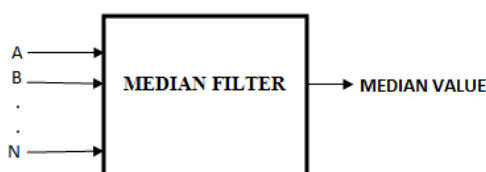
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## 1. INTRODUCTION

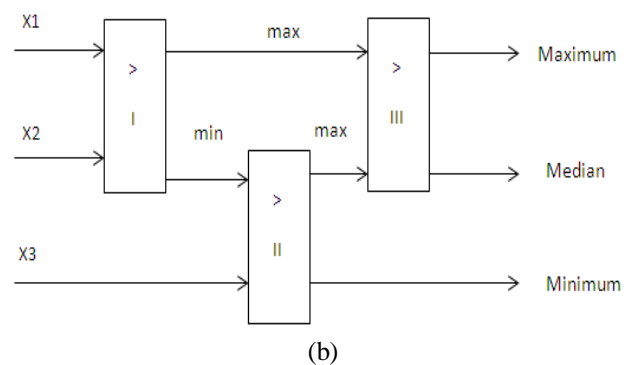
Digital images play an important role in various application such as astronomy, magnitude resonance imaging , mathematical morphology. These images get often corrupted by factors such as channel transmission error, from noisy sensors. Smoothing of these images lead to destroy of edge & instance details of the images ,while sharpening will lead to unwanted intensification of noise. Since the image enhancement through noise cleansing is the fundamental problems in the image processing. So, the depending upon the imagery & the restorstion technique will make more assumption, this technique is not useful for application.

Thus various filtering method are used depending upon whether the noise is non-additive or not. Linear filtering method fails when the noise is non-additive and not effective in removing impulsive noise in the images. This has given importance to the use of non-liner filtering.

The most commonly used nonlinear filter is the median filter because of its superior and edge preservation compared to linear filters. The block diagram of n-bit median filter is shown in figure 1(a) and 1(b)

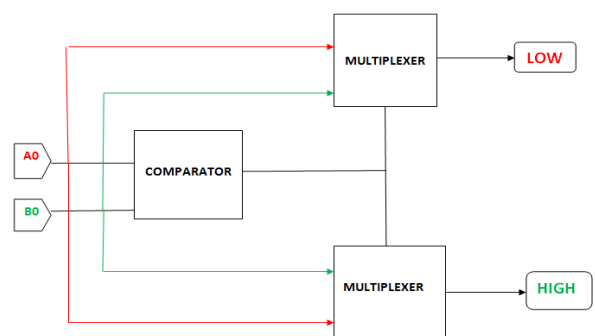


(a)



**Fig: 1(a) and (b) :** Block Diagram of n-Bit and 3-Bit Median Filter

Here the median filter is designed using comparator and multiplexer. The comparator design is implemented by full adder design which is the basic building block of the many digital VLSI circuits. In this paper , the design technique are implemented using the microwind software. The combination of the comparator and multiplexer which is the basic block of the median filter is shown in figure 2.



**Fig 2:** Combination Of Comparator & Multiplexer

## 2. DESIGN IMPLEMENTATION

### 2.1 Basic Median Filter

Firstly ,discussion about the median’s basic block such as the comparator and multiplexer are done. In this paper 3bit 3input are used where the median value are displayed as output. Here the implementation of the median filter are mainly based on the reduction of the power consumption.

The comparator are implemented using various gates as AND, OR, EX-NOR & NOT, where the output is given as  $A > B$ .The multiplexer are implemented with help of AND, OR & NOT gates where output are mainly concerned with selection line  $S_0$ .The basic comparator and multiplexer design used for implementation of basic median filter is shown in figure 3 and figure 4.

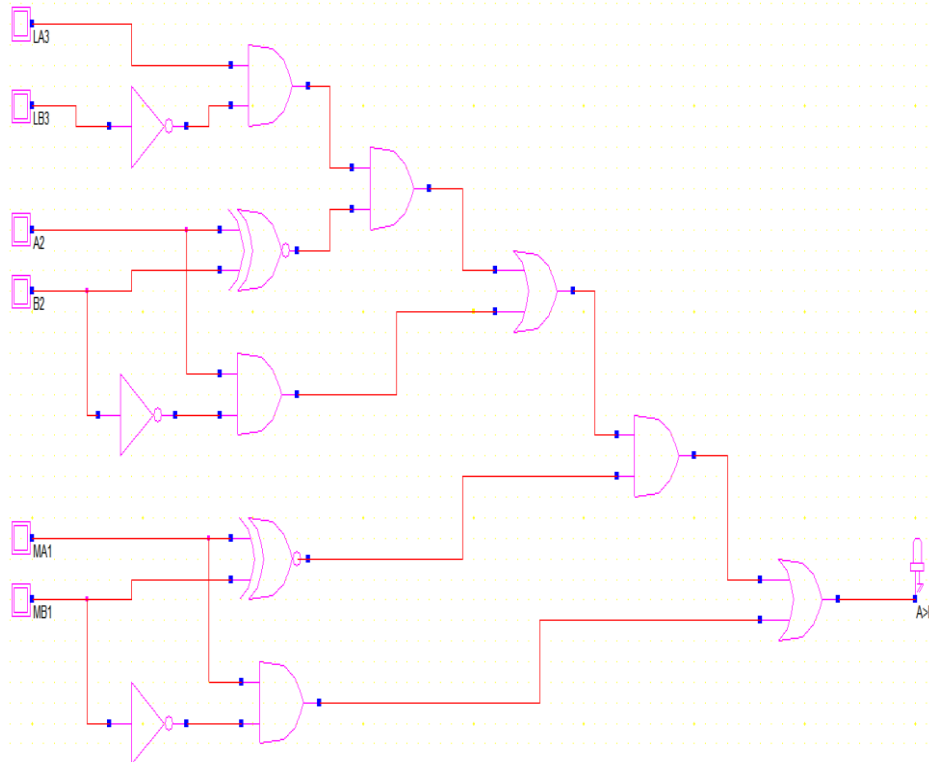


Fig 3: Basic Comparator design

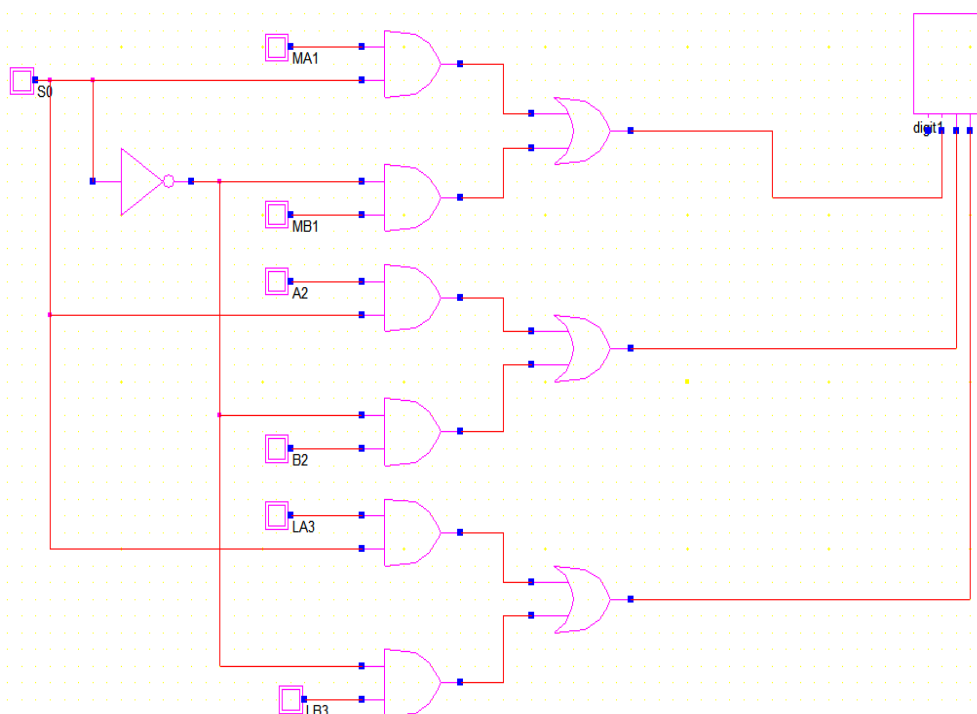


Fig 4: Basic Multiplexer design

The basic median filter design is shown in figure 5

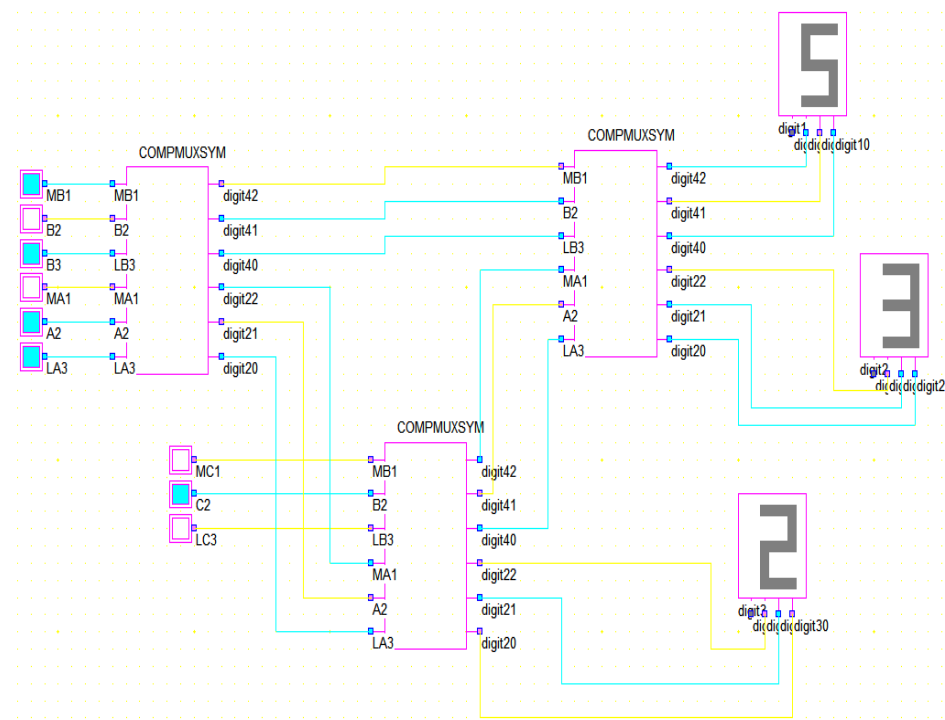
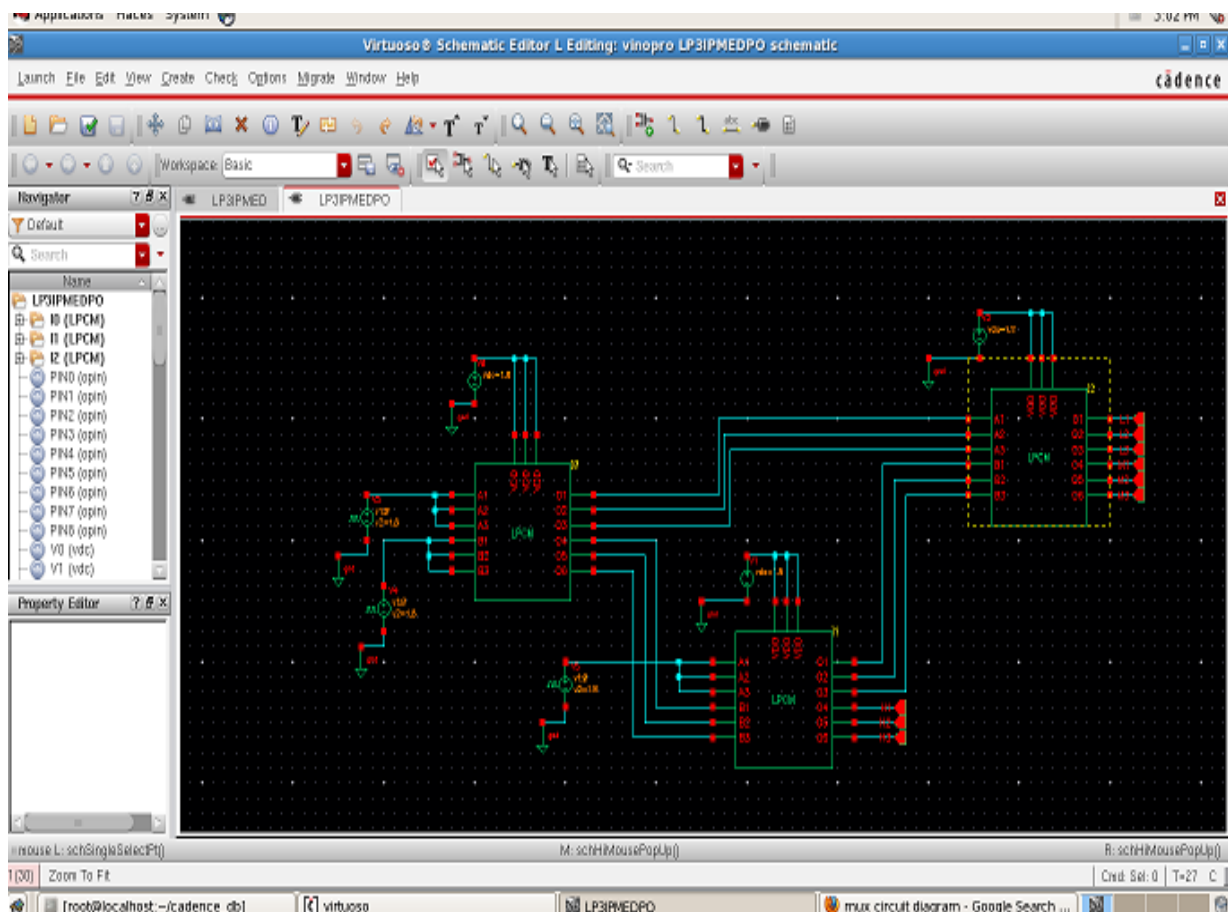


Fig 5: Basic Median filter design

The circuit of the basic median filter integrated using cadence virtuoso platform 0.18nm technology is shown in figure 6

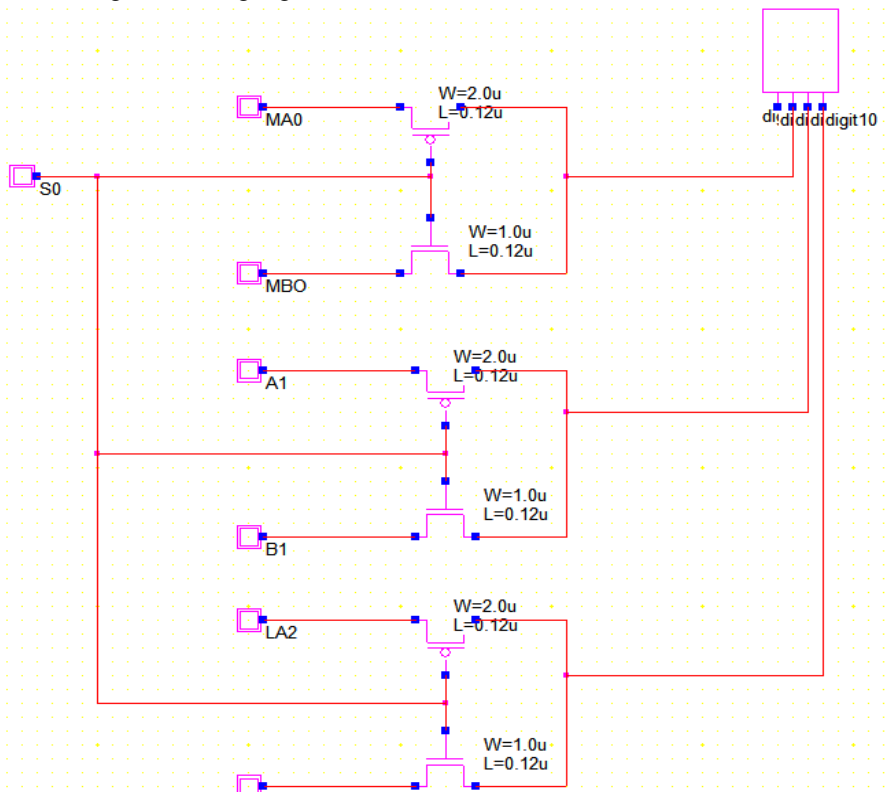


**Fig 6:** Integration of basic median filter

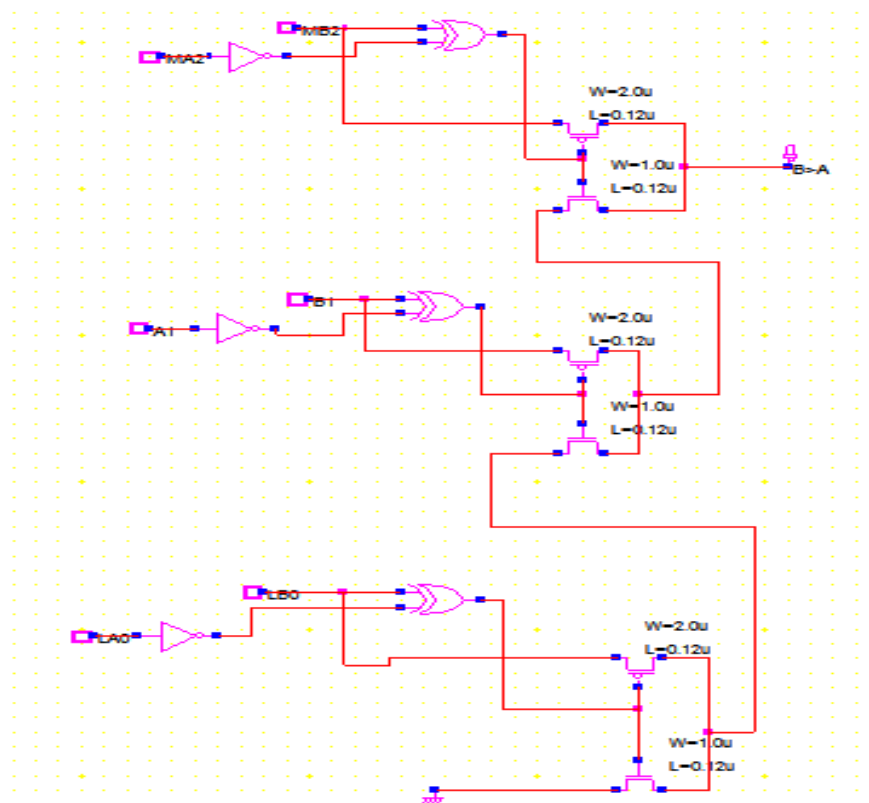
**2.2 Median Filter using Hybrid Full Adder**

Then another design of low power median filter using hybrid full adder is shown in figure 9 using figure 7 and

figure 8. Here the hybrid full adder design is incorporated in the comparator block which is shown in figure 8



**Fig 7:** Multiplexer design



**Fig 8:** Comparator using hybrid full adder design

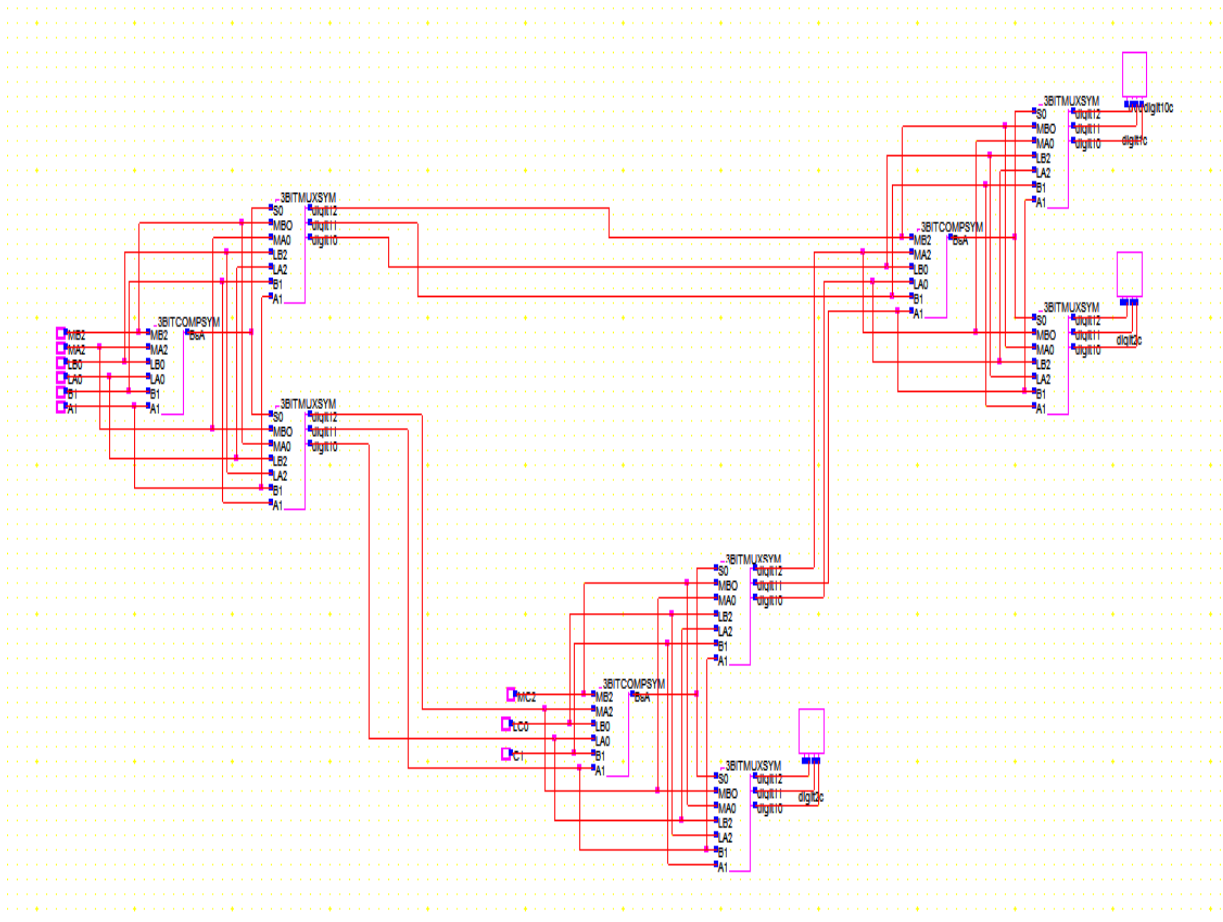


Fig 9: Low Power median filter

The circuit of the median filter using hybrid full adder integrated using cadence virtuoso platform 0.18nm technology is shown in figure 10

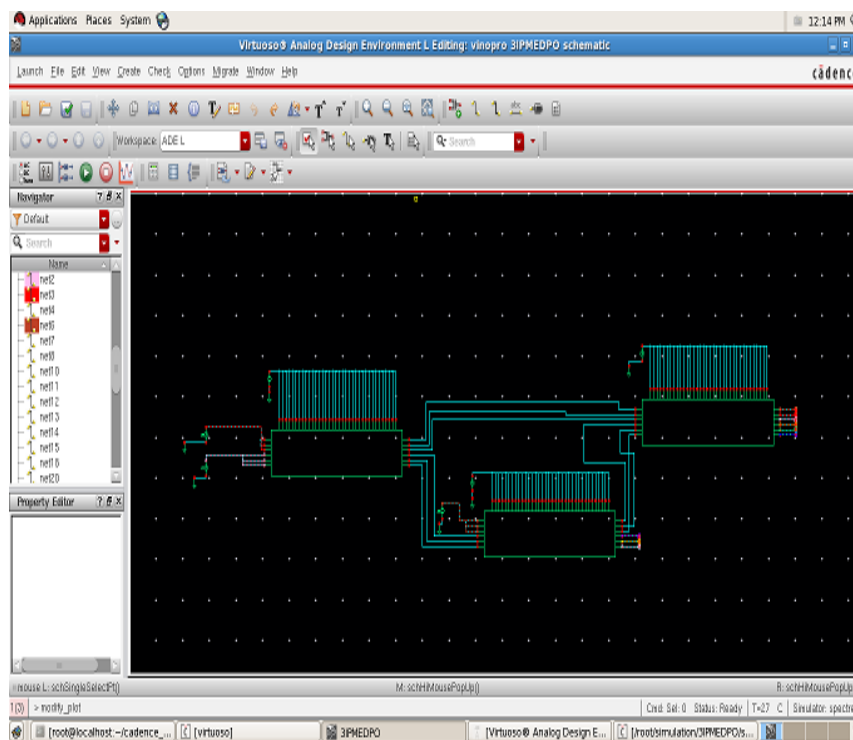


Fig 10: Integration of median filter using hybrid full adder

### 2.3 Median Filter using 6T Full Adder

The median filter design using the hybrid full adder consumes less power compared to the basic median filter. But it doesn't show much variation in power consumption, only slight variation is observed. So, that the median filter is designed using the 6T full adder design. The 6T full adder design is shown in figure 11, which is incorporated in comparator design shown in figure 12.

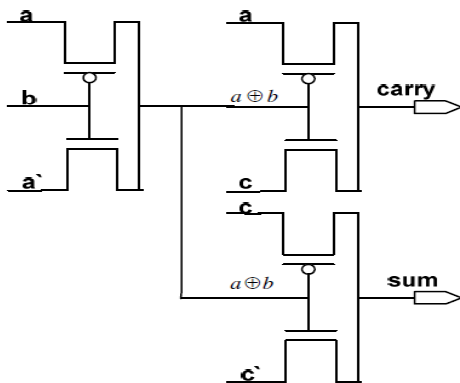


Fig 11: 6T full adder

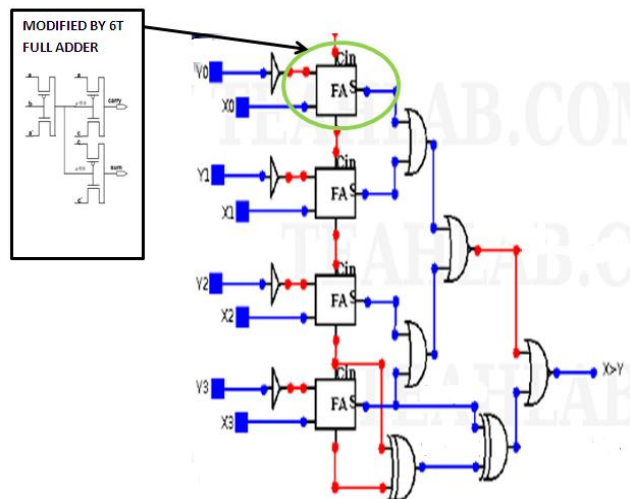


Fig 12: Comparator using 6T full adder design

The circuit of the median filter using 6T full adder integrated using cadence virtuoso platform 0.18nm technology is shown in figure 13

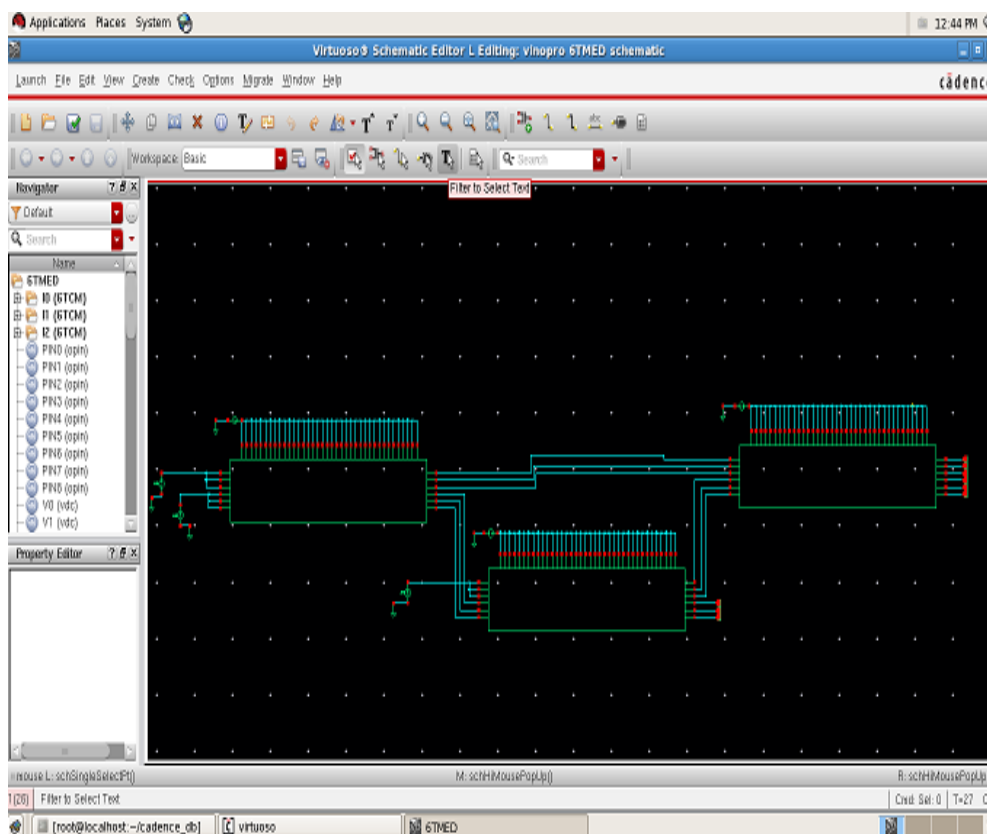


Fig 13: Integration of median filter using 6T full adder

### 3. RESULT ANALYSIS

Here the analysis and the comparison of the median filter using various styles of full adder is shown in table -1 based on the simulated waveform and power calculation obtained from the cadence software 0.18nm technology.

Table- 1 Comparison of median filters of various style

S no	Median filter design	Power (w)
1.	Basic median filter	5.959m

2.	Median filter using hybrid full adder	5.634m
3.	Median filter using 6T full adder	1.176m

The power calculation is done in the following steps. As to obtain the power, first the transient analysis of the median filter of various styles are obtained. From the waveform of the transient analysis the power calculation is done using the cadence software 0.18nm technology.

The analysis are shown in graphical form by means of chart as follows

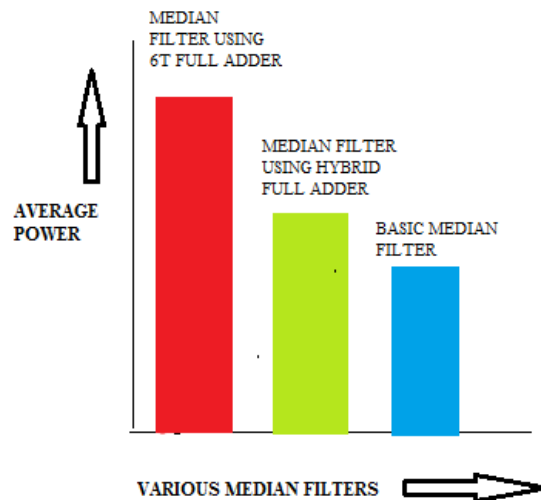


Chart – 1 Power analysis of the median filter of various style

#### 4. CONCLUSION

This paper discuss about analysis of various styles of median filter designed using hybrid full adder and 6T full adder. Here the average power consumption of various styles of filters are calculated using cadence virtuoso platform. From the power calculation it is observed that median filter designed using 6T full adder consumes less power compared to other median filters without much output degradation.

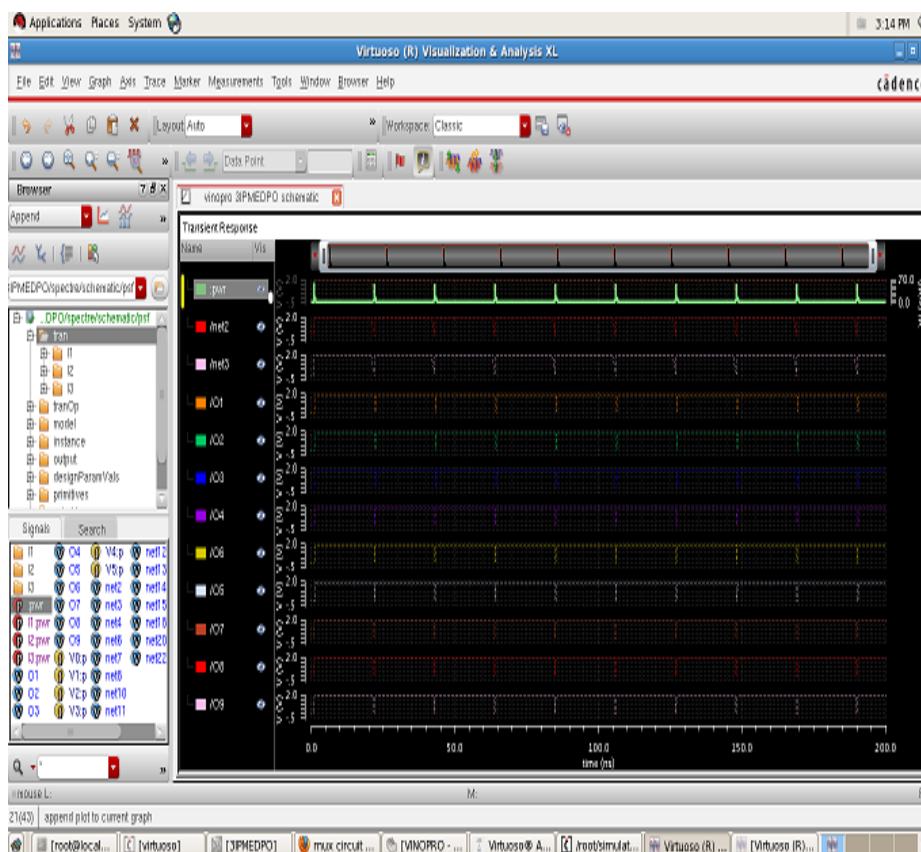


Fig 14: Simulated waveform of basic median filter



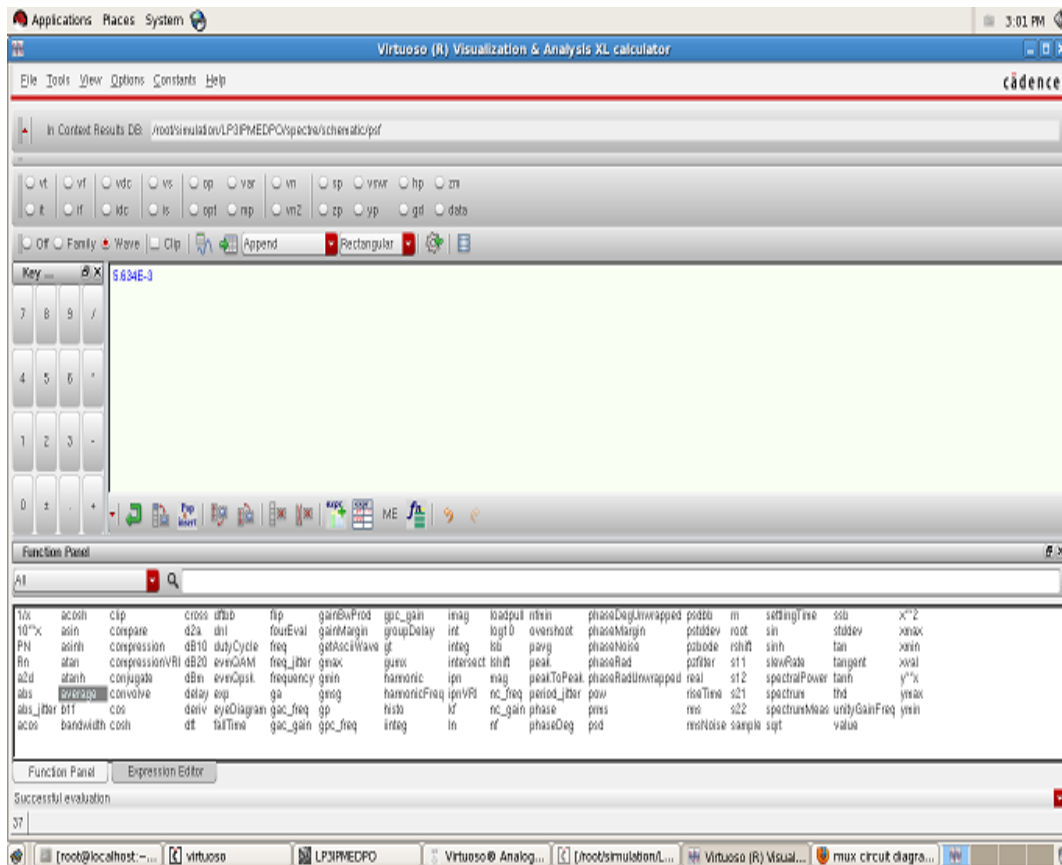


Fig 17: Power calculation of median filter using hybrid full adder

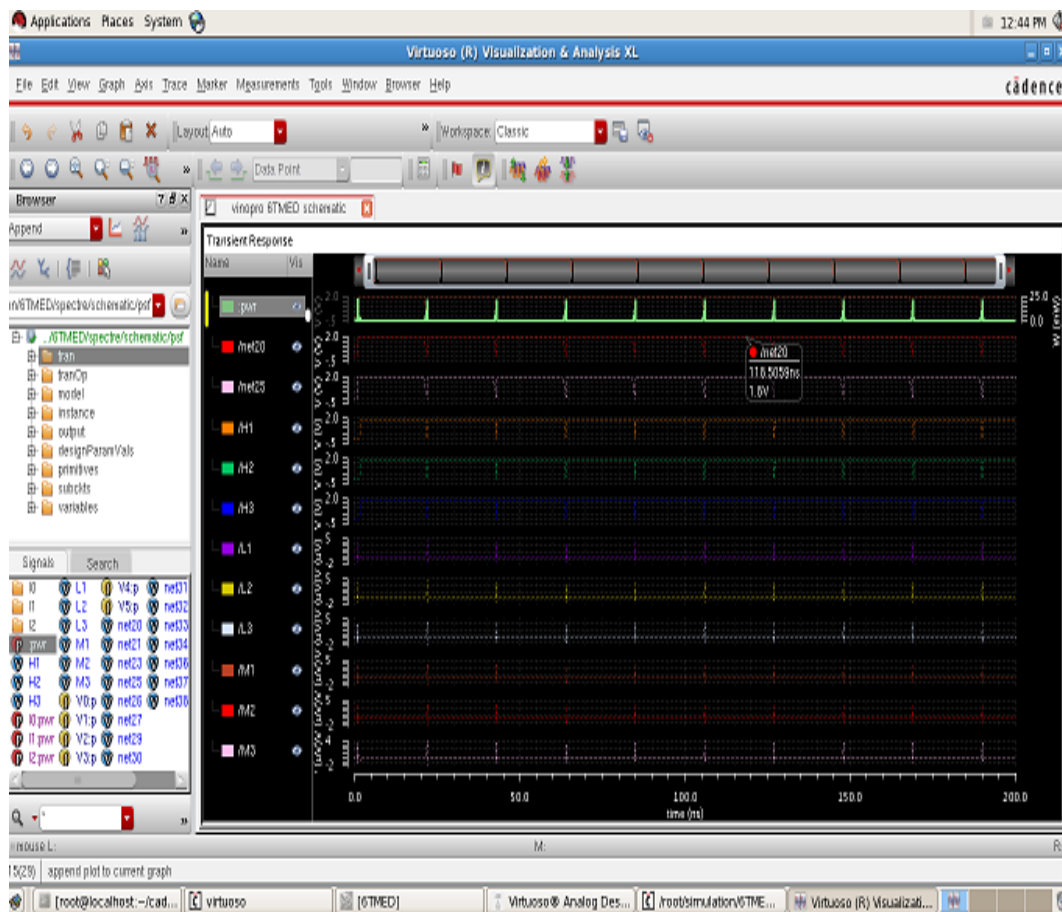


Fig 18: Simulated waveform of median filter using 6T full adder

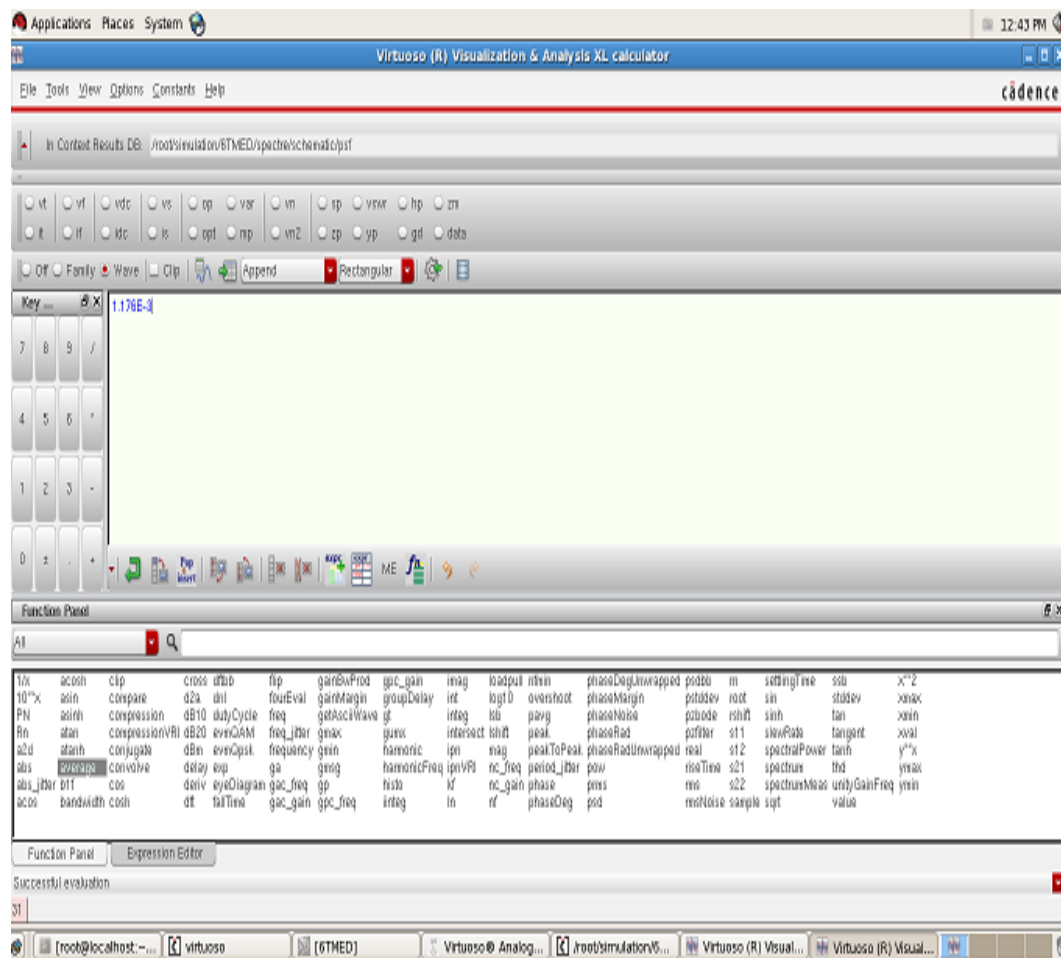


Fig 19: Power calculation of median filter using 6T full adder

## FUTURE ENHANCEMENT

The median filter design using 6T full adder will be implemented in MATLAB software in future for testing of noise reduction in the images.

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