VLSI IMPLEMENTATION OF A PROGRAMMABLE LOW DROP-OUT VOLTAGE REGULATOR

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Abstract

LDO voltage regulators compose a small subset of the power supply arena. Low-drop-out (LDO) voltage regulators are used in analog applications that generally require low noise and high accuracy power rails. Voltage regulators provide a constant voltage supply rail under certain loading conditions. Circuits that are not performing tasks are temporarily turned off lowering the overall power consumption. The LDO voltage regulator, therefore, must respond quickly to system demands and power up connected circuits. To motivate new aspect of power management towards a design of a low drop-out voltage regulator that fulfils the present industry requirements as well as the upcoming demands of the future, it becomes necessary to design the LDO regulator which gives overall performance. A low-voltage low-dropout regulator that uses an Vdd of 1 V to an output of 0.8–0.74 V, with 32-nm CMOS technology is proposed. By scaling down the technology, we can get lower power consumption. More emphasis is given on the compactness and low drop-out voltage. The latest power management unit concept inside the system on chip (Soc) scheme inspires the digital control potential for the design of a novel LDO regulator. A simple operational transconductance amplifier is used as the error amplifier (EA), with a current splitting technique which is able to boost the gain. In the rail-to-rail output stage of the EA, a power noise cancellation mechanism is adopted. Programmability is added by applying two external control signals. These advantages allow the proposed LDO regulator to achieve a 60-mV output variation for low load transient, area efficient architecture with low power consumption.

Keywords: *low drop-out,32nm,low power consumption, programmability*

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1. INTRODUCTION

The usage of the battery power devices in today's global village has become pervasive and indispensable in almost every walk of life. By reducing the number of battery cells, cost and size of design get reduced. This may minimize quiescent current flow and in turn battery life increases. An increasing number of low voltage applications require the use of LDOs, which include the growing family of portable battery products. Voltage regulators provide a constant voltage supply rail under all loading conditions. Most hand-held, battery-powered electronics equipment feature power-saving techniques to reduce power consumption. Low drop-out and low supply current characteristics of CMOS linear regulators found more advantageous in the world of electronics .LDO regulators enable battery to be used up to the certain limit, and therefore the regulators are now essential power management ICs for the devices like mobile phones, digital cameras, and laptop PCs to have long battery life. There has been an increasing demand to design a stable LDO for a wide range of load conditions with high PSR(power supply rejection),low drop-out voltage and low quiescent current. But it is found to be difficult to improve all of them simultaneously. With the advent of low power battery-operated circuits, demanding special emphasis is on compactness and portability. The use of smaller transistor size enables faster transient response since slew-rate limit at the gate of the power transistor is relatively not serious [4].So it has become imperative to optimize existing low drop-out regulator structures for greater all-round performance. The power management unit (PMU) concept inspires researchers to focus on minimum supply voltage, faster dynamic response, higher stability, small area and less power consumption. Previously proposed architectures provides different techniques to isolate input and output along the high current signal path. It is seen that nm technology proves better in achieving required performance specifications. We can make use of digital control to fulfill demands for multifunction among consumer electronics, functional circuits which are integrated as system on chip(Soc). In [5]–[7], external control signals open or short the switch transistors to change the feedback resistor divider ratio to achieve a programmable output voltage required by different applications.

A basic LDO regulator is composed of three main components-biasing circuit, an error amplifier, a power MOS device. The design of the output stage of the error amplifier has impact on the required size of power transistor that improves load regulation especially when the supply

voltage is low. This paper presents an LDO regulator using a simple OTA-type error amplifier and adaptive transient accelerator which can achieve operation below 1V with fast transient response, high PSR under a wide range of operating conditions. Main focus is to design a programmable low-dropout (LDO) voltage regulator that can operate with a very small input output differential voltage with 32nm CMOS technology whose output voltage level is controlled externally by means of control signals. Proposed design is a complete SOC(system on chip) design which provides many circuit applications in portable, industrial and medical sectors. As future nm technology offers more advantages in achieving most of the performance specifications so it is beneficial to propose the regulator with the selection of lower order of nm technology to fulfill targeted demands.

2. DESIGN CONCEPTS OF LOW VOLTAGE LDO REGULATOR

2.1 Low Supply (Input) Voltage and Low IQ

A high loop gain is necessary in LDO regulator design to achieve optimum performance values such as accurate output (line/load regulation) and PSR(power supply rejection).A low supply voltage and output-resistance reduction induced by a shrinking technology limit the achievable gain of the EA[1]. A power transistor with a significant size is required for a specific load current when an LDO regulator sinks current from a low voltage power source. Thus, the EA(error amplifier) requires a higher current slew rate to drive the power transistor., an EA with not more than three stacked transistors between the supply voltage and ground is preferred; each of the transistors, therefore, has more voltage space to stay in the saturation region to achieve low-voltage operation.

2.2 Fast Transient Response

The transient response includes the voltage variation (spike) and recovery (settling) time during the load current transient. The voltage variation is more important than the recovery time, as even a small output-voltage variation can cause severe performance degradation to the load circuit operating at an ultralow supply voltage (e.g., 0.5 V). To reduce the output-voltage variation, both a large closed-loop bandwidth of the LDO regulator and a large output current slew rate of the EA are required [1]. When closed loop bandwidth increases, it may affect the pole/zero locations and the circuitry may become too complex which consumes more *IQ* (quiescent current) .The concept of the Transient accelerator may adopted to conditionally provide extra charging/discharging current paths to get better transient response.

2.3 Power Supply Rejection

Noise suppression is a important factor to provide a clean and accurate output voltage with a low voltage level (≤1 V).An *n*-type power MOS transistor or a cascoded power MOS transistor structure can achieve a high PSR; however, they are unfeasible for sub 1-V operations. As an LDO regulator adopts a *p*-type power MOS transistor, either a high loop gain or good noise cancellation can achieve a high PSR. It is, however, difficult to achieve a high loop gain with a low supply voltage. In addition, the circuit for the power noise cancellation mechanism increases the design complexity and consumes extra *IQ* [2]. The concept of resources sharing power noise cancellation mechanism can be proposed to get good power supply rejection[1].

3. SCHEMATIC OF PROGRAMMABLE LOW DROP-OUT VOLTAGE REGULATOR

A voltage reference is used with the op-amp to generate a regulated voltage; it provides a constant output voltage which will be compared with the output voltage from the feedback network. If the voltage reference is stable with temperature, the fact that the Vreg is a function of a ratio of resistors and the variation in the op-amp's open loop gain is desensitized using feedback makes the regulated voltage stable with process and changes in temperature. Error amplifier produces an error signal whenever the fed back sensed output differs from the reference voltage. Pass Element provides the output current needed to drive any load. Generally pass element used is PMOS pass transistor. This device must be very wide so that it can source large load currents with a reasonable gate-source voltage. The length remains at the minimum value to keep the threshold voltage low. The output voltage of the LDO is at the drain of PMOS pass transistor, and resistors R1 and R2 form a voltage divider to feed a fraction of the output voltage back to the input. R1 and R2 are made large so that very little current flows through them, minimizing the power consumption of the feedback path. The loop gain depends on the products of the voltage gains of the two main gain stages in system architecture. The high loop gain provides good line and load regulations. In proposed architecture, a current-sourcing PMOS in the output stage is added. It is required that the PMOS be pulled to ground so as to be biased into saturation region. Because of this, the existing topology is modified and a Common- Source Stage is added, with the amplifying device. This amplifying device used is large enough so as it is to be used as a strong pull down device. The Common-Source stage is responsible to enhance signal swing and boost the gain at the op-amp output, subsequently. The Common-Source stage also useful to pull the gate of the large PMOS low enough so that its gate-to-source voltage increases. If the feedback voltage is smaller than the reference voltage, the gate of the PMOS device is pulled to lower, so that more current is allowed to pass and increases the output voltage. If the feedback voltage is greater than the reference voltage, the gate of the PMOS device is pulled to higher, so that less current is allowed to pass and decreases the output voltage. Programmability is added to the LDO by using two external control signals, ctrl1and ctrl2 which are applied at the gate inputs of two NMOS devices. The binary input brings that resistance into the circuit and controls the output voltage by biasing the transistor in saturation. The proposed architecture consists of the following stages:

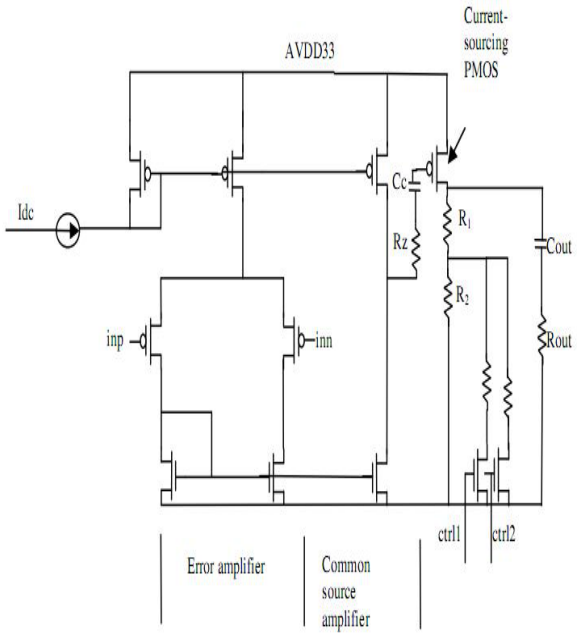

Fig-1: Schematic of programmable LDO regulator

3.1 Error Amplifier

A high gain operational amplifier is used as the error amplifiers [11], with a stable voltage reference fed to one of its inputs while other to the ground. The voltage reference is generally derived from a band gap reference circuit. The differential pair of the operational amplifier is used which consists of a current mirror NMOS load and a PMOS tail current source, along with the gate-drain connected load being driven by an ideal current source Idc. A current mirror NMOS load is responsible to provide high output impedance and high gain. An operational amplifier connected with this sort of load is termed as an open-transconductance amplifier, where all nodes are low impedance nodes with the exception of the differential pair [12].The resistive feedback network balances the amplifier by minimizing op-amp offset. The design of the output stage of the error amplifier has a substantial impact on the required size of the power transistor for the improvement of load regulation, especially when the supply voltage of the VLSI systems is low [4].

3.2 Common-Source Amplifier

In general, a source follower is used as the buffer stage in most LDO's. The source follower is a simple implementation of the buffer which uses natural NMOS transistor and it has asymmetric current driving capability and limited gain. Hence a common-source amplifier is used. It has a small signal gain given by-

$$Av=gm\ (Ro1 \| Ro2)$$

Here, gm is the transconductance of the amplifying device; Ro1 and Ro2 are the output resistances of the load and the amplifying device. When the amplifying device (NMOS) is made large enough, then we can get improved gain at the second stage. NMOS also acts as a strong pull down device, yielding rail-to-rail swing. Operational amplifiers with rail-to-rail output stage achieve the maximum output signal swing in systems with low single-supply voltages. They are capable of generating an output signal up to the supply rails.

3.3 Current-Sourcing PMOS

In our design, a PMOS with high voltage threshold has been used. If a lower voltage threshold PMOS is used, then we can get advantage of lesser area but low-voltage threshold FETs are known to contribute to leakage currents, increasing power dissipation in the device. Therefore current-sourcing PMOS is used which is responsible for quick charging and discharging of the output node, capable of increasing slew rate to obtain faster settling times.

4. CMOS LAYOUT OF PROGRAMMABLE LDO REGULATOR

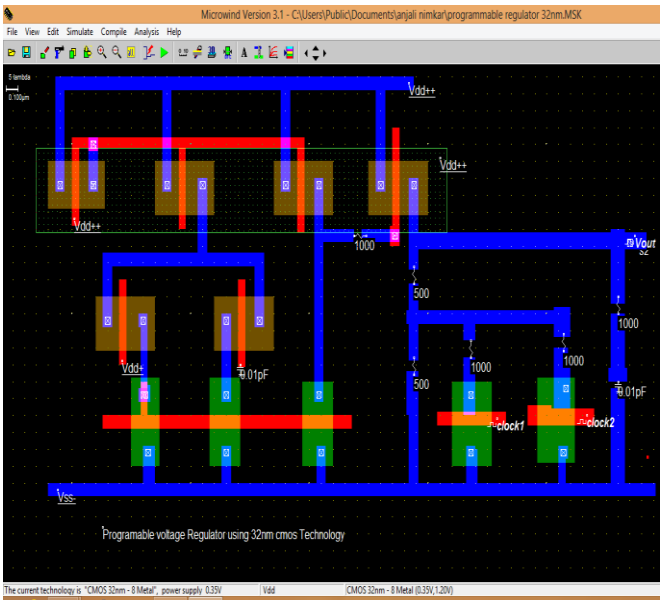

Fig-2: CMOS Layout of Programmable Low Drop-out Voltage Regulator

The proposed LDO is designed using 32 nm CMOS/VLSI technology in MICROWIND 3.1. The effective gate length required for this technology is 28nm. The main novelties related to the 32nm technology are high-k gate oxide, metal gate, 3rd generation high-k channel strain and very low-k interconnect dielectric. These key features of 32 nm technologies are provided from various providers like TSMC, Fujitsu, Intel, etc. Figure 2 shows CMOS layout of programmable low drop-out voltage regulator and figure 5 shows CMOS layout of programmable LDO regulator The MICROWIND3.1 program allows designing and simulating an integrated circuit at physical description level. The package consists of library of common logic and analog ICs to view and simulate. Also this program includes all the commands for a mask editor as well as original tools never gathered before in a single module (2D and 3D process view, VERILOG compiler, tutorial on MOS devices). Every step of design follows the design flow of MICROWIND 3.1 software. The design methodology will be according to VLSI backend design flow. The main objective is to design

and analysis of the low drop-out regulator. We can gain access to circuit simulation by pressing one single key. The electric extraction of circuit is automatically performed and the analog simulator produces voltage and current curves immediately. Table-1shows MOS device design parameters.

Table -1: MOS device design Parameters

MOS	W(µm)	L(µm)	W(Lambda)	L(Lambda)	Type	Current drawn by MOS(mA)
N1	0.320	0.100	16	5	Standard	0.156
N2	0.340	0.080	17	4	Standard	0.201
N3	0.260	0.080	13	4	Standard	0.000
N4	0.260	0.080	13	4	Standard	0.000
N5	0.240	0.080	12	4	Standard	0.000
P1	0.320	0.060	16	3	Standard	0.036
P2	0.320	0.060	16	3	Standard	0.000
P3	0.320	0.060	16	3	Standard	0.000
P4	0.320	0.060	16	3	Standard	0.000
P5	0.320	0.060	16	3	Standard	0.000
P6	0.280	0.060	14	3	Standard	0.000

5. RESULTS AND DISCUSSION

Here for the design, microwind3.1 VLSI Backend software is used. This software allows designing and simulating an integrated circuit at physical description level. The proposed LDO is designed using 32 nm CMOS/VLSI technology in microwind3.1software, which in turn offers high speed performance at low power. This layout design is implemented using 5 NMOS along with 6 PMOS BSIM4 transistors with optimum dimensions of transistors and metal connections which follow the lambda based rules of microwind 3.1 software. The power dissipation in CMOS digital integrated circuits is a strong function of the power supply voltage. Therefore, reduction of VDD emerges as a very effective means of limiting the power consumption. For the proposed LDO, power supply VDD of 1 volt is used.

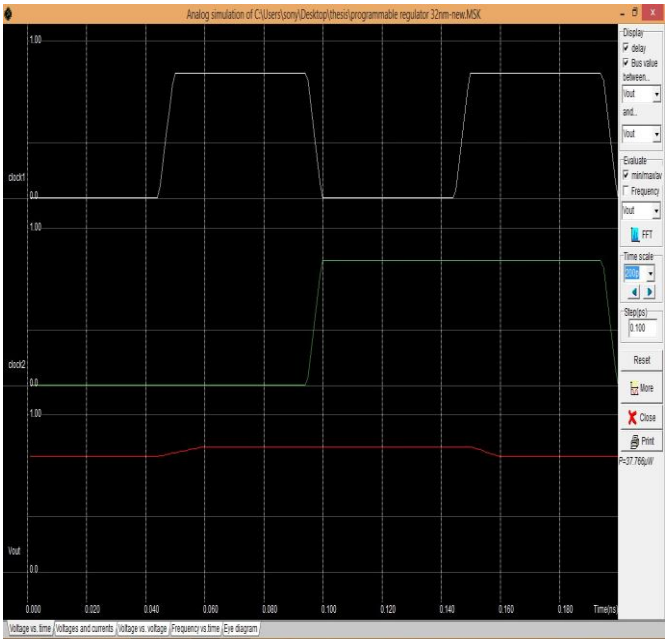

Fig- 3: Regulated output of Programmable LDO Regulator

Fig-3 shows transient waveforms of programmable LDO regulator. It is seen in programmable LDO, that when we apply two external control signals at the gate inputs of two NMOS transistors; the binary input that appears at the gate is responsible for bringing regulation into the circuit and we get regulated programmable voltage for different levels as given in table 2.This programmability allows two different output voltages for four control inputs with output to output dropout voltage of only 60 mV and input to output dropout voltage of 200mV. Power consumption is very low as it consumes 15.446µw of power. More than one application can make use of programmability, requiring output voltage at 0.74V and 0.80V.

Table 2: Range of output voltages

Binary input	Output voltage
00	0.74
01	0.80
10	0.80
11	0.74

The width of programmable LDO is 5.7µm & its height is 2.7µm.Thus the surface area of proposed Programmable LDO is 15.2µm^2.The electrical nodes used are 20.So We have used minimum resources to get optimum results.

From MOS characteristics of transistors, it is seen that the normal operating region of transistor is saturation region when used as an amplifier and operates as a constant current device as Id is relatively independent of Vds. It is due to fact that as Vds increases, channel resistance also increases proportionally thereby keeping Id constant. Hence the current depends only on Vgs and not on Vds and channel becomes completely pinched off near the drain, so the value of capacitance Cgd and Cgs approaches to zero. The MOS transistor is a symmetric device. This means that the drain

and source terminals are interchangeable. For conducting NMOS transistor, Vds>0V;For the PMOS transistor, Vds<0V.

The tabulated results clearly indicate that LDO results in lesser resource utilization with minimum dropout, lower quiescent current at lower load conditions. The system gain is high; it indicates the stability of the system is good.

6. COMPARATIVE RESULTS

Table 3: Comparison of proposed model with different published paper

parameters	[6]	[5]	[4]	[3]	[2]	[1]	This work
Technology	0.13 um	0.35um	0.35um	65 nm	0.18um	90nm	32nm
Vdd (V)	1	2.8	1.5-4.5	1.2	1.8-0.9	1	1
Load capacitance	-	Capacitorless	-	10 pF	1uF	1 uF	0.01 pF
Drop-out voltage	0.15 V	200mV	200mV	200mV	0.1 V	500 mV	200 mV
No. of NMOS and PMOS	More than 15	11	-	5,6	-	More than 15	5,6
Area	0.049mm^2	0.29mm^2	371umx270um	-	0.81mm^2	0.041mm	15.2 mm^2
Power Consumption	-	-	High	100um	-	moderate	15.446uW

Referring table 3, It is seen that our programmable LDO yields better power consumption of 15.446µW than [3],[4]and[1].Our design has a lower dropout voltage than that of IEEE 2014 results. Their design extends a good PSRR to much higher frequencies without an external capacitor, but it is not reported how much current their design used to do it. Also, it is likely that their design took up more area than ours [1].

The LDO designed in [4] and [5] had a same dropout voltage than our design, and a comparable current consumption. Since some of the LDO's supply voltage was higher, so their power consumption was higher.

In our design we have used the capacitor value of 0.01Pf & the power consumption of our proposed model is 15.446µW which is very less as compared to the results mentioned in [3]. LDO in [3] used the external capacitor of 10µF which is quite large than ours. As compared to IEEE 2010 results the surface area used is more compared to our proposed model and their power consumption is high as their supply voltage is greater.

7. CONCLUSION

From the continuous study it is observed that foundry of technology and supply voltage range is continuously decreases with the advancement of technology. By scaling down the technology, we can get lower power consumption. We have designed a low power low drop-out regulator that is capable of delivering different output voltages, depending on the control signals. Hence we able to design an area efficient programmable low drop-out voltage regulator with very less power consumption and open a door to save battery life of product.

Also the optimum, high efficient chip design of programmable low power LDO with four output using 32nm VLSI technology give different voltage ranges for different applications. Multiple applications can make use of programmability. The better gain can be achieved by further increase in transconductance of the differential pair. Also by reducing the number of stages and using cascade topology with resistive biasing can generate greater gain. In this architecture, the external capacitor used is of 0.01pF, but capacitorless architectures [4] have been proposed and form a significant part of current CMOS LDO design literature. The current design hence has scope of improvement in this direction. The large external capacitor used in typical LDOs can be removed allowing for greater power system integration for system-on-chip (SoC) applications that require a sound compensation scheme for both the transient response and the alternating current (ac) stability. Furthermore, the designing can be possible with digital implementation and programmability can be added to become suitable for more applications considering the advancement of future technology.

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