SATELLITE TELECOMMAND MODEM

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Abstract

With the increasing interest in nano, micro and small satellites, need arises for miniaturization of satellite systems for small size, low weight, low cost designs and short development periods. For the operation and maintenance of a satellite in the designated orbit, a reliable commanding system is mandatory. This paper presents the work carried out in designing and developing a telecommand modem for use with student satellites. To transmit low bit rate command data, PSK/PM a two level modulation scheme is adopted. The architecture and the simulation and test results of the hardware realized on an FPGA are provided.

Keywords *–Phase Shift Keying, Phase Modulation, PSK/PM Modem, bit error rate, satellite commanding.*

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1. INTRODUCTION

Miniaturizing technology has created vast interest towards small satellites. Unlike conventional large satellites, small satellites have smaller size, lower weight, cheaper designs, and shorter development period, which made it possible for universities to develop nano and micro student satellites. Up-to-date technology can be incorporated into nano, micro and mini satellites without bothering for most expensive space proven designs which are essentially required for much larger, more expensive missions.

Student satellites are generally designed with commercial or industrial components and VLSI chips. Telecommand, being the one of the most critical subsystems of the satellite communication network, needs utmost care in design and realization process. The command sub system is simulated on Matlab simulink platform to optimize the performance and realized on an FPGA.

2. DESCRIPTION

Command data being very low is formatted and encoded at a bit rate of 100 bits per second. A carrier in the standard ITU allotted up link frequency band of 2015 to 2110 MHz is phase or frequency modulated with the command data for transmission. Since the data rate is low compared to the carrier, the sidebands will be close to carrier and the receiver cannot detect the data as C/N will be too low due to phase noise of the high frequency carrier. To overcome the phase noise limitation, a two level modulation PSK/PM[6] is used for modulating the command data on an IF carrier which is further up-converted to the operating frequency band and amplified for transmitting to satellite from a satellite control station. The onboard satellite communication system receives the signal, down converts to an IF frequency and the two level PM/PSK demodulation carried out for extracting the command data. This paper presents the architecture that is implemented on an FPGA along with simulation and test results.

3. MODEM ARCHITECTURE

The satellite telecommand modem consists of a modulator at ground station and demodulator at the on-board satellite along with clock recovery circuit. The ground station computer formats and encodes the command data. a low frequency carrier of 10 KHz is BPSK modulated with the command data. The BPSK modulated carrier in turn phase modulates the IF carrier. The PM carrier is up converted, amplified and transmitted to satellite. The onboard command receiver receives the PM carrier, down converts, phase demodulates. The demodulated PSK carrier is PSK demodulated to extract the data. The clock is generated from the data for further processing the recovered data. The RF up conversion and the down-conversion modules are generally external and not addressed in this paper. The block diagram is as shown in Fig.1.

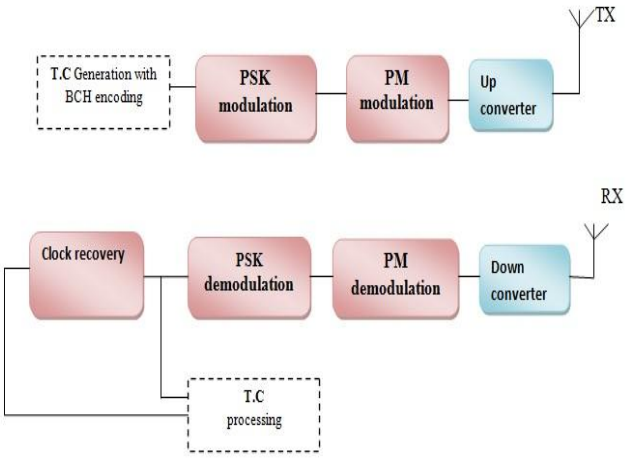


Fig.1 MODEM blocks

4. CIRCUIT DESIGN & IMPLEMENTATION

For the designed modem, the specifications used is as shown in below table 1,

Table.1 Specifications

Type	Frequency
Data rate	100bps
Subcarrier sine wave	1kHz
Carrier wave	16kHz

After optimizing the performance on Matlab Simulink platform, implemented in Xilinx system generator for data rate of 100bps.The implementation module is shown in Fig.2

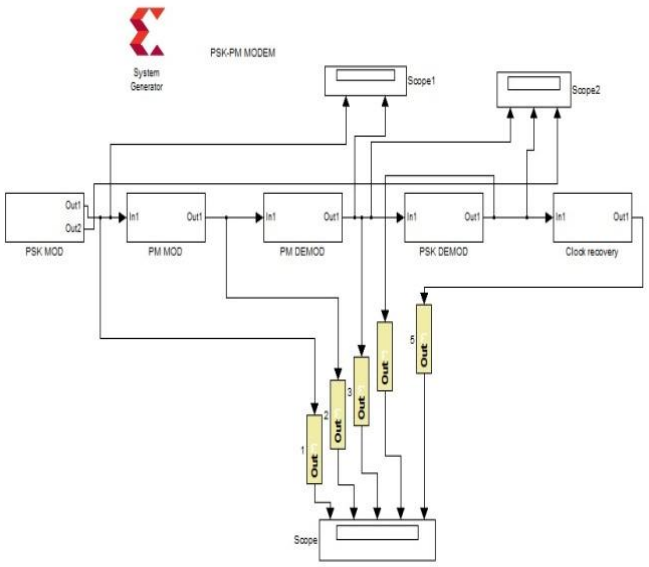


Fig.2 Sysgen MODEM module

The proposed modem consists of five sub-modules:

a) PSK modulation
b) PM modulation
c) PM demodulation
d) PSK demodulation
e) Clock recovery

4.1 PSK Modulation

The random data generated is converted to bipolar signal and it is fed as one of the input to the PSK modulator and the other input to the modulator is the sine wave, which is the carrier for the PSK modulation is as shown in the below Fig.3.

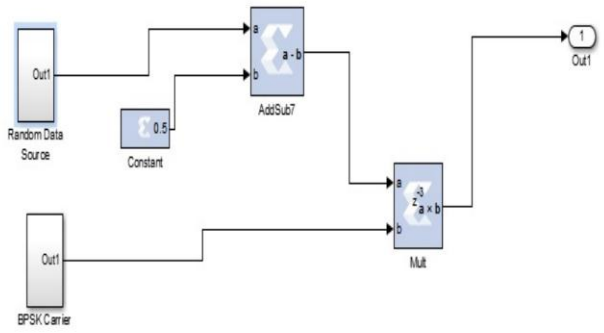


Fig.3 PSK modulator

4.2 PM Modulation

PSK modulated wave is differentiated and is given one of the input to the NCO and the other input to the NCO is carrier which is 16 kHz, the PM modulator is as shown below in Fig.4.

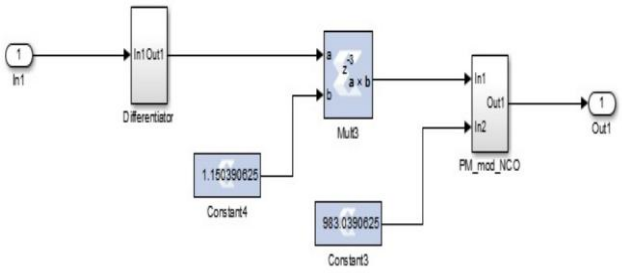


Fig.4 PM modulator

4.3 PM Demodulation

The PM demodulator is implemented with the help of simple PLL and with the loop filter as shown below in Fig.5 & the loop filter is designed as per the specification.

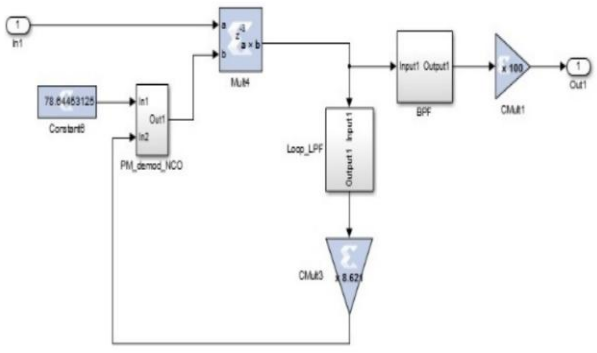


Fig.5 PM demodulator

4.4 PSK Demodulation

The PSK demodulation is done using COSTAS loop and is as shown in Fig.6, this Costas loop performs both carrier reconstruction and data detection within the loop. The upper loop is referred to as quadrature loop and functions as a typical PLL, the lower loop is referred to as in-phase loop, provides data extraction. The corrected error signal is applied through the loop filter to the NCO, which gives the phase estimation.

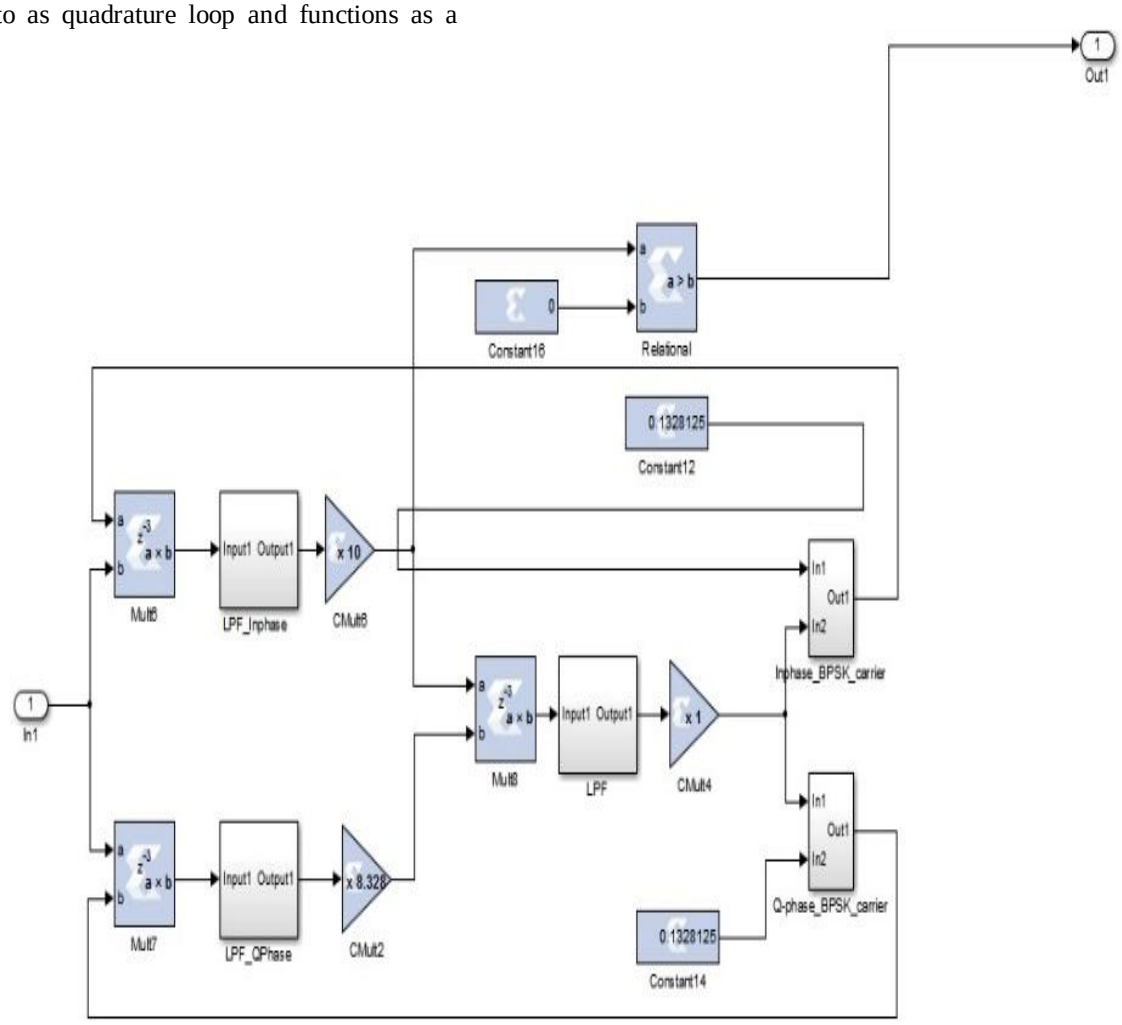


Fig.6 PSK demodulator

4.5 Clock Recovery

The clock is generated from the PSK demodulated wave and this clock recovery circuit contains filter and simple PLL, this generated clock is synchronized with system clock and the schematic for the clock recovery circuit is as shown below in figure 7.

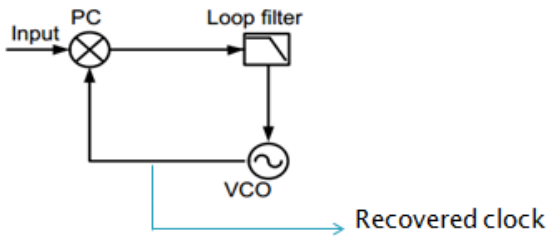


Fig.7. Clock recovery

5. SYSTEM GENERATOR SIMULATION RESULTS

5.1 PSK Modulation

The generated random input data at 100bps and the subcarrier of 1kHz sine wave is PSK modulated[2] in the system generator, here at the transition of the input data the phase of the carrier wave is changed and is as shown in the below simulation result in Fig.8.

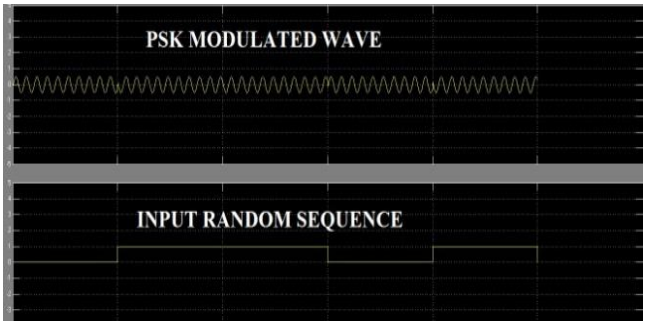


Fig.8 PSK modulated waveform

5.2 PM Modulation

The input to the PM modulator is the differentiated PSK modulated wave and the other input to the PM modulator is the carrier wave[3], here the carrier wave is taken as 16kHz and the simulation result for the PM modulation is as shown in the below Fig.9.

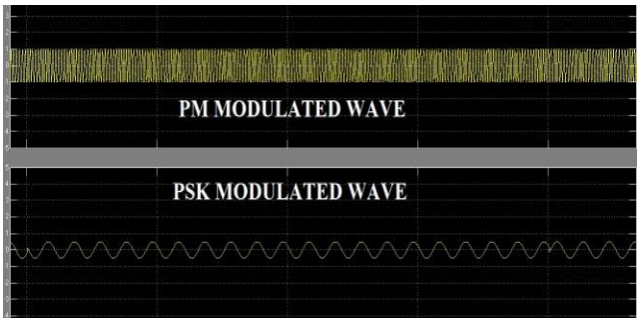


Fig.9. PM modulated waveform

5.3 PM Demodulation

The PM demodulator consists of PLL, where the reference frequency for the PLL[5] is carrier used at the PM modulator and the filtered output of the phase detector gives the PM demodulated output. The simulation result of the PM demodulator shown in Fig.10, depicts that both PSK modulated wave and the PM demodulated wave matches exactly at the transition.

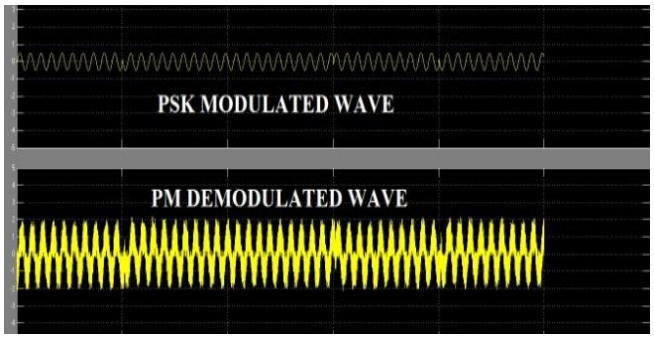


Fig.10. PM demodulated waveform

5.4 PSK Demodulation

The PM demodulated wave is split it into In-phase and quadrature phase component as shown in the PSK demodulator fig.,11, the simulation result for the PSK demodulator is shown in Fig.10., depicts that the demodulated data and the input random data matches the same but it contains some phase reversal due to the communication channel, in order to overcome that problem differential decoding is done after demodulation, which is not addressed in this paper.

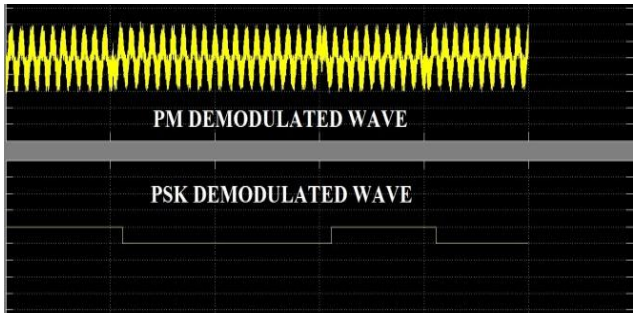


Fig.11. PSK demodulated wave

5.5 Clock Recovery

From the PSK demodulated data the clock is generated, which should synchronize with the system clock[2] if the demodulated data matches the baseband data, the simulation results shows that the clock generated matches the system clock and is shown in below Fig.12.

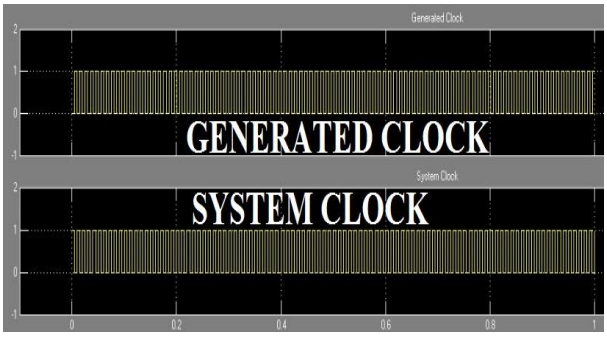


Fig.12. Generated clock

6. SYNTHESIS & FPGA RESULTS

The design summary for the designed modem is as shown below in figure 13.

Top_module Project Status			
Project File:	psk_pm1_cw.xise	Parser Errors:	No Errors
Module Name:	Top_module	Implementation State:	Programming File Generated
Target Device:	xc5vlx110t-1ff1136	• Errors:	No Errors
Product Version:	ISE 12.4	• Warnings:	999 Warnings (244 new)
Design Goal:	Balanced	• Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	All Constraints Met
Environment:	System Settings	• Final Timing Score:	0 (Timing Report)

Device Utilization Summary				
Slice Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Registers	1,650	69,120	2%	
Number used as Flip Flops	1,628			
Number used as Latch-thrus	22			
Number of Slice LUTs	18,200	69,120	26%	
Number used as logic	17,753	69,120	25%	
Number using O6 output only	16,767			
Number using O5 output only	861			
Number using O5 and O6	125			
Number used as Memory	300	17,920	1%	
Number used as Shift Register	300			

Fig.13. Design summary

Overall RTL schematic is taken from the VHDL code and is shown is below in the figure 14.

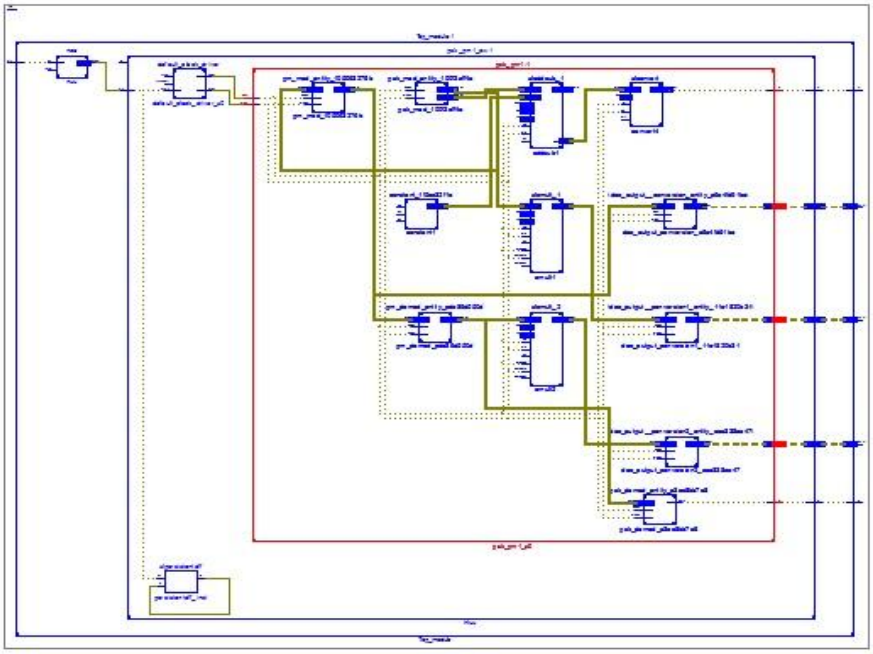
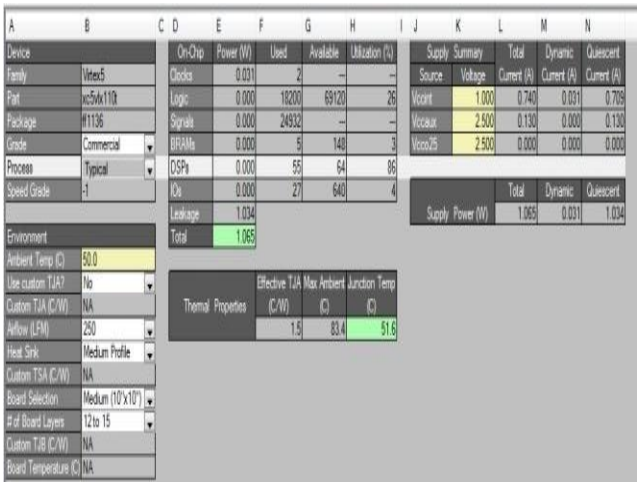


Fig.14. Overall RTL schematic

Power analysis is made for the designed modem through Xilinx tool and the report is as shown below in the figure 15.



Device	
Family	Virtex5
Part	xc5vlx110t
Package	ff1136
Grade	Commercial
Process	Typical
Speed Grade	-1
Environment	
Ambient Temp (C)	50.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250
Heat Sink	Medium Profile
Custom TSA (C/W)	NA
Board Selection	Medium (10"x10")
# of Board Layers	12 to 15
Custom TJB (C/W)	NA
Board Temperature (C)	NA

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.031	2	–	–
Logic	0.000	18200	69120	26
Signals	0.000	24932	–	–
BRAMs	0.000	5	148	3
DSPs	0.000	55	64	86
IOs	0.000	27	640	4
Leakage	1.034			
Total	1.065			

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.000	0.740	0.031	0.709
Vccaux	2.500	0.130	0.000	0.130
Vcco25	2.500	0.000	0.000	0.000

	Total	Dynamic	Quiescent
Supply Power (W)	1.065	0.031	1.034

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	1.5	83.4	51.6

Fig.15. Power analysis report

Designed modem is implemented in the Vertex 5 FPGA ML605 and the results for the same is as shown below in fig 16.

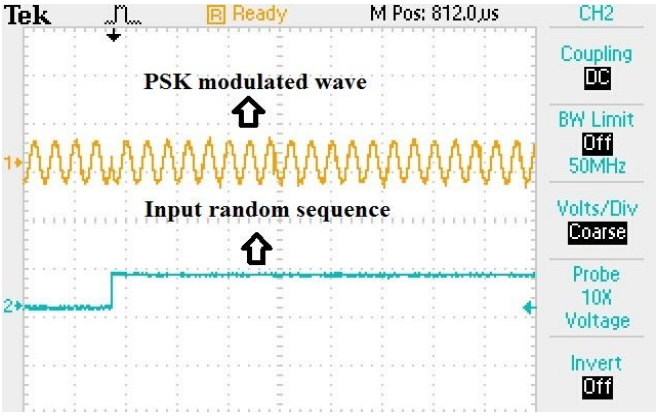


Fig.16. PSK modulated wave

Input random sequence with 100bps is recovered at the receiver is as shown in the figure below

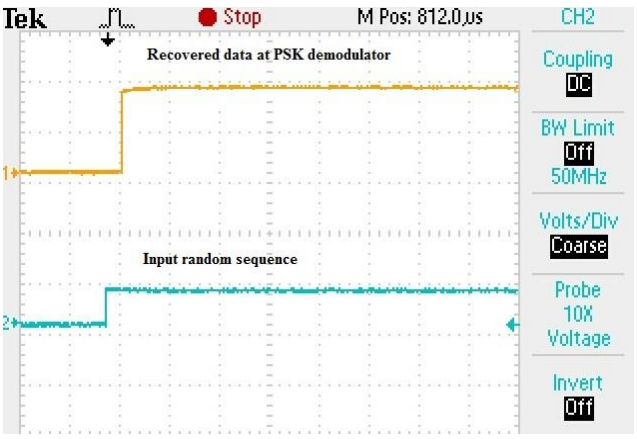


Fig.17. Recovered data at receiver

7. CONCLUSION

A two level modulation namely PSK/PM modulation is considered for transmitting the low bit rate command data on an S-band carrier in the frequency band allotted by ITU for satellite uplinks. A PSK/PM modulator and demodulator are designed, simulated with simulink tool of Matlab. After optimizing the performance a bit file is generated using Xilinx system generator and an FPGA is fused. The simulation results are presented.

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BIOGRAPHIES

Dr. V. Sambasiva Rao, Professor in ECE Department of PES University, Bangalore, is an engineering graduate (1973) from College of Engineering, Kakinada (Andhra University) and obtained PhD from BITS, Pilani in 2010. For over 37 years (April 1974 to June 2011), he was associated with ISRO in various capacities. He is a senior member of IEEE, Fellow of IETE and Member of IET and Astronautical Society of India. He received five distinguished awards and published 70 technical papers.

Mr. Shreyas M has obtained his Bachelor’s degree in Electronics & Communication at Visvesvaraya Technological University, Belgaum, and is currently Pursuing his Masters in VLSI and Embedded System Design at PES Institute of Technology, Bangalore. His fields of interest are VLSI and Communications.