CONTROLLER DESIGN FOR MULTICHANNEL NAND FLASH MEMORY FOR HIGHER EFFICIENCY IN SSD'S

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Abstract

Flash based storage system is presently very attractive in the market than the previous Magnetic disk drives. Flash memory is basically Non-Volatile memory; it means it can electrically erasable and programmable. The Flash memory has less power consumption and less latency compare to previous magnetic disk drives, this makes flash more attractive and popular. Flash memory basically comprises of three basic operations, they are Read, Write (program), and Erase. The Flash memory will be written in pages and will be erased in blocks. Functions of the multi-channel parallel controller are validated according to a wide spread of workloads. The proposed Flash controller develops its own method for the reorganization and mapping of invalid blocks in a Flash chip. This paper explains about new flash controller design and control signals for flash operations and also exploits the parallelism by using multiple channels or multiple controllers for single flash memory in order to reduce the further latency in read, write and erase operation.

Keywords: *NAND Flash Controller; Multichannel; SSD;*

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1. INTRODUCTION

The increase in use of digital equipment's in present day scenario has led to improvements in memory modules. In previous days the basic memory is nothing but Magnetic disk drives. The severe drawback of magnetic disk drives is due to its mechanical system, high latency and more power consumption.

Flash memory overcomes this drawback by having less latency, less power consumption and no mechanical system. Flash memory is faster than the traditional magnetic disk drives.

There is mainly two types of flash memories available in the market, they are NAND flash memory and NOR flash memory. Basically this difference is because of the interconnection. NOR flash memory is known for random access capability and NAND flash memory is known for large density and high read and write speed.

The flash memory used for large data storage is NAND flash. NAND flash is non-volatile and will be used mostly in day today's electronic and digital equipments. NAND flash memory is most popular storage technology for solid-state drivers (SSDs) due to low-power consumption, light weight, and non-volatility. Each NAND flash cell consists of a floating gate transistor whose threshold voltage can be programmed by injecting certain amounts of charge into the floating gate

A NAND controller required to handle the bit errors, the bad blocks, and also have to maintain the high data accessing speed, flash memory management, etc. The appropriateness of a NAND controller can enhance the reliability and increase the flash cycles of the flash memory. In addition, the system performance and product lifetime also improved by incorporating an excellent NAND flash controller in the NAND flashes storage systems. This paper designs a NAND flash controller which uses the state machine to manage a flash memory chip efficiently.

This paper is organized as follows. In section 2 and 3 we describe Motivation and related works. Multichannel NAND flash memory controller architecture is introduced in the section 4. The experiments and results are presented in section 5. Section 6 concludes this paper

2. MOTIVATION

Present day digital devices need a fast and powerful memory. The previously used hard disk drives highly complex systems consisting of electronic and mechanical components. Due to the slow mechanical latency, the disk I/O system has been repeatedly identified as a major bottleneck to system performance in many computing systems. The hard disk drives are also known for their high energy consumption which also effects complete device.

Because of these drawbacks we moved to flash devices. Flash memory is improvised version of hard disk drives but their working complete differs from hard disk drives. Flash memory contains different logical sectors, where each logical sector contains many blocks and each block contains different pages and data will be stored in pages as shown in fig 1. Flash memory writes in pages and erases in blocks. Flash memories are very fast compared to previous hard disk drives and them well known for their less power

consumption. The improved version of flash memory is multichannel flash memory. Where we use single flash memory but multiple controllers for the parallelism and to improve further latency

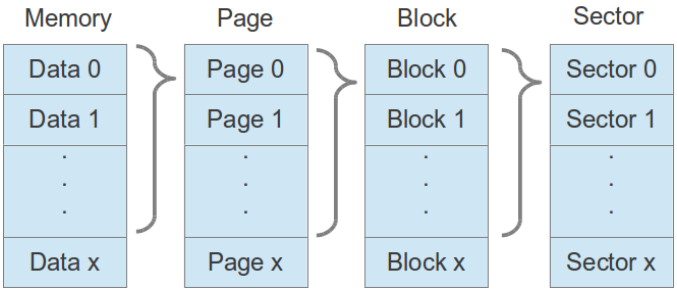

Fig -1: Flash memory Layout

3. RELATED WORK

In [3] Tang Li describes about basic controller design for flash memory. The controller basic work is to send the control signal or to measure the data adequacy. The proposed paper develop self designed controller to recognize and avoid mapping of invalid blocks.

In [1] soya Teresa and Pradeep discuss about multichannel NAND Flash memory controller by using single controller for each and every channel. This paper basically exploits the parallelism of multiple channels in flash memory so that more than one instruction will be processed at a time so that the lot of latency will be reduced compare to single channel Flash memory controller.

The paper [6] by koushal agrawal exploits use of Xilinx simulation for multi channel flash memory controller and it provide control signal in order to reduce the further complexity with respect to software simulation.

Flash Translation layer plays very important role with respect to flash controller as it uses for logical and physical address mapping the paper [8] exploits about flash translation layer use in the controller design.

The Scalable techniques for controller design have been shown in [4]. The controller designs with respect to SOC are shown in [5].

4. MULTICHANNEL FLASH CONTROLLER

Controller looks after the every instruction given to flash memory as the name indicates. Multichannel basically exploits parallelism in a flash memory. By using multiple controllers we achieve this parallelism. The basic multichannel flash design will be as shown in the figure 2.

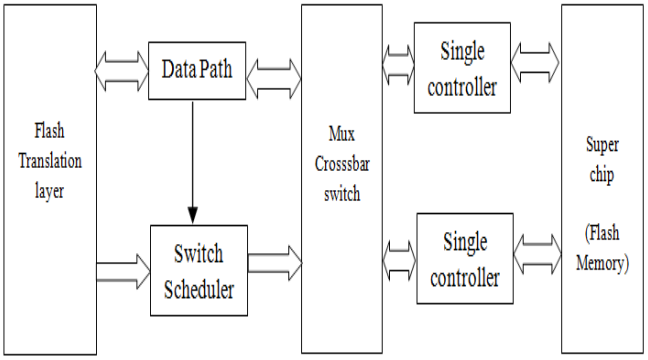

Fig 2: Multichannel NAND Flash design

The host requests are directly fed into flash translation layer. This converts physical address to logical address. The multiplexer is used for the purpose of choosing the controller. The flash memory will be accessed through flash controller which chosen by mux. The logical address is converted into main logic and control logic. Main logic contains the data and control logic contains control signals for specific function to perform in controller such as write, read and erase.

The control signal working can be seen by using finite state machine (FSM) as shown in fig 3

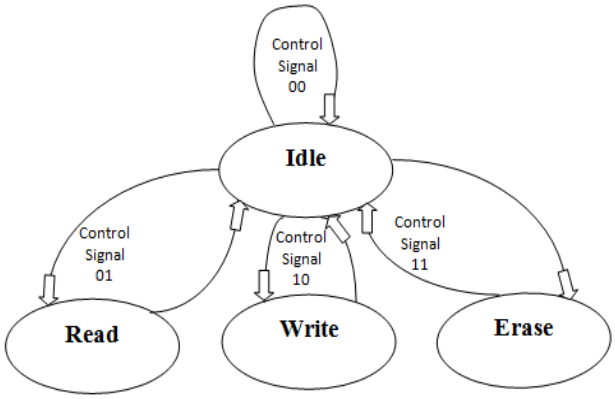

Fig 3: Finite state machine for controller

The controller basically will be in idle state and they will move to read, write and erase state as shown in table 1. After completion of each function the controller will reach the ideal state.

Table 1: Controller operations

Control signal	***Operation***	***Action***
00	Idle	Controller will be in idle state
01	Read	The data will be read by host from flash memory
10	Write	The data will be written into flash memory by host
11	Erase	The block of data will be erased from flash memory

4.1 FTL

Flash Translation layer or FTL basically emulates as a hard disk drive which eventually translates host requests into flash requests. An FTL provides some core functionalities such as address translation, bad block management, wear-leveling, and error correction and code checking. An FTL receives read and write requests from the file system and maps a logical address to a physical address in the NAND flash. The key role of an FTL is to redirect each write request to an empty area of flash memory, thereby avoiding the "erase-before-write" limitation of flash memory

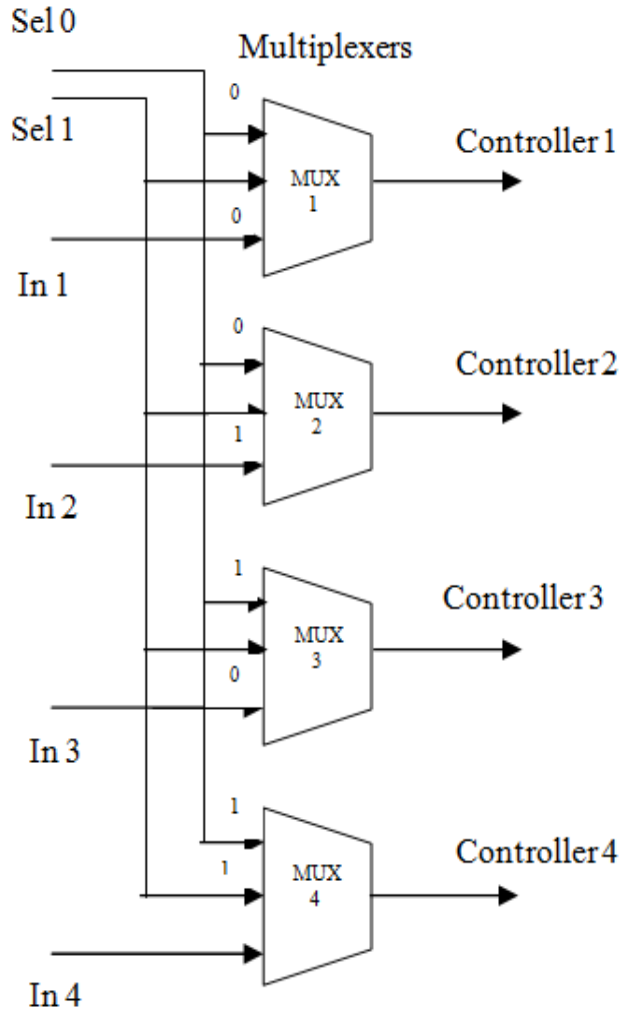

Fig 4: Multiplexer for 4 Controllers

4.2 Crossbar Switch

As we are interested in multichannel flash memory we have to use some sort of selector, which are nothing but multiplexers. Mux will be used for selection purpose the select lines for mux will be given by switch scheduler in the block. The multiplexer will be seen as shown in the fig 4.

The inputs to multiplexer will be different data requests and it will give to different controllers depending on select signal.

4.3 Flash Controleer

Controller gets the data from switch scheduler and it will perform operations as per table given in table 1 as per given control signal. The typical flash device will be as shown in the fig 5.

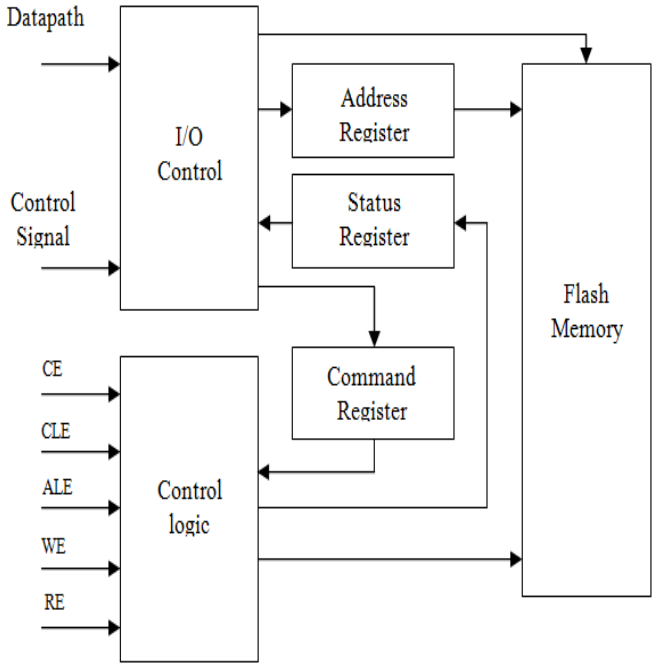

Fig 5: Typical flash controller

The inputs to controllers are converted inputs from Flash Translation Layer (FTL). The FTL translates host requests into flash requests, where the host requests such as read and write requests are specified in terms of logical sectors. The FTL issues the commands, addresses and data to the multichannel controller via the channels of the datapath. When receiving the requests the switch scheduler sends the select signal of the crossbar switch, then switching circuit sends the request to a single controller decided by the address of the request. Then according to the type of the requests the single controller sends corresponding control signals to NAND flash chip to complete the operation like read page, program page, erase block. The data transfer occurs between the controller and the host through the datapath.

It consists of address register, data register, command register, main logic and the control logic. This has single IO path to the memory transactions, which shares the addresses, command and data.

When a request arrives the main state machine will identify the operation from the command code, and it will sends an information to the identified operation sate. After that control goes to sub-state machine and generate control signals to perform the corresponding operation. After the complete implementation sub-state machine sends done signal to the main state machine that informs the completion of action.

The control signals to the control logic are explained as below

a) CE: This pin indicates NAND flash chip enable. This pin is high indicates the NAND flash memory controller are in working mode, it reflects that the data is storing in a memory in sequential order. When it is low, the NAND Flash memory controller does not work.
b) CLE: This pin indicates NAND flash clear mode When this pin is high the data are cleared in the main memory of NAND flash memory controller. When it is low it will not work.
c) ALE: This pin indicates NAND flash advanced latch enable when this pin is high, the NAND flash memory controller work and when it is low the NAND flash memory controller are in latch mode.
d) WE: This pin indicates NAND flash in write operation when it is high; data are in writing process in a write mode i.e. we can write the data at particular memory address. When it is low it will not provide a permission to write the data.
e) RE: This pin indicates NAND flash reset when this pin is low, it will work properly and if it is high the NAND flash memory controller are in reset mode i.e. all operations of NAND flash memory controller stopped.

5. RESULTS

With references to above discussion performance of HDD, single channel flash and multichannel flash has been tabled, latency and speed of all three devices are compared. Where IOPs in speed means Input Output Operations per Second

parameters	***Speed (IOPs)***		***Latency***	
Device	***Read***	***Write***	***Read***	***Write***
HDD	160	270	5ms	5ms
Single Channel Flash	1050	2100	20us	200us
Multichannel flash (4 Channels)	2370	3890	8us	60us
Multichannel Flash (8 Channels)	4150	6530	4us	30us

6. CONCLUSION

The Controller for multichannel NAND Flash has been designed and parameters like latency and speed (IOPs) has been compared with HDD and single channel flash controller. It's been noticed that there will be great deduction in latency in multichannel NAND Flash memory and also the input output request of multichannel is very high compared to single channel flash memory, hence they will be used in high data requesting devices

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