MODELLING OF NEXT ZEN MEMORY CELL USING LOW POWER CONSUMING HIGH SPEED NANO DEVICES

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Abstract

Hybrid SET-CMOS circuits which syndicate the assets of both the SET [Single Electron Transistor] and CMOS depicts highest possibilities to be incorporated in practical implementation for future low power VLSI/ULSI configurations. The proposed work is an attempt based on SET-CMOS hybrid circuit to realize the next gen simple Memory Cell. The authors adhered to MIB model for SET and BSIM4 model for CMOS in realizing the complex cell. The maneuver of the proposed circuit is verified subsequently in standard environment. The outcomes are in good trade off with the conventional statistics of existing memory cell.

Keywords: *SET, SED, Hybrid CMOS-SET, MIB and Memory Cell*

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1. INTRODUCTION

The 2003 edition of the International Technology Roadmap for Semiconductors forecasts the pathway of ultra-thin body (UTB) CMOS transistors by 2015; the possible miniaturization is to reach gate lengths within 10 nm. This in fact renders that today's device speed has enhanced by four orders of magnitude from the earlier device speed [1 & 2]. It gives the impression that the device scaling down trend of CMOS transistors is likely to endure its exponential growth for the next few couple of decades. Contrariwise, Moore's prediction of device down scaling by no means is a never-ending process. The penalties of technological limitation on CMOS technology immensely distress the trimming of CMOS transistors. Researchers reported several empirical studies based technological limitations owing to physical laws, application limits and the manufacturing limitations [3 & 4]. Such has endangered the end of CMOS technology possibly within this decade; thus the requisite for a successor is now foreseeable.

Then after the exploration of possible successor technologies with greater scaling potential attracted Researchers. Few new invented technologies are Rapid Single Flux Quantum (RSFQ), Resonant Tunneling Diodes (RTD), Single Electron Device (SED), Carbon Nano-tubes and Magnetic Spin devices [5 - 14] and reports revealed that they are quite impressive in post CMOS era. Manipulation of a single charge of electron through tunneling is the ultimate point of operation in device electronics. This is a major research boom for the last two decades and also produced several new technologies. This attributes electron transport metaphor in confined structure in nano regime. The Single Electron Tunneling (SET) technology has created high expectations for post CMOS era as it is compatible for designing low power consuming nano-scaled device that posses high integration density [15 - 18]. The development made so far in SET technology is divided in: - (i) Device Research which consist of device fabrication and fabrication technology studies. Scientists all over the world have devoted largely in this category; and (ii) The Application of SET devices for various purposes is a different and completely new aspect to explore but only a little has been achieved in this category. In present context, authors are emphasizing in realizing fast switching, low power and less space consuming SET based memory cell to substitute the conventional CMOS memory cell as SET appears better candidate for the survival of the fittest in modern electronics [19 - 22].

1.1 Diagnostic Study of Set

Describing SET is quite similar to a small conductor, which is at the outset an 'electro neutral', having exactly as many electrons as it has protons in its crystal lattice. In this form any significant electric field is not generated by the island afar its border. Predominantly an additional electron may propel in due to a weak external force. Now the net charge is e^-. Here the charging energy of the island is denoted by E_C, where the total capacitance is C and E_C can be calculated as [23 & 24]

$$E_{c=}\frac{e^2}{C}$$

Most interestingly only if the size of the island becomes equivalent with the de Broglie wavelength of the electron inside the island, the energy quantization

$$E_{N=}\frac{(n\pi\hbar^2)}{2xw^2}+\frac{\hbar^2k^2}{2x}$$

$$E_a = E_C + E_K$$

$$E_K = \frac{1}{g(\epsilon_F)V}$$

The most promising applications for SETs are (i) charge-sensing applications such as the readout of few electron memories, (ii) the readout of charge –coupled devices and (iii) precision charge measurement in metrology. Beneath here the authors have included the general architecture of SET in Fig 1 and 2.

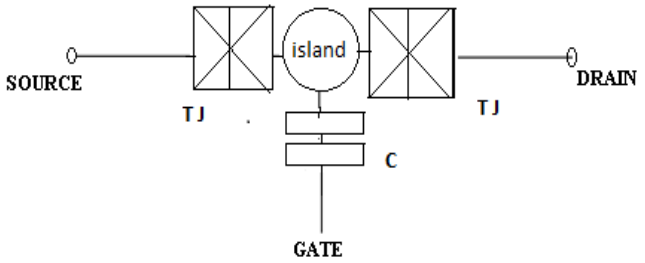

Fig -1: Simple SET structure

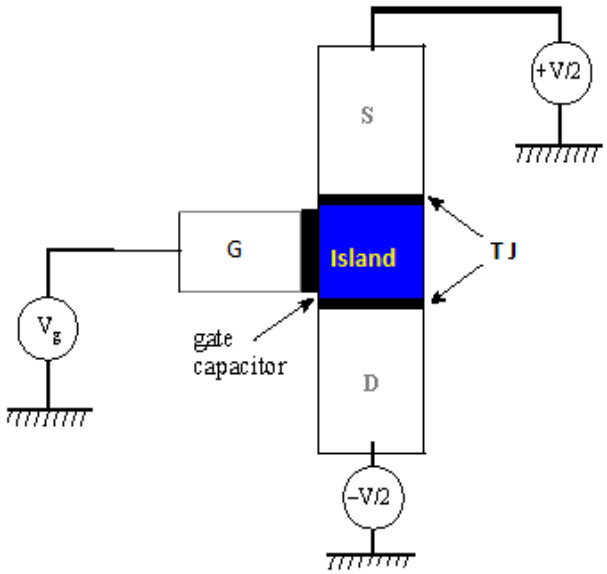

Fig -2: Detailed realization of SET

1.2 Need of Hybridization

Detailed research in SET has attracted attention as a candidate for future VLSI circuits owing to its three features: nano scale feature size, ultralow power dissipation, and unique Coulomb blockade oscillation features. Amid such overwhelming properties, the practical execution of the SET is under scanner because of its low current drive and lack of mature room temperature operable technology. SET advocates low power consumption and new functionality (related to the Coulomb blockade oscillations), while CMOS has advantages such as high-speed driving and voltage gain that can compensate for the intrinsic drawbacks of SET. Though a complete replacement of CMOS by SET is not easy task to achieve but simultaneously it is also true that the combination of SET and CMOS can bring a new era in VLSI technology [25 -28].

Researchers at Delft University in Netherlands endorsed a SPICE simulation package for SET circuit [29] employing Orthodox theory of SET. The authors here follow the SET-MOS quaternary transmission gate [30] which is highly accredited and mostly cited in reputed journals. The co-integration model of Parallel-In-Serial-Out Shift Register were designed and further simulated on this above cited SPICE soft-computing layout which allows place sharing of SETs with the conventional MOS devices in one particular die area as elucidated in Fig. 3. More conveniently, the logic operations of the proposed circuit were first tested by simulation using T-Spice simulation software. Thereafter, MIB compact model for SET device and BSIM4.6.1 model for CMOS was incorporated for obtaining detailed empirical results which are briefly included in this presentation. Following are some realizations of Hybrid CMOS-SET based logic devices:

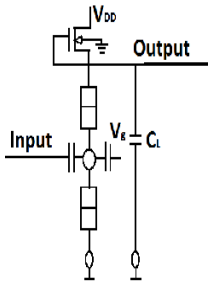

Fig -3: Hybrid CMOS-SET based simple Inverter

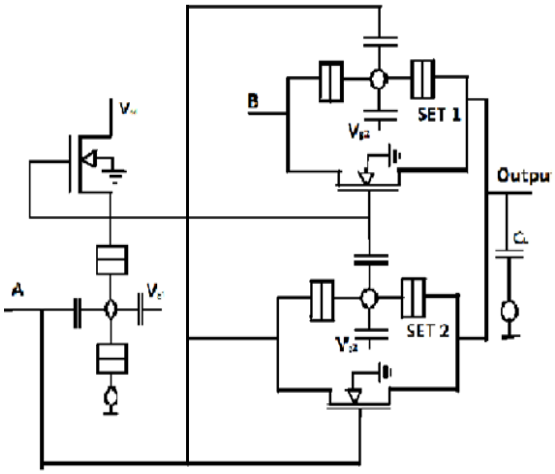

Fig -4: Hybrid CMOS-SET based simple AND logic implementation

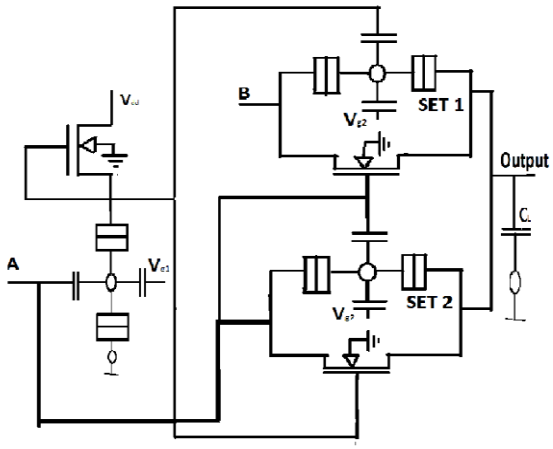

Fig -5: Hybrid CMOS-SET based simple OR logic implementation

2. BASIC MEMORY CELL CONCEPTUALIZATION

The memory cell is well defined as the fundamental building block of memory, usually implemented using bipolar, MOS, and other semiconductor devices or from magnetic material like ferrite cores or magnetic bubbles. Notwithstanding any of the implementation technology, the purpose of the binary memory cell remains identical as it stores one bit of binary information at particular time span and it must be set to store a 1 and reset to store a 0. Memory is a key element of digital systems and is also employed in designing temporary storage of the output of combinational circuits – thereby creating sequential circuits. Its output solely depends not merely on the present value of its inputs, rather on the circuit's previous state. Orthodox theory on memory cells are reported several times in SCI journals [31-33]. The incorporation of memory cells are thereby very common in today's computer kernels.

2.1 Proposed Hybrid CMOS SET based Memory Cell

The authors refer here the proposed model enumerated in Fig. 6. This cell comprises of low power consuming hybrid CMOS SET based R-S flip-flop and the inputs are controlled by hybrid CMOS SET based 4-input AND gates. In order to perform the desirable read/write operation on this cell, the control points is made high i.e., 1. Here logic 1 is made by giving input voltage @ 0.8mV and the logic 0 is provided by making the input voltage equal to 0mV. Thus the circuit can operate in very low voltage. More conveniently the hybrid CMOS-SET based memory cell is extremely low power consuming device.

2.1.1 Write Operation

For writing data into this memory cell, the authors ponder over the following control signals.
X-select = 1
Y-select = 1

$$\overline{RD}/\mathrm{WR} = 1$$

Under these signal conditions, the first three AND gates (starting from the left) and the AND gate just beyond the flip-flop are enabled while AND gate that drives the output is disabled. Data present on the data line is therefore transferred through three AND gates and are loaded into the flip-flop.

2.1.2 Read Operation

For read operation, the memory cell has to perform in the following manoeuvre

X-select = 1
Y-select = 1

$$\overline{RD}/\mathrm{WR} = 0$$

X-select and Y-select signals enable two AND gates in the middle section of the proposed model, but the $\overline{RD}$/WR remains 0 i.e., it is disabled. Then after again the first three AND gates are periodically enabled and simultaneously the same occurs for the last output driving AND gate. this ensures that the consecutive last two AND gates remain enabled and output becomes available on the date line.

3. CONCLUSION

The design and simulation of hybrid CMOS-SET basic memory cell is modelled successfully and the results are obtained categorically to expose the underlying potential of perfect co-integration of CMOS-SET. One remarkable attribute is that the SET and CMOS are placed in series and thereby the hybridization achieved improves the gain of the models and simultaneously the propagation delay is lessened to some extent. Based on the hybrid CMOS-SET logic gates, the model was designed and implemented using sophisticated simulation software.

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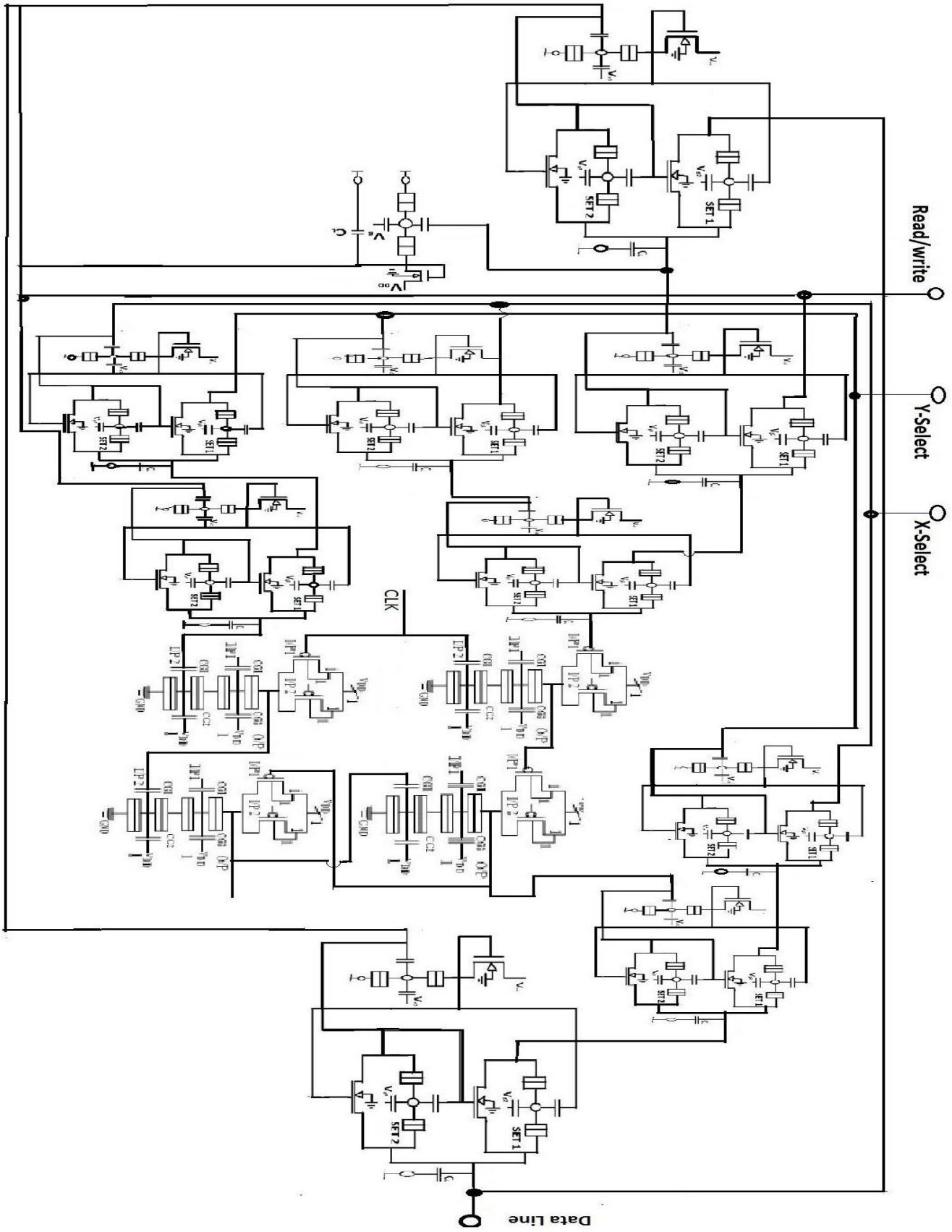

Fig -6: Hybrid CMOS-SET based Memory Cell