LOW POWER LOW VOLTAGE OPERATION OF OPERATIONAL AMPLIFIER

Abhishek Chakraborty[1]

[1]*B.Tech (ECE), Adamas Institute of Technology, WBUT University, West Bengal, India*

Abstract

The increasing demand for high performance, battery-operated, system-on-chip (SoC) in communication and computing has shifted the focus from traditional constraints (such as area, performance, cost and reliability) to power consumption. With the increasing integration level, energy consumption has become an important issue. Consequently much effort has been put in achieving lower dissipation at all levels of the design process. Minimizing power saves energy, simplifies cooling and contributes to device longibility. The low power design can increase operation time and /or utilize a smaller size and a light-weight battery. Low voltage operation is demanded because it is desirable to use as few batteries as possible for size and weight consideration. Low voltage analog circuit design techniques considerably differ from high voltage design technique .There are so many strategies available for low voltage design. In the field of Analog electronics we generally apply ±15 V or ±12V for proper operation of operational amplifier. In this paper it is shown that if we apply ±5V, then also all the op-amp electrical parameters(such as input offset voltage, input bias current, input offset current, CMRR) maintain datasheet specification for a particular type of IC. Here LM741C IC has been chosen to represent the operation of operational amplifier at ±5V. Here MULTISIM is used for the simulation purpose and the change in the external biasing circuitry is made to meet the datasheet specification of LM741 IC. Research is needed to provide intelligent policies for careful management of the power consumption while still providing the appearance of continuous connection to system service and application.

Keywords: *low power, low voltage, input offset voltage, input bias current, CMRR.*

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1. INTRODUCTION

It's no secret that power is emerging as the most critical issue in system-on-chip(SoC)design today. Power management is becoming an increasingly urgent problem for almost every category of design. Some key principles of low power design are using of lowest possible supply voltage, using the smallest geometry, highest frequency device but operating them at lowest possible frequency, power management by disconnecting the power source when the system is idle.

Voltage gain of the amplifier typically depends on the load resistor and other parameters that may vary considerably with temperature or process. Variation with process means that circuits fabricated in different "batches" exhibit somewhat different characteristics [1].

2. INVERTING AMPLIFIER IN ±5V

The non-inverting amplifier consists of an op amp and a voltage divider that returns a fraction of the output voltage to the inverting input.

$$Vin2=\{R2/(R1+R2)\}*Vout \qquad (1)$$

Figure-1 shows the above arrangement where both the theoretical value and simulated value are matched. In the following figure multimeter-XMM1 and XMM2 is used to show the corresponding output.

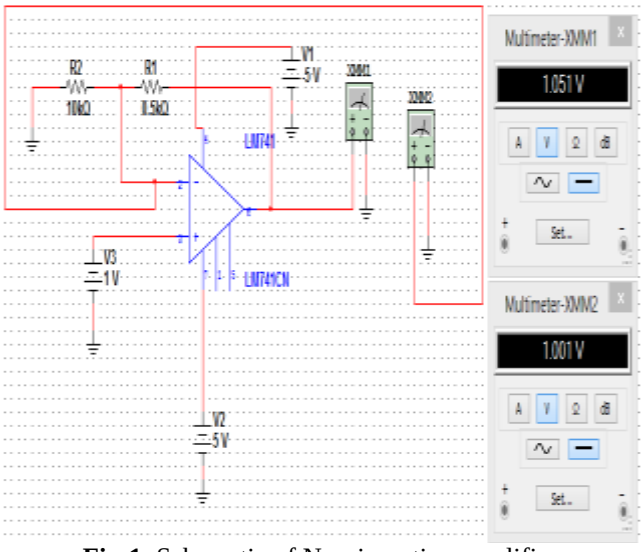

Fig-1: Schematic of Non-inverting amplifier

In the above figure Vin2 is the input voltage at the inverting terminal and Vin1 is the input voltage at the non-inverting terminal and it is clear that Vin1≈ Vin2.

3. OUTPUT VOLTAGE IN ±5V

The circuit arrangement is shown in figure-2 where the values of the resistances are chosen to get the output voltage in ±5V. Here also it is observed that the both the theoretical value and simulated value are matched.

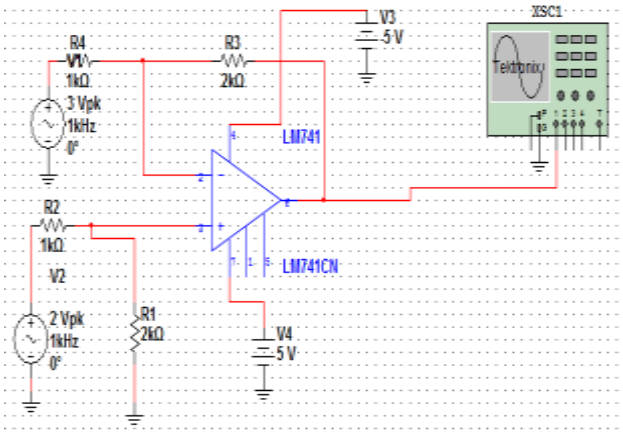

Fig-2: Schematic of Maximum output voltage in ±5V

Here the output voltage comes from the equation:

$$VO= (R3/R4)*(V1-V2) \qquad (2)$$

Using the value of the resistors used n the above circuit the theoretical value for the output voltage should come 2 V.

From the simulator using oscilloscope also 2 V output voltage is obtained and it is shown in the figure-3.

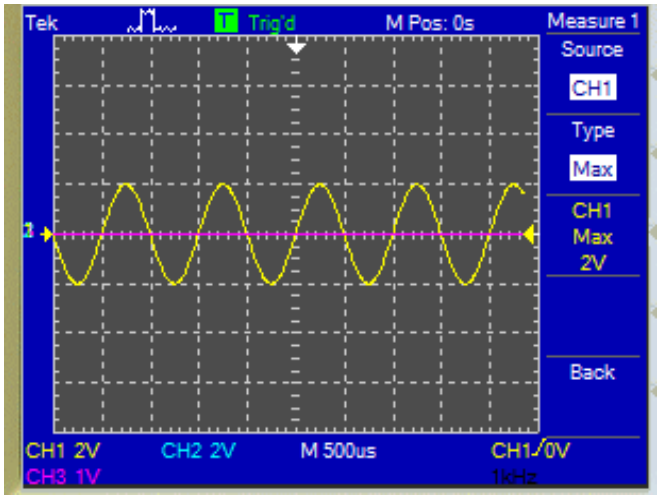

Fig-3: Simulated output voltage in ±5V

4. INPUT OFFSET VOLTAGE IN ±5V

Input off-set voltage is defined as the output off-set voltage divided by the gain of the amplifier when difference in the input offset voltage is zero [2]. The internal circuit of the op-amp experiences random asymmetries during fabrication and packaging. The bipolar transistor sensing two inputs may display slightly different base-emitter voltages. Input off-set voltage is the voltage which when applied to the input of the op-amp the output should be zero**.** But if no voltage is applied to the input of the op-amp, then in that condition the measured output voltage is the offset voltage of that op-amp due to input bias current of the op-amp. Figure-4 shows the arrangement for measuring offset voltage.

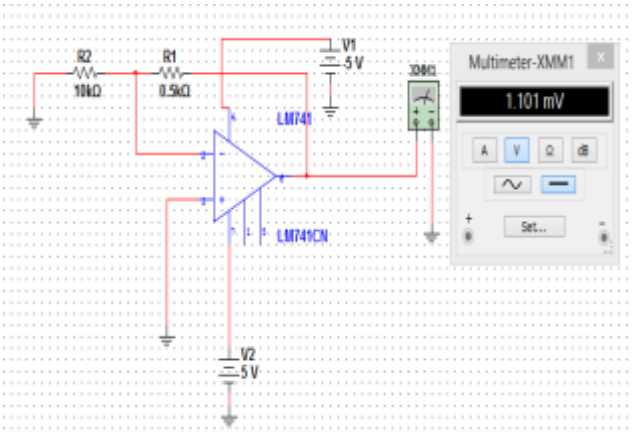

Fig-4: Schematic of Input offset voltage measurement

Input offset voltage comes from the equation:

$$VO = [(R2+R1)/R2]*Vio \qquad (3)$$

In the above equation assuming the value of Vio=1mv, the output should come 1.05mv theoretically. In simulator the output is coming 1.1mv. Near about both the values are matched here also.

5. INPUT BIAS CURRENT AND INPUT OFFSET CURRENT IN ±5V

Op-amp implemented in bipolar technology draws a base current from each input. The external circuit arrangement for measuring input bias current and input offset current is shown in figure-5.

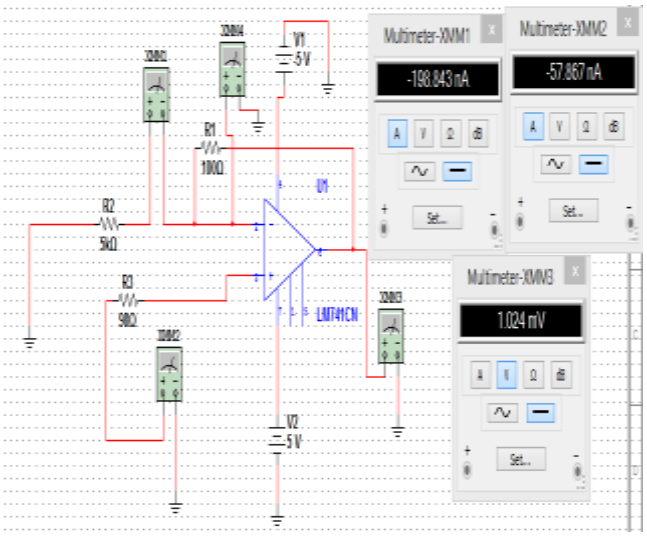

Fig-5: Schematic Of Input bias current and offset current measurement

Here R3 is chosen such that R3=R2||R1. R3 is called as offset minimizing resistor as input bias current can be minimized by selecting R3=R2||R1. Even if the input offset current is not zero, the effect of input bias current can be minimized by incorporating resistor R3. In experimental set up it is observed that offset voltage is 1mV. Here for measurement of input bias current value of R2 is chosen to

keep constant input offset voltage at 1 mV. IB1 is measured by XMM1 multimetre and IB2 is measured by XMM2 multimetre. VOIB is shown by XMM3 multimetre. So input bias current:

$$IB= (IB1+IB2)/2 \quad (4)$$

and input offset current :

$$IOS = (IB1-IB2) \quad (5)$$

Theoretically from the set up, 100IB1+5000IB1=1.024.So the value of IB1 =200nA.Using simulator the value of IB1 is obtained as 198.843nA. The value of input offset current is 140.97nA.

6. COMMON MODE REJECTION RATIO

Common -mode rejection ratio (CMRR) is defined in several essential equivalent ways by various manufacturers [3].Common mode rejection ratio measures how the output changes in response to the change in common-mode input level. A high CMRR is important in application where the signal of interest is represented by a small voltage fluctuations superimposed on a(possibly large) voltage offset, or when relevant information is contained in the voltage difference between two signals[4].CMRR is defined in terms of differential gain and common mode gain as:

$$CMRR= Ad/|Ac|$$

$$Or, CMRR=20*\log (Ad)-20*\log (|Ac|) \quad (6)$$

The experimental set up for determining CMRR is shown in figure-6.

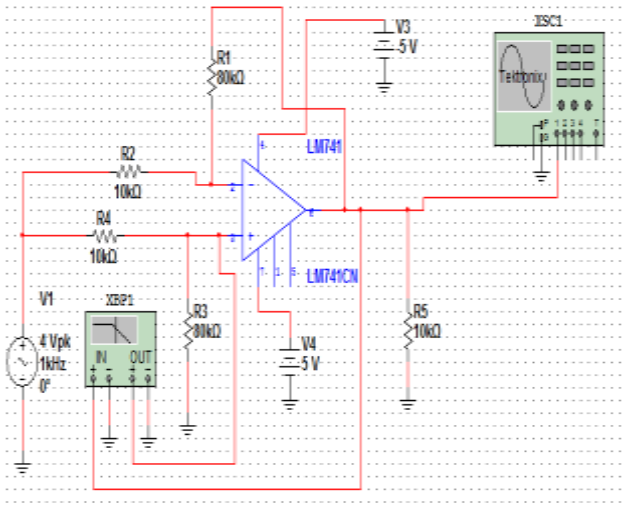

Fig-6 : Schematic of CMRR measurement

From the experimental set up it is clear that the signal at pin 2 or pin 3 is essentially common –mode signal VC, where

$$VC= [R3/ (R3+R4)]*V1 \quad (7)$$

$$= [R1/ (R1+R2)]*V1 \quad (8)$$

From the experimental set up it is clear that R1>R2 & R3>R4. Also it is clear that R1=R3 & R2=R4.

Voltage across R2 is:

$$[Vi-V1R4*(R4+R3)] \quad (9)$$

and voltage across R1 is:

$$[VO-Vi-V1R3/ (R4+R3)] \quad (10)$$

Here Vi is voltage across pin no 2 and 3.Now equating current through resistor R1 and R2 and assuming R2=R4 and R1=R3, it is obtained that:

$$Vi= [R2/(R2+R1)]VO \quad (11)$$

It is known that:

$$VO= AdVi +AcVc \quad (12)$$
$$= [(AdR2VO)/ (R2+R1)]+ [(AcR1V1)/(R2+R1)]$$

Now, if (AdR2)/ (R2+R1)>>1, then:

$$(AdR2VO) + (AcR1V1) \approx 0 \quad (13)$$

And then Ad/Ac =R1/R2 [V1/VO] = CMRR

In the figure-6, to show the CMRR plot in dB , bode plotter has been used. Here theoretical value is coming approximately 66 dB where using simulator from the plot we are getting value of 70dB. For this CMRR measurement purpose AC analysis is made. The CMRR plot in db is shown in figure-7.

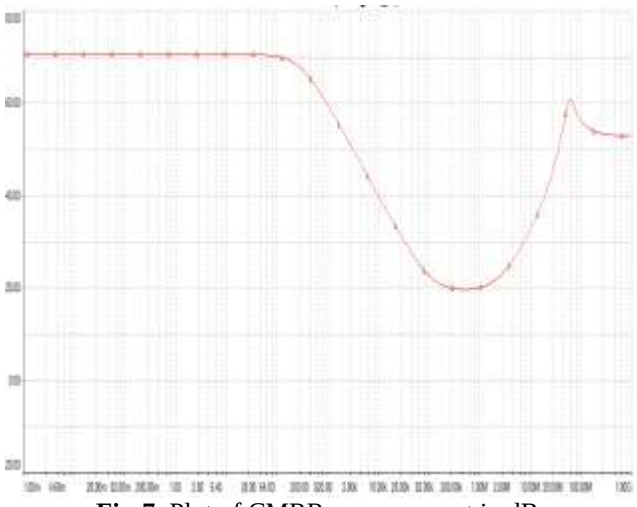

Fig-7: Plot of CMRR measurement in dB

Here to maintain LM741C datasheet specification value of source resistances (R2, R4) is taken 10KΩ, as mentioned in datasheet specification.

7. POWER CONSUMPTION

For power consumption measurement DC sweep analysis is done, where supply voltage range of -3 V to +3 V is selected as a DC sweep parameter. Finally consumed power has been

calculated across load resistance of 5 KΩ at the output of op-amp.

Plot of the consumed power is shown in figure-8.

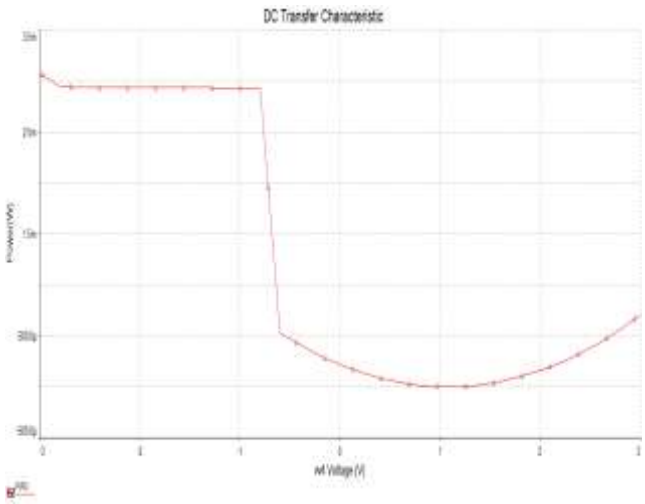

Fig-8: Plot of Power consumption

8. SIMULATION RESULT

In this paper all the values of resistors has chosen to meet datasheet specification of LM741C IC. Using table-1, a comparison is made between standard value and simulated value of LM741 IC. MULTISIM of National Instrument is used for the simulation purpose.

Table-1: Comparison in between standard value and simulated value

Name of the op-amp parameter	Standard value	Simulated value
INPUT BIAS CURRENT	0.8µA(max)	0.13µA
INPUT OFFSET CURRENT	300 nA(max)	140.97 nA
INPUT OFFSET VOLTAGE(Rs<=10kΩ)	6mV(max)	1mV
CMRR(dB) at Rs<=10 kΩ	70 dB(min)	70 dB
Power Consumption	----------	665 µW-3 mW (for DC sweep of -3 V to + 3 V)

9. CONCLUSION

In this paper an overview of the challenges imposed by the use of ±5V is presented. Analysing the above results and circuit arrangement it is clear that op-amp retain its characteristics in ±5V and thus work properly. So, instead of using ±15V, if ±5V is used, then power consumed by the circuit will be less and this less consumed power will increase the number of transistors on a chip.

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