DESIGN OF AREA AND POWER EFFICIENT HALF ADDER USING TRANSMISSION GATE

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Abstract

This paper gives an idea to reduce power and surface area of half adder circuit using very popular technique i.e. transmission gate. An adder is a digital circuit that performs addition of two numbers. In many computers and other kind of processors, adders are used not only in arithmetic logic unit but also in other parts of the processors where they are used to calculate addresses, table indices and similar operations .in this paper two bit addition has been done using conventional and transmission gate level and power, area and number of transistors are the scope of comparison. According to the simulation result, power and area are reduced by 55.35 % and 40.269% respectively when the circuit is implemented by transmission gate .thus transmission gate has become a very popular and useful technique to implement digital circuits which help to reduce power, surface area as well as number of transistors.

Keywords: *Transmission gate (TG), Half adder, CMOS logic gates, Surface area, Power.*

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1. INTRODUCTION

Now a day's low power and less surface area become the area of interest of VLSI system designers to design a digital circuit. The conventional CMOS gates implemented digital circuits do not fulfill these basic requirements. To overcome this problem they use a very important and effective technique i.e. transmission gate which gives better result in both field of power and area. The extensive development in the field of portable system and cellular network has intensified the research efforts in low power micro-electronics [1]. This paper concerns with one x-or gate which is one of the basic building block of various combinational circuits.

Transmission gate require lower switching energy and it reduces the count of transistors used to make different logic gates [2].

This paper uses a new design concept of X-OR gate using transmission gate with two inverter circuits.

In VLSI implementation, major problems are heat dissipation and power consumption. To solve this problem it is required to reduce power supply voltage, switching frequency and capacitance of transistors [3]. The strength of a signal is measured by how closely it approximates and ideal voltage source [4].

This paper uses DSCH3 simulation software for circuit simulation and MICROWIND3 for layout design. The technology used in this paper i.e. Transmission gate use less area and less transistors compare with conventional design logic. Area, delay and power dissipation have emerged as the major concern of the designers. The performance of the complex logic circuits is affected by XNOR-XOR circuits [5].

The DSCH3 program is a logic editor and simulation. It provides user friendly and fast simulation [6]. Transistor count is, of course, a primary concern which largely affects the design complexity of many function units such as multiplier and algorithmic logic unit (ALU). The limited power supply capability of present battery technology has made power consumption an important figure in portable devices. Here, we have given a brief description of the evolution of half adder circuits in terms of lesser power consumption, higher speed and lesser chip size. We have started with the most conventional 28 transistor full adder and then gradually studied half adders consisting of as less as 8 transistors.

With the development of the technology towards submicron region leakage power has become significant component of total power dissipation [7].In this paper, comparison of CMOS technology & transmission gate logic based on 90 nm technology with the help of XOR gate. The main advantage of the TG logic is complex logic functions are implemented by using small number of transistors. Another advantage is logic level swing can be reduced by using PTL.

The problems with transmission gate are it degrades the output as it passes through various stages and no isolation between input and output terminal. NMOS and PMOS device gives poor performances. The NMOS degrades the logic level "1" while the PMOS degrades the logic level "0'. Thus, a perfect transmission gate can be constructed from

the combination of NMOS and PMOS devices, leading to improved performances. The drawback in a transmission gate is that it needs inverted signal values to control gates of PMOS and NMOS, respectively [8].

2. HALF ADDER DESIGN

Half adder circuit needs two binary inputs and two binary outputs. The input variables designated the augends and added bits; the output variables produce the sum and carry [9].

The block diagram of half adder is shown in Fig-1.

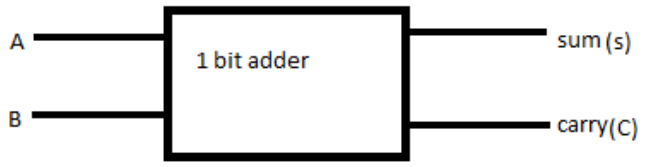

Fig-1: Block diagram of half adder

Table-1 gives the input output relation as

Table-1 Truth table of half adder

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

The simplified Boolean function according to the truth table is given as

$$S=A'B+AB'$$

$$C=AB$$

Fig-2 shows the equivalent circuit using CMOS logic gates which is called conventional logic gates.

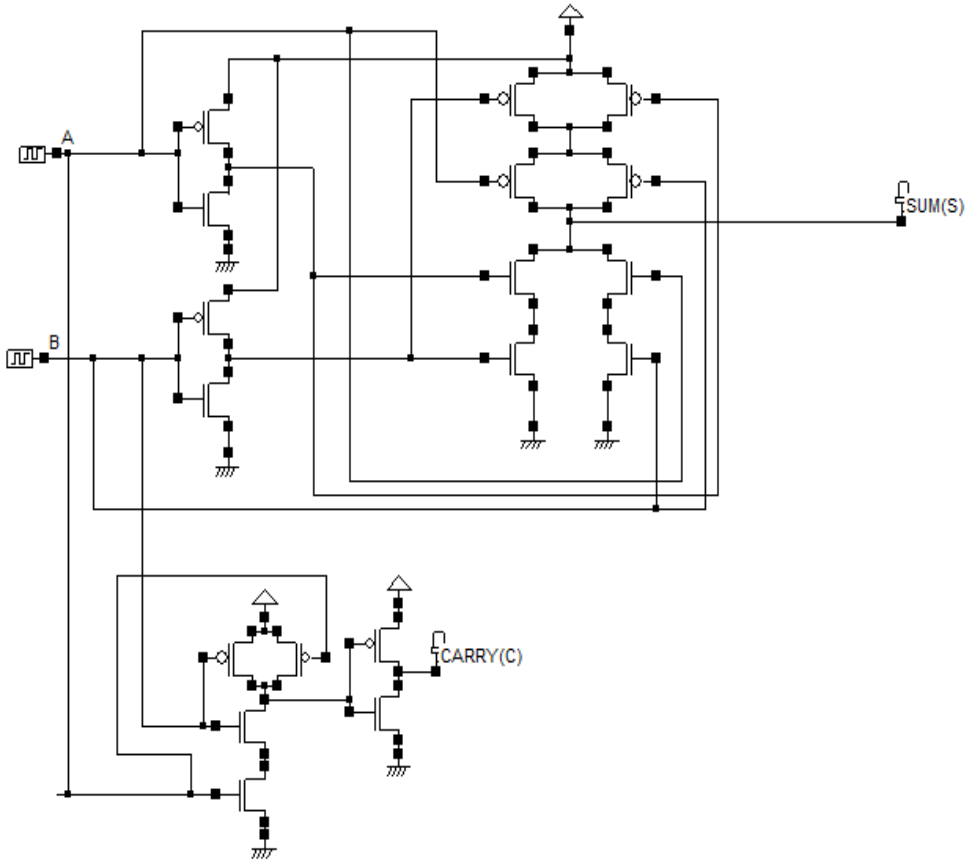

Fig-2: CMOS equivalent of half adder on DSCH3

Fig-3 shows the simulation result of half adder on DSCH3.

Equivalent full automatic layout design of half adder is obtain on MICROWIND3.1 as shown in Fig-4.

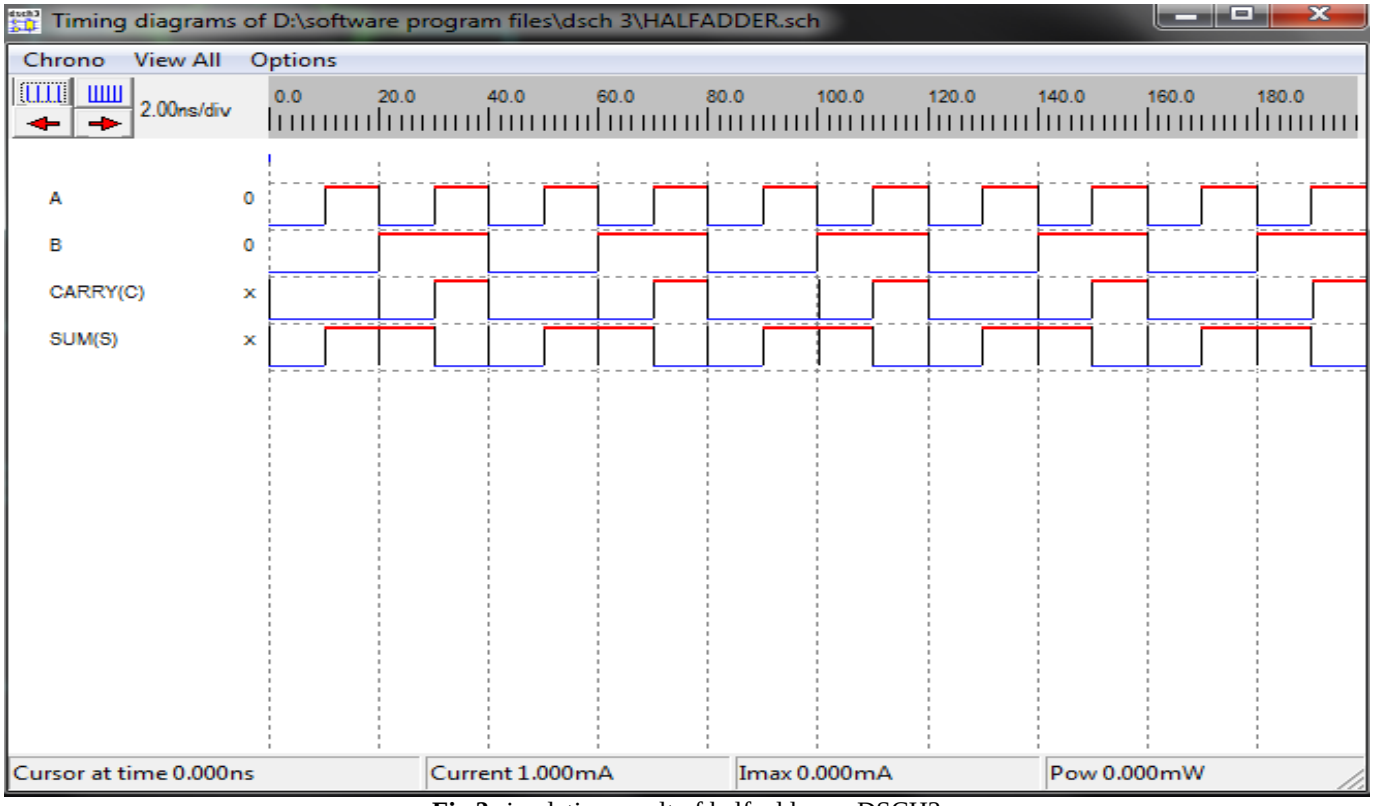

Fig.3 simulation result of half adder on DSCH3

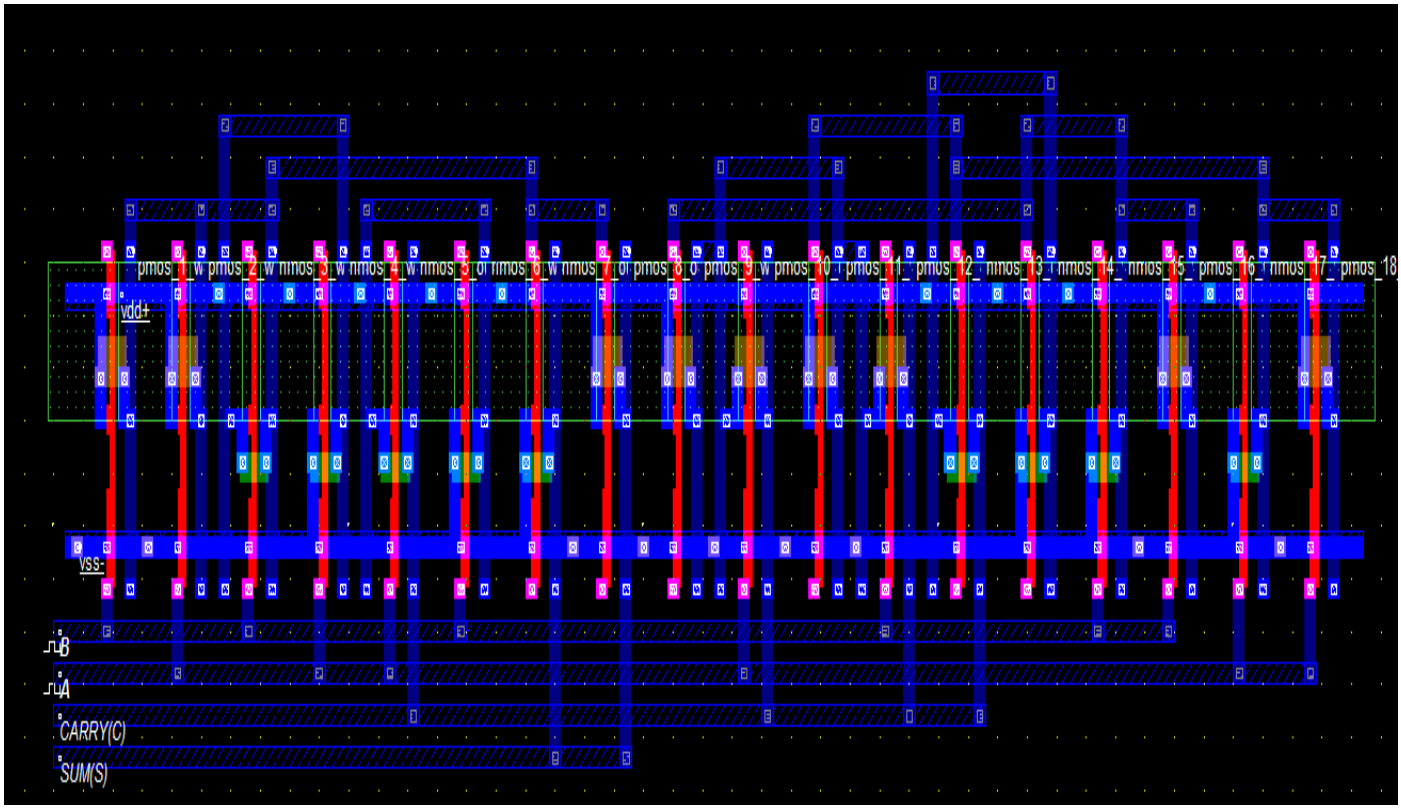

Fig-4: Full automatic layout design of half adder

Now the task is to make the original CMOS circuit of half adder with the help of transmission gate. Thus Fig-5 shows the half adder implementation using transmission gate on DSCH3.

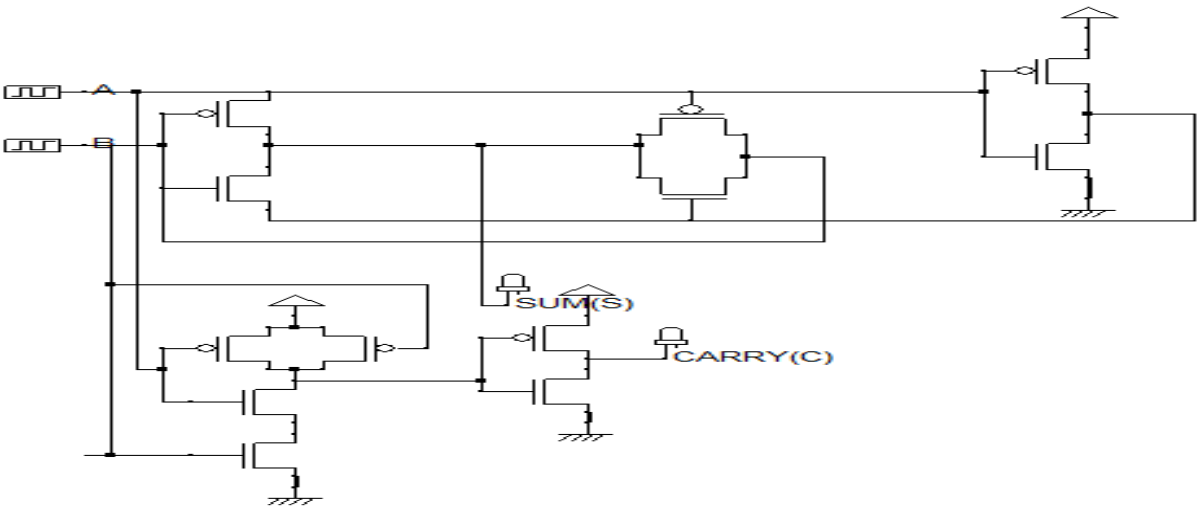

Fig-5: Half adder using transmission gate on DSCH3

Thus above circuit clearly shows that transmission gate reduces the number of transistors.

Again the full automatic layout design of transmission gate based half adder is shown in Fig-6 which is obtain on MICROWIND3.1

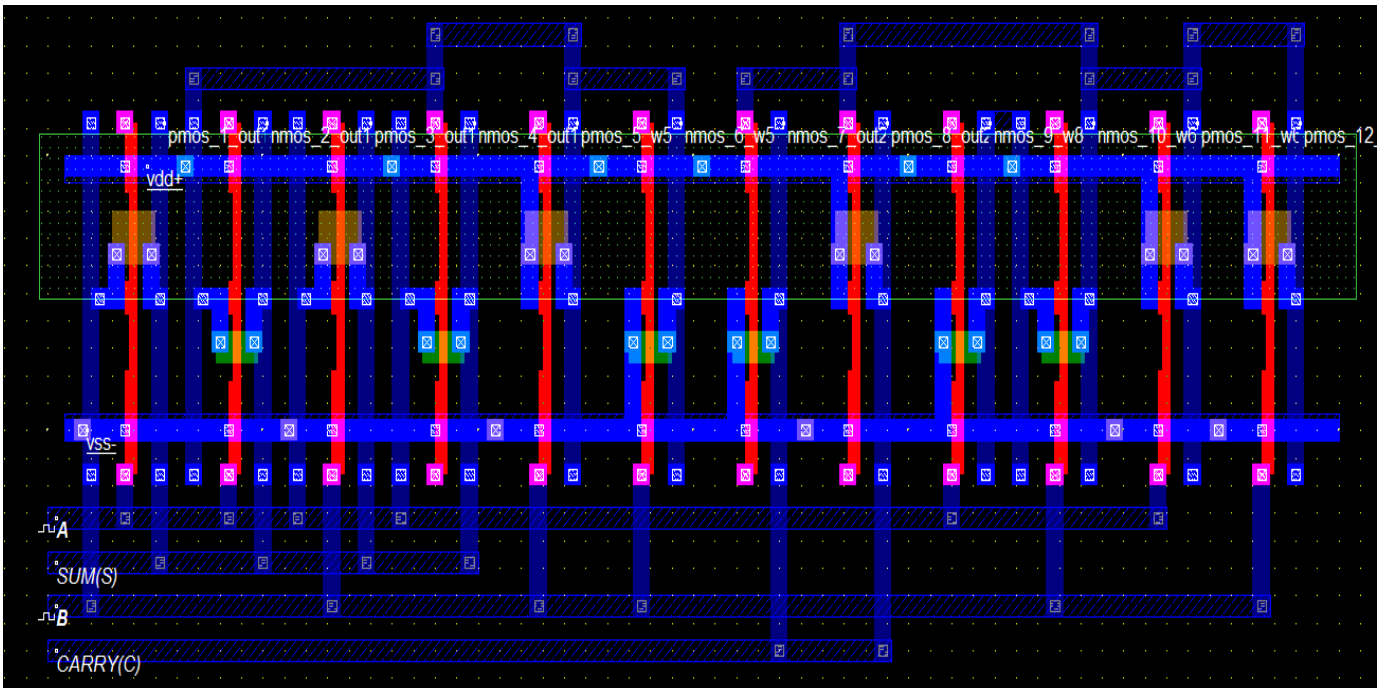

Fig-6: Full automatic layout design of half adder using transmission gate

The simulation result of half adder using transmission gate obtain on MICROWIND3.1 is shown in Fig-7.

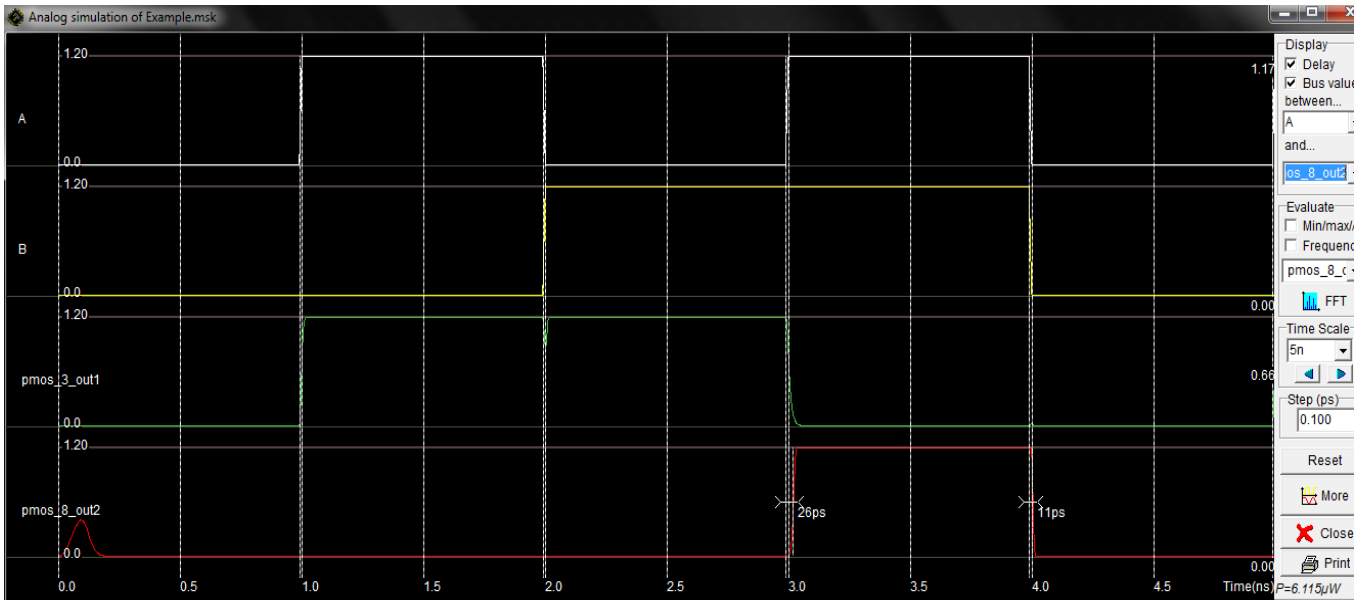

Fig-7: Simulation result of half adder using transmission gate on MICROWIND3.1

3. RESULT ANALYSIS

Comparative analysis between two types of design method i.e. Half adder using transmission gate and with ought transmission gate is shown in table-2. Comparison aspects are based on power consumption, surface area and number of transistors used. Comparison shows that transmission gate based half adder is better than half adder without transmission gate.

Table-2 Comparative Analysis

S.N.	PARAMETERS	HALF ADDER WITHOUT TG (DESIGN 1)	HALF ADDER WITH TG (DESIGN 2)
1.	POWER(µw)	13.696	6.115
2.	AREA(μm^2)	148.5	88.7
3.	NO. OF TRANSISTORS	18	12

Graphically we can compare these parameters which show the real view of comparison.

Thus chart-1, chart-2 and chart-3 show the comparison graph for power, area and number of transistors used in desire circuit.

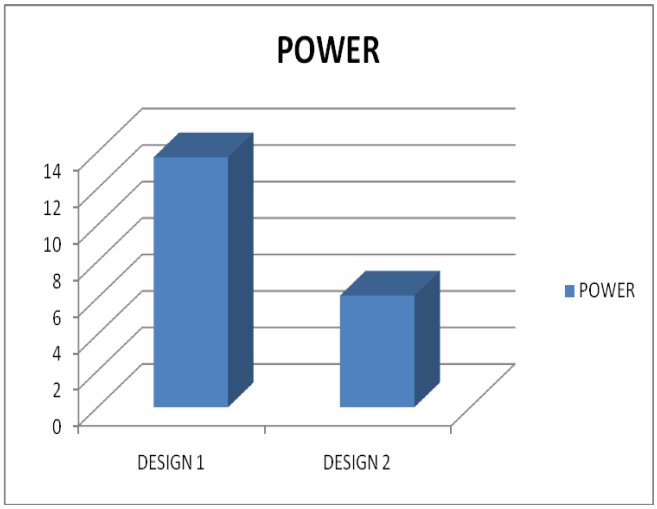

Chart-1: Power comparison between design-1 and design-2

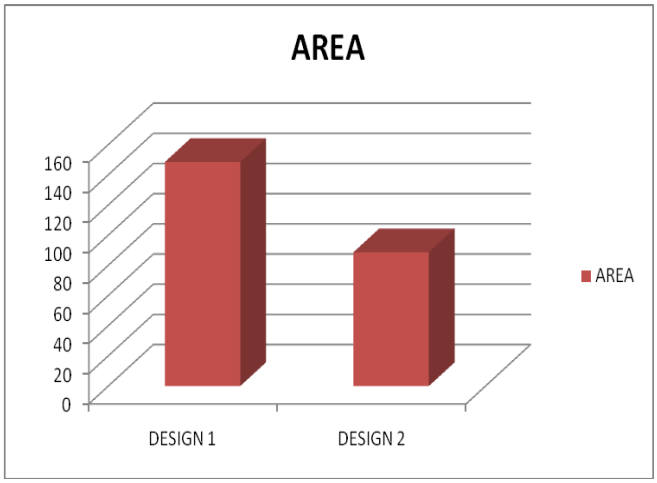

Chart-2: Surface area require for design-1 and design-2

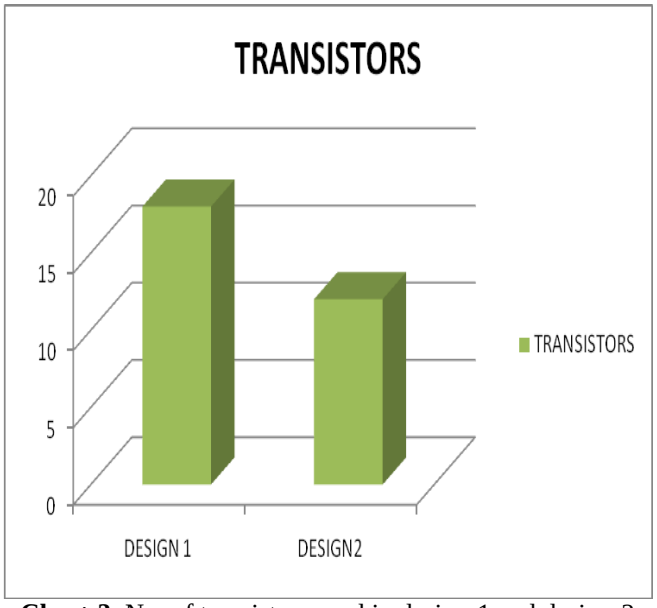

Chart-3: No. of transistors used in design-1 and design-2

4. CONCLUSION

From the above discussion we can conclude our discussion that transmission gate is very useful technique to reduce the surface area on a chip, number of transistors and power consumption.

So we focus here for transmission gate design analysis and find better result for all parameters point of view. Numerically power consumption is reduces by 55.35%, surface area is reduced by 40.269 % and required CMOS devices are reduced by 33.33%.

REFERENCES

[1]. Saradindu Panda, A.banerjee, B.maji and Dr. A.K. Mukhopadhyay, "Power and delay comparison in between different types of full adder circuits", International Journal of advanced research in electrical, electronics and instrumentation engineering, volume 1, issue 3.pp.168-172, 2012.

[2]. S,Goel.M.A. Elgamel, M.A. Bayoumi, and Y.Hanarty. "Design methodologies for high performance noise-tolerant XOR-XNOR circuits," circuits and systems I:Regular papers, IEEE Transactions on, vol.53,pp.817-878,2006

[3]. Richa Singh and Rajesh Mehra , "Power efficient design of multiplexer using adiabatic logic", International Journal of advances in engineering and technology, pp 247-254, march 2013.

[4]. Neil H.E.Weste, David Harris and Ayan Banaerjee, "CMOS VLSI design". Pearson Education,Inc., pp. 11, Third Edition, 2005

[5]. Nabihah Ahmad, Rezaul Hasan, IEEE "A New Design of XOR-XNOR gates for low power Electronic Devices", System and Applications(ICEDSA), pp.45-49, 2011.

[6]. I. Hassoune, D. Flandre, I. O'Connor and J.D.Legat:ULPFA: ANew Efficient Design of A Power Aware Full Adder", IEEE Transactions on Circuits and Systems I-5438,pp.2066-2074, 2008

[7]. Hanchate, N. Ranganathan "A new technique for leakage reduction in cmos circuits using self-controlled stacked transistors," 17th International Conference on VLSI Design,pp.228-233.2004

[8]. W.Jyh-Ming. F.Sung-Chuan, and F.Wu-shiung, "New efficient designs for X-OR and XNOR functions on the transistor level," solid-state circuits, IEEE journal, Of. vol.29,pp.780-786,1994.

[9]. M. Morris Mano, Michael D. Cilleti "Digital Design", 4th edition, pp.143, 2012.

BIOGRAPHIES

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