CONTROL ANALYSIS OF A HIGH FREQUENCY RESONANT INVERTER FOR INDUCTION COOKING APPLICATION

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Abstract

Stability of three possible close-loop control of a series resonant inverter is studied for induction cooking application. Ultimately, a single close-loop control technique is proposed in this work which can ensure both the power control as well as a satisfactory zero voltage switching (ZVS) in a finite control range near the operating point. A phase shift controlled series resonant inverter is used as a power supply for an induction cooking system. Its linearized model is developed for small signal analysis and a PID controller is designed for the proposed close-loop control and its performances are judged under various operating conditions using MATLAB/Simulink® platform.

Keywords: *ZVS, linearization, bode plot, step response, PID control.*

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1. INTRODUCTION

Induction cooking employs generation of thermal energy directly into the cooking vessel. In order to achieve efficient transfer of energy,thermal dissipation in the electrical supply system and the coil must be as low as possible in comparison to heat generated in the vessel.

Mechanically this is achieved by the special design of vessel which permits maximum flux linkage [1, 2]. From the electrical point of view, the load circuitry should be made to be in resonance at the supply switching frequency so that maximum power transfer can be ensured [3, 4]. However, in case of high power induction heating systems, the variation in resistance and inductance of the specimen at the high temperature especially when the work-piece reaches the curie temperature poses a major problem by changing the resonant frequency of the load circuit [5]. Thus, in order to have a robust design, the phase margin and the gain margin of the system should be well beyond the expected limit.

For induction cooking, supply switching frequency should be sufficiently high to increase heat generation. Lower limit is set by the acoustic noise generated in the supply and the utensils at the fundamental and the second harmonic to 20 kHz [6, 7]. Upper limit is decided by the problems posed on power semiconductor switches and their performance at the higher frequency owing to dissipation of heat generated in them. This problem can be solved by using special switching techniques like zero voltage switching (ZVS) [8], applied to voltage source inverters and zero current switching (ZCS) [9], applied to current source inverters. Using these techniques, either turn-ON or turn-OFF losses can be reduced to zero by making the load slightly inductive or capacitive. However, capacitive loads have inherent demerit of increase in diode reverse recovery stress which may result in voltage spikes in output voltage. To achieve ZVS in voltage source inverters, switching frequency is made slightly higher than the resonant frequency so that the load would be inductive and the current will be lagging in nature [10].Moreover, the frequency at which ZVS is achieved increases with the increase in phase shift between the switching pulses.

For different food stuffs, there might be a demand of different and accurate power transfer to maintain a given temperature profile. This can be ensured by controlling the output voltage of the resonant inverter. There are various methods described in literature for this purpose like phase shift control (PSC) [10, 11], asymmetrical voltage control (AVC) [12], asymmetrical duty-cycle control (ADC) [13]. Out of these, PSC produces symmetrical alternating output voltage (i.e. voltage pulse with equal positive and negative area) whereas AVC and ADC gives an asymmetrical output voltage pulse with a considerable DC content at the lower reference value. In AVC, negative area is constant and positive area is a function of duty-ratio; whereas in case of ADC both positive as well as negative areas are the functions of duty-ratio (with one being increasing and another being decreasing in nature). Thus, they can be used only for a limited band of operation. Apart from this, PSC has the advantage of simplicity in its implementation. Fig.1 shows block diagram for the proposed control scheme.

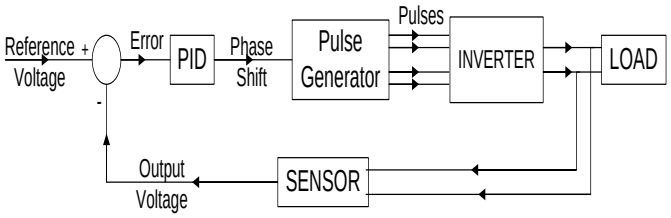


Fig 1 Control scheme for controlling the output power

In present work, a phase shift controlled voltage source series resonant inverter is used as power source for the induction cooker. Its switching frequency is linearly varied (within a finite acceptable range) [14] with change in phase

shift to ensure ZVS and its performances have been analyzed for different reference values. Rest of the sections have been categorized as such: *section 2*- system modeling (which presents a critical analysis and trade-offs between various complementary factors for load and frequency selection), *section 3*- small signal modeling, *section 4*- control scheme and operation, *section 5*- results and discussions and *section 6*- conclusion.

2. SYSTEM MODELING

2.1. Load Parameters

For an induction cooker, the load is the utensil in which heat is to be generated. For a fixed geometry and switching frequency, the selection of utensil material must be proper to obtain efficient heating. The surface resistance (R_s) offered by these materials can be empirically given by (1) [6, 15].

$$R_S = \Psi / \Delta \qquad (1)$$

Where, Ψ is the resistivity of the material and Δ is the skin depth. Hence, conductors with low value of resistivity and high skin depth results in less resistance offered to the eddy currents and thus in less generation of heat. Generally, conventional magnetic materials with quite low skin depth are used in such utensils. Again, the value of load resistance should not be low enough to give a steep selectivity profile at the resonant frequency (f_o) (as shown in Fig.2) so that a slight variation in switching frequency (f) doesn't have a much impact on output power.

In present work authors have considered a total load resistance of 3.2Ω. Since, the load is series resonant (at fundamental switching frequency), the values of inductance (L) and capacitance (C) are so chosen that they form an under damped circuit to produce required sinusoidal oscillation. This can be ensured approximately by fulfilling (2)

$$R \le 2\sqrt{\frac{L}{c}} \qquad (2)$$

Where, R is the equivalent series resistant (ESR) of the complete circuit including the resistance of the switches as well as that of the coil and capacitor. Values parameters of load and their values have been tabulated in Table-1.

Table 1 Load Parameters

Quantity	Symbol	Values
Load Resistance	R_s	3.2 Ω
Inductance of Coil	L	34 µH
Output Capacitance	C	1 µF
Resistance of Coil	R_L	0.53 Ω
Resistance of Capacitor	R_C	0.1 Ω
Resonant Frequency	f_o	27.272 kHz
Characteristic Impedance	Z_o	5.83 Ω

2.2. Frequency Selection

For a full bridge inverter, the relation between output power (P_o) and the f can be given by (3)

$$P_o = \frac{8V_{dc}^{\,2}R_L}{\pi^2 Z_O^{\,2}\left[\left(\frac{R_L}{Z_O}\right)^2 + \left(\frac{f}{f_O} - \frac{f_O}{f}\right)^2\right]} \qquad (3)$$

Fig.2 shows the variation of nominalised output power with nominalised switching frequency, (f/f_o) for the load considered above. To ensure ZVS, f should be either slightly less than or greater than the f_o. However, operation below resonance has the drawback of increased diode reverse recovery stress which results in spikes in output voltage. Thus, in the present work, load has been made slightly inductive by selecting f as 1.1 times f_o (i.e. 30 kHz) and is linearly increased to 1.2 times f_o (i.e. 33 kHz) as the phase shift is increased to 180° (discussed in detail in *section-4*). This increment doesn't have a much impact on the variation of output power as shown by blue curve in Fig.2.

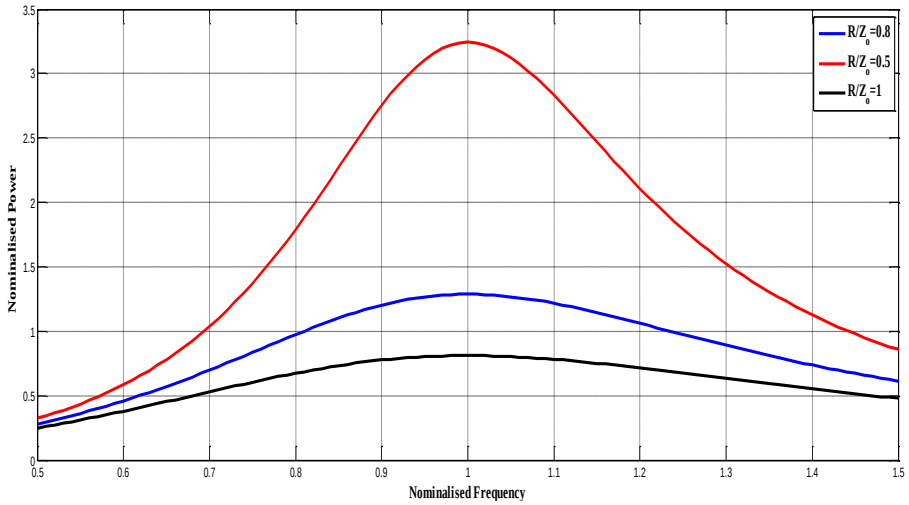


Fig 2 Variation of nominalised power with nominalised frequency for different ratios of R/Z_o

2.3. Switch Parameters

A full bridge inverter with *power mosfets* as the switching element is used in the present study. Details regarding various parameters have been provided in Table-2. Since $f > f_o$, turn-ON switching loss will be negligible for the switch (as observed from Fig.6). However, turn-OFF loss will be present.

Table 2 specification of switch

Quantity	Symbol	Values
Mosfet ON Resistance	R_{DS}	0.4 Ω
Diode ON Resistance	R_d	0.1 Ω
Diode Forward Voltage Drop	V_T	0.7 V
Maximum Current Stress	I_{SM}	15 A
Maximum Voltage Stress	V_{SM}	48 V
DC Source Voltage	V_{DC}	48 V

3. SMALL SIGNAL MODELING

State space model of the system (inverter + load) has been developed using harmonic approximation for the inductor current and capacitor voltage and then applying extended describing technique [16] to the input voltage [17]. The system is then linearized at an arbitrary operating point using Tailor's series expansion method to give a small signal model as shown by (4) to (7)

$$\overset{o}{x} = \begin{bmatrix} \frac{-R}{L} & W_S & \frac{-1}{L} & 0 \\ -W_S & \frac{-R}{L} & 0 & \frac{-1}{L} \\ \frac{1}{C} & 0 & 0 & W_S \\ 0 & \frac{1}{C} & -W_S & 0 \end{bmatrix} x + \begin{bmatrix} \frac{4}{\pi L}\sin\left(\frac{\pi}{2}D\right) & \frac{2V_{DC}}{L}\cos\left(\frac{\pi}{2}D\right) & I_C \\ 0 & 0 & -I_S \\ 0 & 0 & V_C \\ 0 & 0 & -V_S \end{bmatrix} \begin{bmatrix} \hat{v}_{DC} \\ \hat{d} \\ \hat{w}_S \end{bmatrix} \quad (4)$$

$$y = \begin{bmatrix} RI_S & RI_C & 0 & 0 \end{bmatrix} x \quad (5)$$

$$x = \begin{bmatrix} \hat{i}_S & \hat{i}_C & \hat{v}_S & \hat{v}_C \end{bmatrix}^T \quad (6)$$

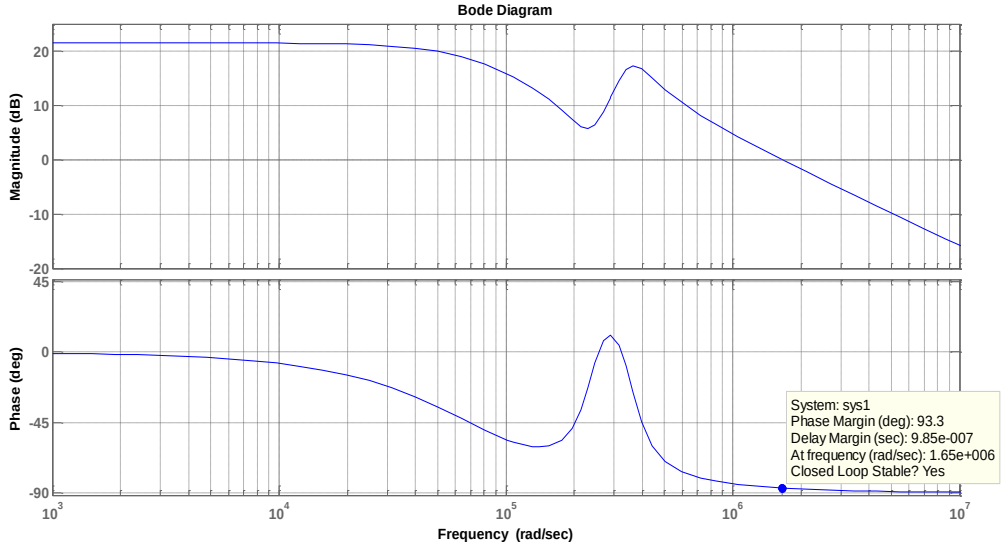
$$y = \hat{p}_O \quad (7)$$

Where, lower case letters with a sign of kappa (^) over them represent a small amplitude perturbation and the upper case letters represent corresponding values of the parameters at an arbitrary operating point. Meanings of other symbols have been described in Table-3.

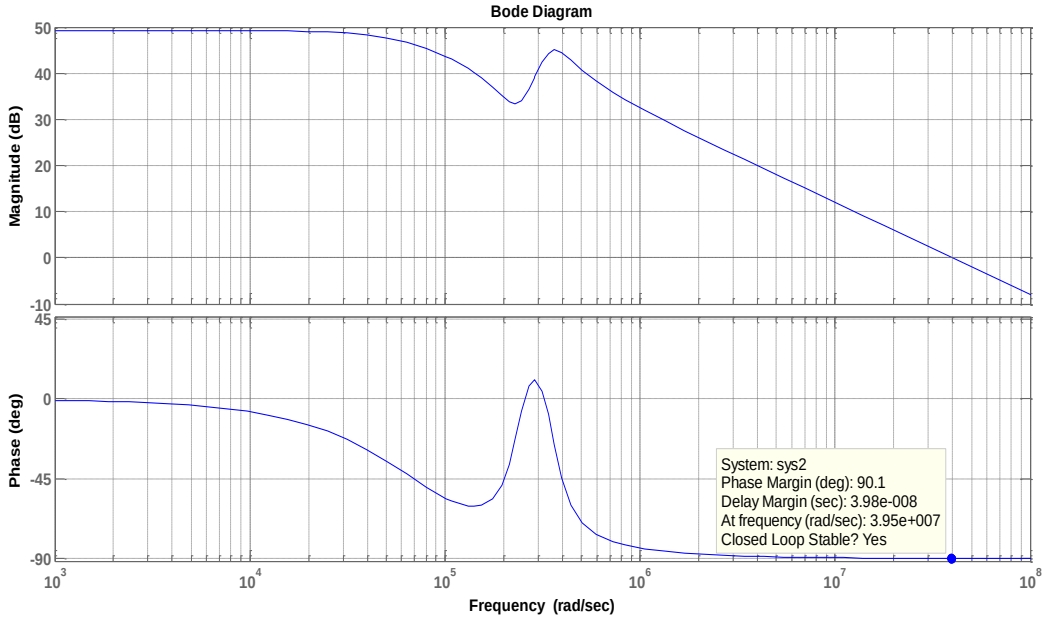
Table3 Description of symbols

Symbols	Description
i_c	Magnitude of cosine component of harmonically approximated output current
i_s	Magnitude of sine component of harmonically approximated output current
v_c	Magnitude of cosine component of harmonically approximated output voltage
v_s	Magnitude of sine component of harmonically approximated output voltage
d	Duty ratio of output voltage wave form
w_s	Switching frequency

From the derived model, it can be observed that P_o can be controlled by varying either of the three inputs viz. v_{DC}, w_S or d. Stability of the system is analyzed using Bode plot and it is seen that it is stable for all the three inputs as shown in Fig.3.



(a)



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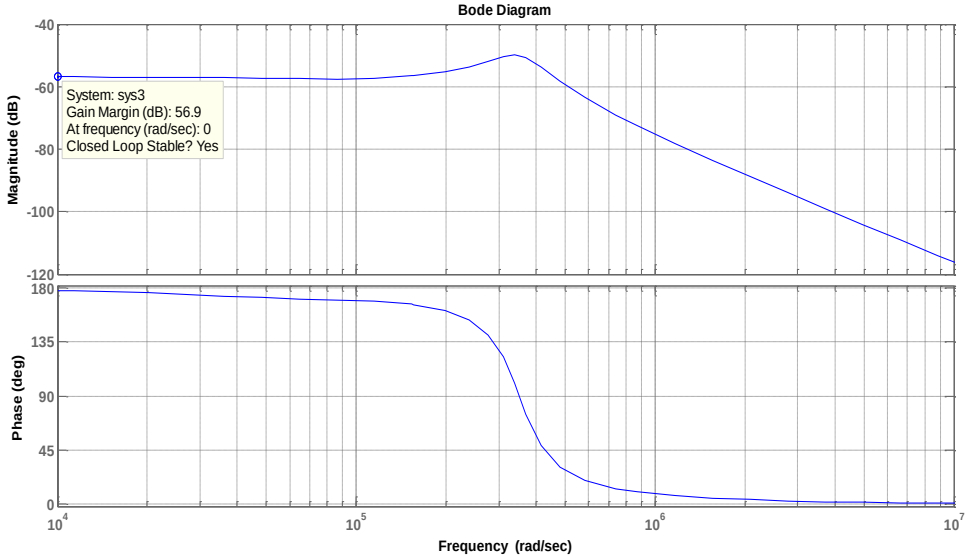

(c)

Fig 3 Bode plot (both magnitude and phase) for inputs (a) v_{DC}, (b) d and (c) w_S

4. CONTROL SCHEME AND OPERATION

4.1 Control Scheme

In present work, authors have used duty ratio control (of output voltage) using phase shift technique to control the output power. The switching pulses as shown in Fig.4 were applied to the four switches of the full bridge inverter shown in Fig.5.By controlling the phase shift between the pulses applied to *S1* and *S2*,RMS value of output voltage is controlled and hence the output power. Step input (reference value) of unit magnitude in Fig.1 corresponds to zero phase shift between the switching pulses (or *D=1*). As the magnitude of step is decreased to zero, the phase shift is gradually increased to *pi* and thus *D* is automatically reduced to zero.

4.2 Zero Voltage Switching (ZVS)

When a pair of *mosfets* (present in complementary arms) doesn't conduct simultaneously, then the load current completes its path via freewheeling diodes. These anti-parallel diodes conduct after the *mosfet's* output capacitance is discharged. During diode conduction period, the voltage across power *mosfet* is maintained to almost a negligible

value (equal to diode forward conduction voltage drop). It is the interval during which *mosfets* should be turned ON to achieve ZVS. If *D* is gradually decreased, maintaining the resonant frequency f_o, then ZVS will be lost at a certain value when the load current becomes positive before *S2* turns ON. This problem can be solved by increasing *f* so as to allow more negative load current to flow before *S2* turns ON, ensuring a full discharge of the *mosfet's* output capacitance. This can be easily implemented using microprocessor based firing circuit provided increment required in *f* is an integral multiple of the clock frequency applied to microprocessor.

In order to ensure ZVS at lower duty-ratio, the switching frequency is increased linearly in parallel (open loop control), according to (8).

$$f = f_0 + (1-D)\Delta f \qquad (8)$$

Here, f_0 is taken as 30 kHz and Δf as 3kHz; thus, the range of frequency variation is limited to 30 kHz to 33 kHz.

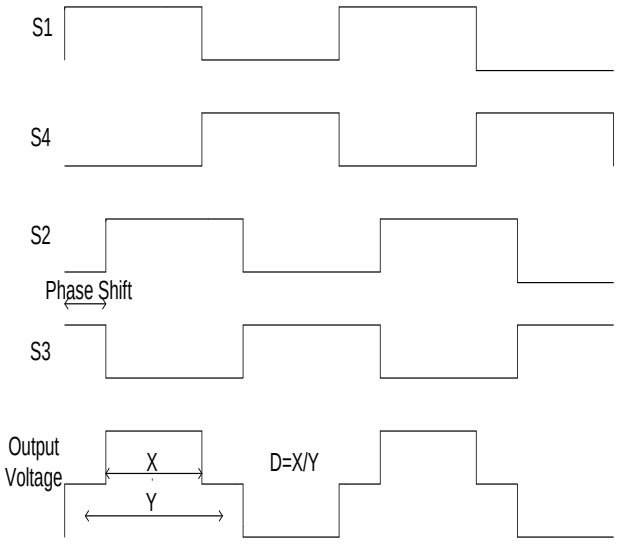

Fig 4 Switching pulses and output voltage

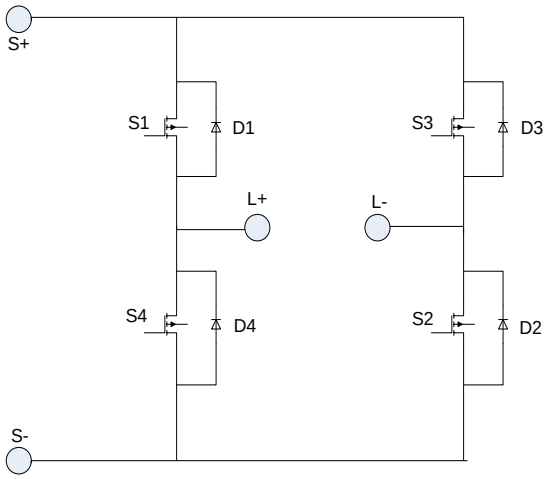

Fig 5 Full bridge inverter configuration

4.3 Operation & PID Controller design

A quasi square wave voltage pulse of peak to peak magnitude of 96V is generated between the output terminals *L+* and *L-*(as shown in Fig.8). Fig.6 shows the voltage and current across the switches (for an operating point corresponding to *D=0.7*). From the graph it is clear that ZVS is achieved in all the four switches.

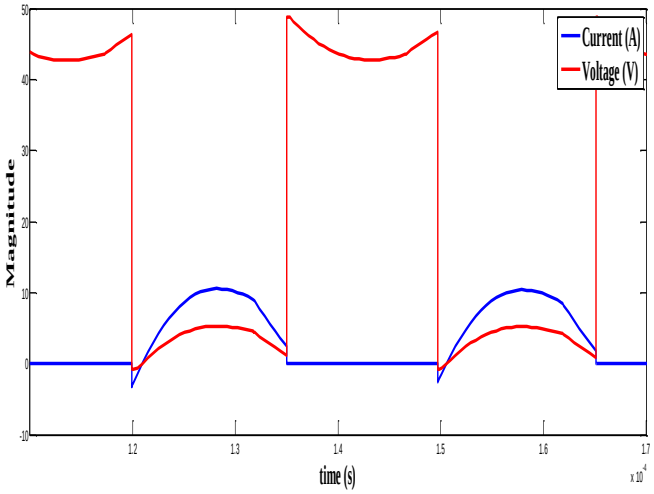

Fig 6 Voltage and current across switches (for D=0.7)

From Fig.7 and Fig.8, it can be observed that magnitude of both V_L and V_C is maximum at the same time (but with opposite polarity) which is obvious in a resonant circuit and the load current is maximum at the instant when the voltage across the capacitor is zero, which is quite expected. The maximum voltage stress developed across inductor during the course of operation is around 110V and across capacitor, it is around 62V.

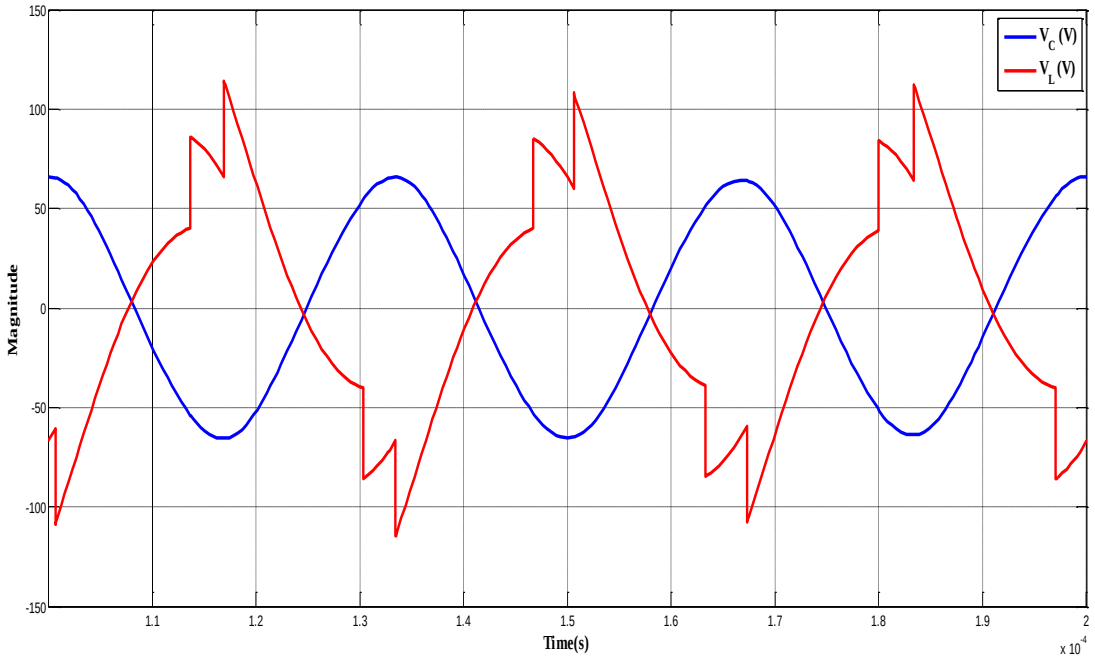

Fig 7 Voltage across capacitor (V_C) and inductor (V_L) for *D=0.8*

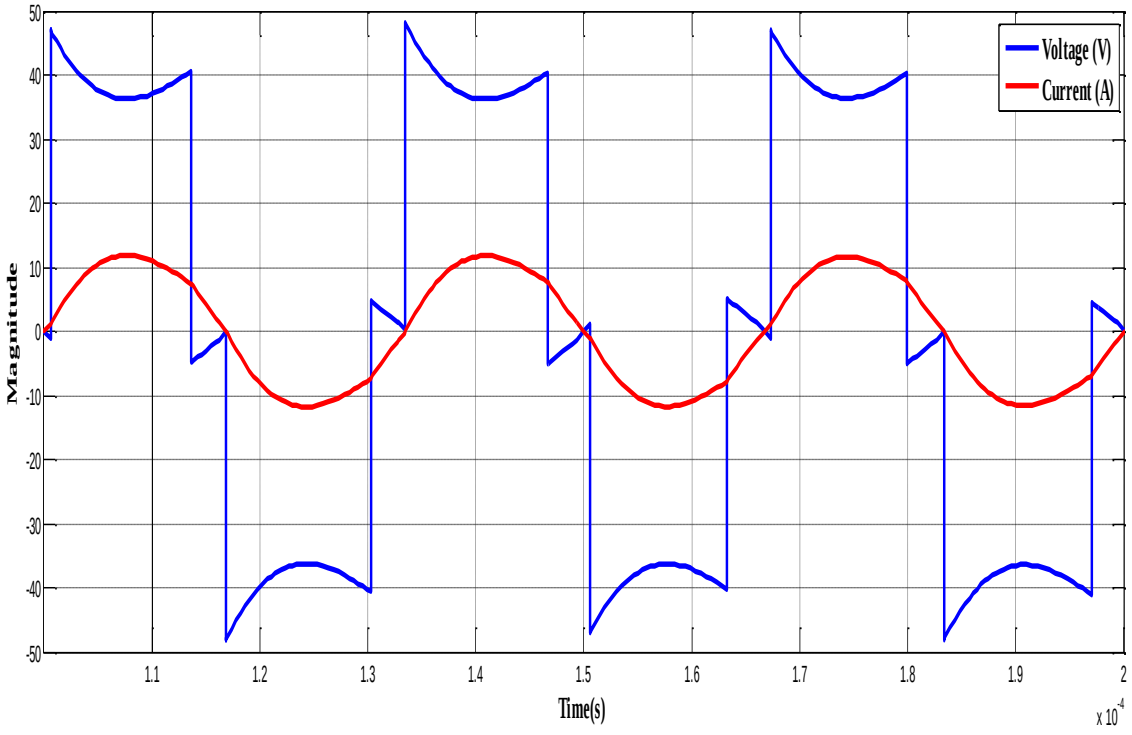

Fig 8 Output voltage and current (for D=0.8)

Fig.9 shows open loop response of the studied system with power as the output. The curve shows that the system has a settling time of around 0.02s under open loop condition. Using this open loop response, a PID controller for closed loop control system has been designed using *Ziegler Nichols* method [18]. The values of K_p, K_i and K_d are obtained as 4.99, 568.33 and 0.0109 respectively and some manual adjustment is made after that.

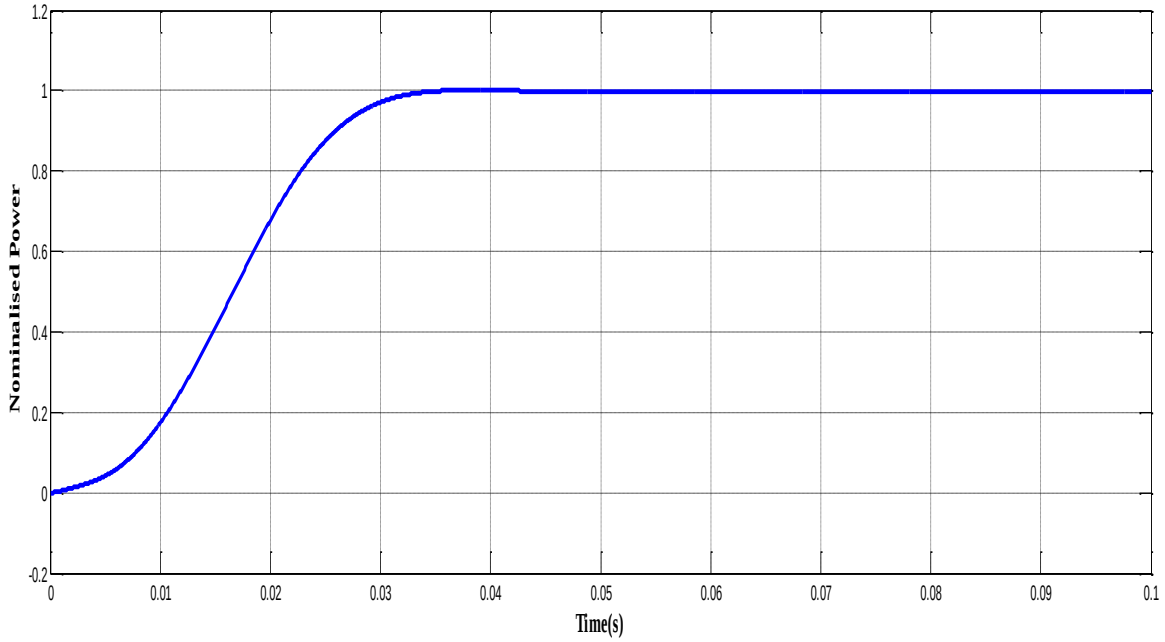

Fig 9 Open loop response of the studied system for a unit step input

5. RESULTS AND DISCUSSIONS

A system as shown in Fig.1 was developed in MATLAB/Simulink to study its performances and properties under different conditions. A reference is set for the output voltage and is compared with actual output voltage to generate error signal which excites the PID controller to produce manipulated phase shift which is fed to a pulse generator to generate appropriate switching pulses.

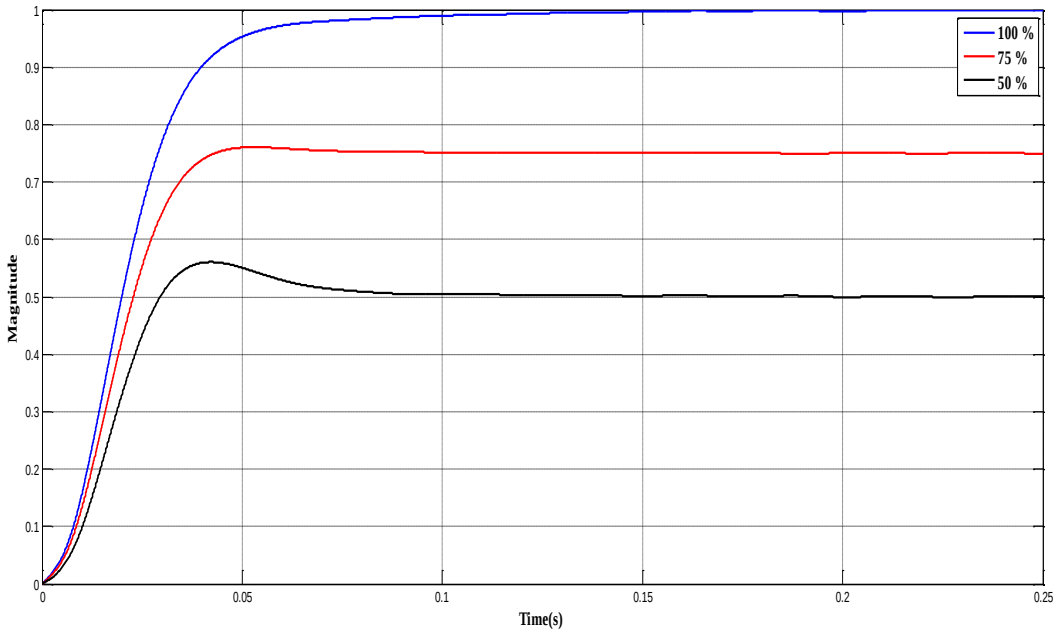

Figure 10 Response of close-loop system (with PID controller) for different reference values (step input)

Fig.10 shows the response of closed loop system with various step reference values. The settling time of the system is around 0.08s for a 3% band limit. However, overshoot of the system gradually increases for lower values of reference. Fig.11 shows the performance of PID controller as designed in *section 4.3* with intermittently changing reference from (75% to 100% of rated value). The curve is obtained with settling time of around 0.06s and 1.1s for 5% and 3% band limit respectively and justifies the performance and efficiency of designed PID controller.

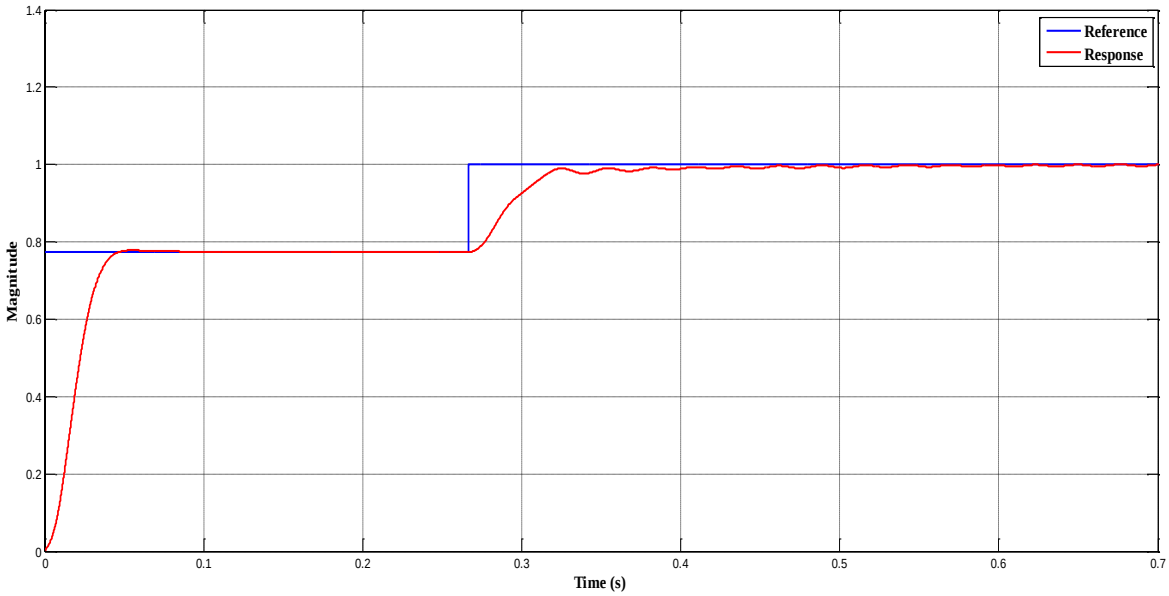

Fig 11 Response of closed loop system with intermittently changing reference from 75% to 100% of rated value

6. CONCLUSION

A close-loop power control of high frequency inverter for induction cooking has been analyzed in this paper. Although controller design is based on the linearized model of the system near operating point corresponding to *D=0.8*,yet simulation study shows that the controller works well to control output power in the range of 50% to 100% of rated value. The accuracy of the results obtained (in the specified range) justifies the validity of the proposed method and design.

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