AN EFFICIENT FPGA BASED SPACE VECTOR PULSE WIDTH MODULATION IMPLEMENTATION FOR SERVO CONTROL APPLICATION

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Abstract

This paper focuses on the design of a low power and high performance FPGA based Space Vector Pulse Width Modulation (SVPWM) controller for three phase implementation for Servo control Application. A new method is proposed to realize easy, accurate and high performance SVPWM technique based on FPGA with low resource consumption and reduced execution time than conventional methods. The FPGA based SVPWM generation involves a digital controller implementation to execute the algorithm and DQ reference generator gives reference vector signal to the controller. The controller in turn controls the PLL generator to generate pulse width modulated clock for three phases. The PLL generator is sourced by clock generator. Experimental results are presented for SVPWM architecture synthesized on standard low-cost FPGA chips, showing very good linearity and resolutions up to 1ns.

Keywords: *FPGA, PLL Generator, Space Vector Pulse Width Modulation (SVPWM)*

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1. INTRODUCTION

An analog signal has a continuously varying value, with infinite resolution in both time and magnitude. By controlling analog circuits digitally, system costs and power consumption can be drastically reduced. What is more, many microcontrollers and DSPs already include on-chip PWM controllers, making implementation easy. PWM is a way of digitally encoding analog signal levels. Digital control has obtained great research attention due to their advantages, such as low sensitivity, advanced control algorithms, reduced component count, ease of design and prototyping, etc. The advantage of these DPWMs is that they are very simple and obtain high linearity. However, their resolution cannot be very high, as the minimum time step is equal to the clock period of the counter. Furthermore, their power consumption is proportional to the clock frequency; so, trying to obtain a relatively high resolution results in high power consumption. In order to increase DPWMs' resolution, delay lines can be used.

This paper describes FPGA base SVPWM architecture, this involves digital controller implementation which will execute the algorithm. The SVPWM technique is very popular in three phase systems due to its performance benefits. There are many ways of Pulse width modulation schemes to obtain variable voltage and frequency supply. The widely used Pulse Width Modulation is Space Vector Pulse Width Modulation due to its due to its wide range of applications. SVPWM has low harmonic distortion, less hardware and low power consumption.

In this paper low cost Field Programmable Gate Array (FPGA) based design of SVPWM generation involves a digital controller implementation to execute the algorithm and DQ reference generator gives reference vector signal to the controller. The controller in turn controls the PLL generator to generate pulse width modulated clock for three phases. The PLL generator is sourced by clock generator.

2. EXISTING SYSTEM

The architecture of PLL-based DPWM is shown in Fig. 1. The PLL-based DPWM will generate fixed delays and it will avoid post fitting delay adjustments. The Digital controller in turns control the generator to generate pulse width modulated clock for phases. The Digital Pulse Width Modulation can manage the clock signals given by the PLLs. We can change the phases of clock signals and we can manage the frequencies and we can control them in a specified manner. The PLL can multiply the generated clock frequency from 25MHz to 250MHz. We can generate additional outputs P90, P180 and P270 with main output P0. The signals will generate high resolution of the DPWM, adding the other input bits provides adjustment of the duty cycle will reach 1ns resolution.

The variations in delay due to different paths inside the multiplex or may lead to non monotonic non linear behavior. To eliminate these effects calibration process will be used. The post-fitting simulation has to run for estimating the delay differences and the phase shifts at the PLL outputs are adjusted accordingly. The digital phase-locked loop (DPLL) has better controlling over the analog PLL, PID, fuzzy logic controller etc. and so it provides accurate speed control on

loading. DPLL is used in various fields such as communication fields, instrumentation and control fields etc. to escape the drawbacks such as the various types of noise like white noise, spur noise, damping factor, high frequency noise etc. get introducing with linear PLL, it has also poor stability of locking range of frequency so dumping occurs and less efficient for the higher frequencies. Digital PLL controls the speed of DC motors and provides wide locking range. The Digital PLL provides better synchronization for digital signals with help of phase frequency detector and loop filter.

Delay differences due to different paths inside the multiplexer may lead to non-monotonic and non-linear behavior. These undesired effects are eliminated by a calibrating procedure: a post-fitting simulation is run to estimate the delay differences and the phase shifts at the PLL outputs are adjusted accordingly. Special care must be taken to lock on-chip placement of the DPWM module resources after this calibration is completed. Otherwise the insertion of additional circuit elements can completely modify the placement of the circuit inside the chip and therefore also the timing and delays, leaving the previous calibration useless.

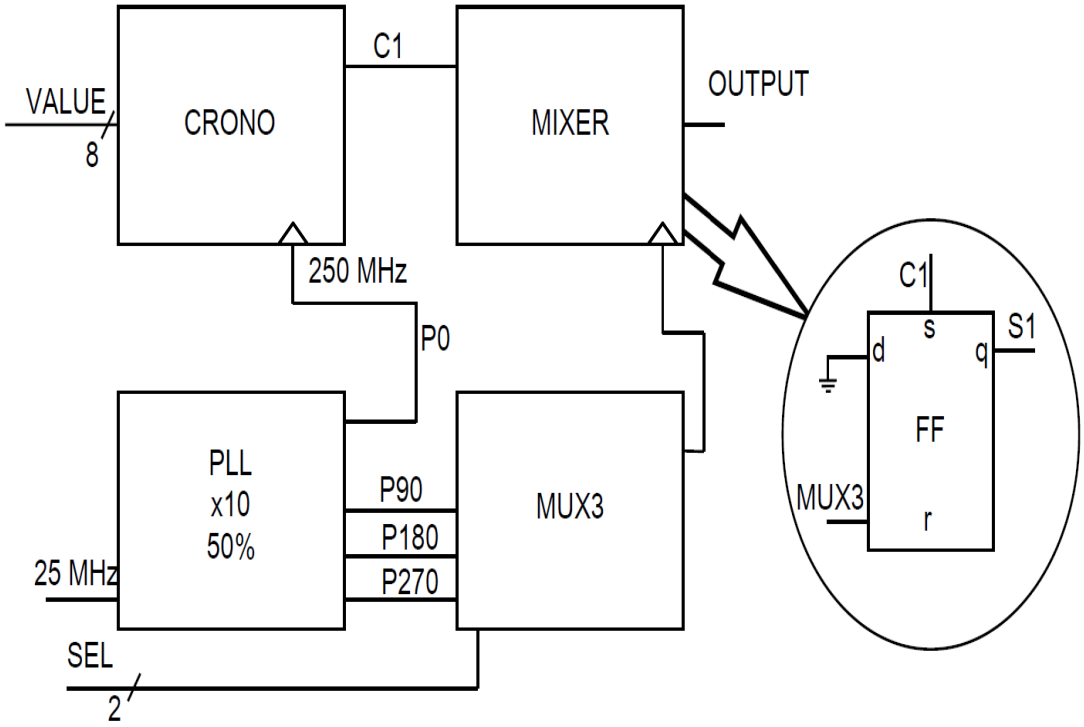


Fig. 1 Simplified diagram of the PLL-based DPWM architecture

3. PROPOSED SYSTEM

Pulse-width modulation (PWM), or pulse-duration modulation (PDM), is a technique used to encode a message into a pulsing signal. Space vector modulation (SVM) is an algorithm for the control of pulse width modulation (PWM).It is used for the creation of alternating current (AC) waveforms, most commonly to drive 3 phase AC powered motors at varying speeds from DC using multiple class-D amplifiers. There are various variations of SVM that result in different quality and computational requirements. The design of Efficient FPGA based Digital Space Vector Pulse Width Modulation controller for Servo control Application. The method involves SVPWM generation.

The FPGA based SVPWM generation involves a digital controller implementation to execute the algorithm and DQ reference generator gives reference vector signal to the controller. The controller in turn controls the PLL generator to generate pulse width modulated clock for three phases. The PLL generator is sourced by clock generator

The SVPWM technique offers significant performance benefits and has proved to be very popular in three-phase systems such as Servo Controllers, Power Converters and Robotics. The system is having many advantages such as SVPWM based control of power drives gives precision control, Low Harmonic Distortion compared to other PWM techniques and reduction of hardware etc.

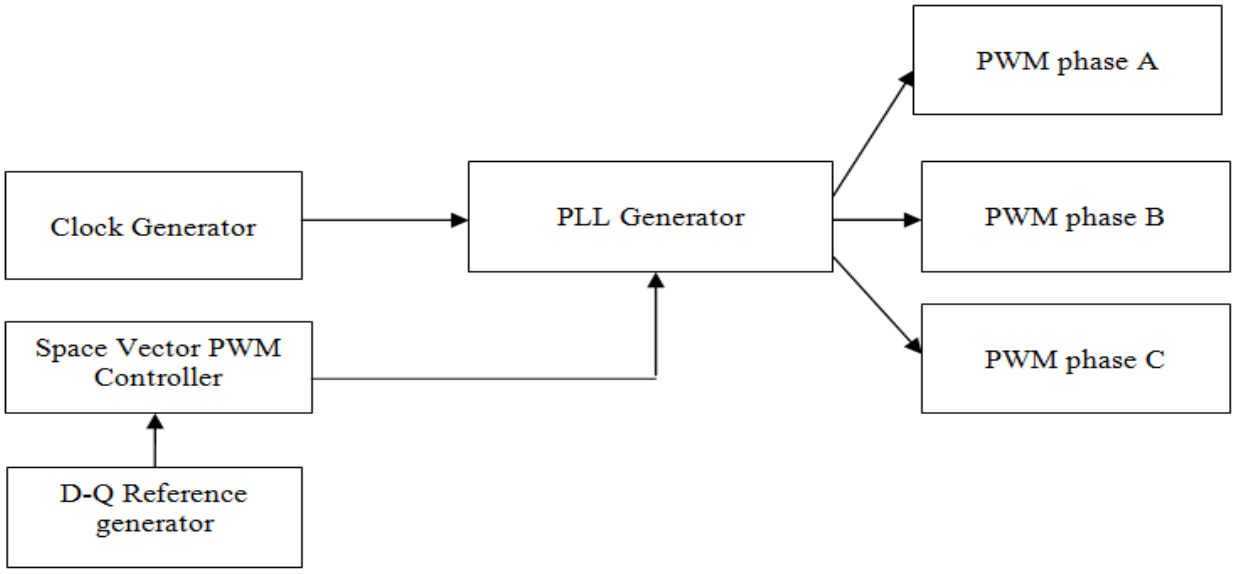
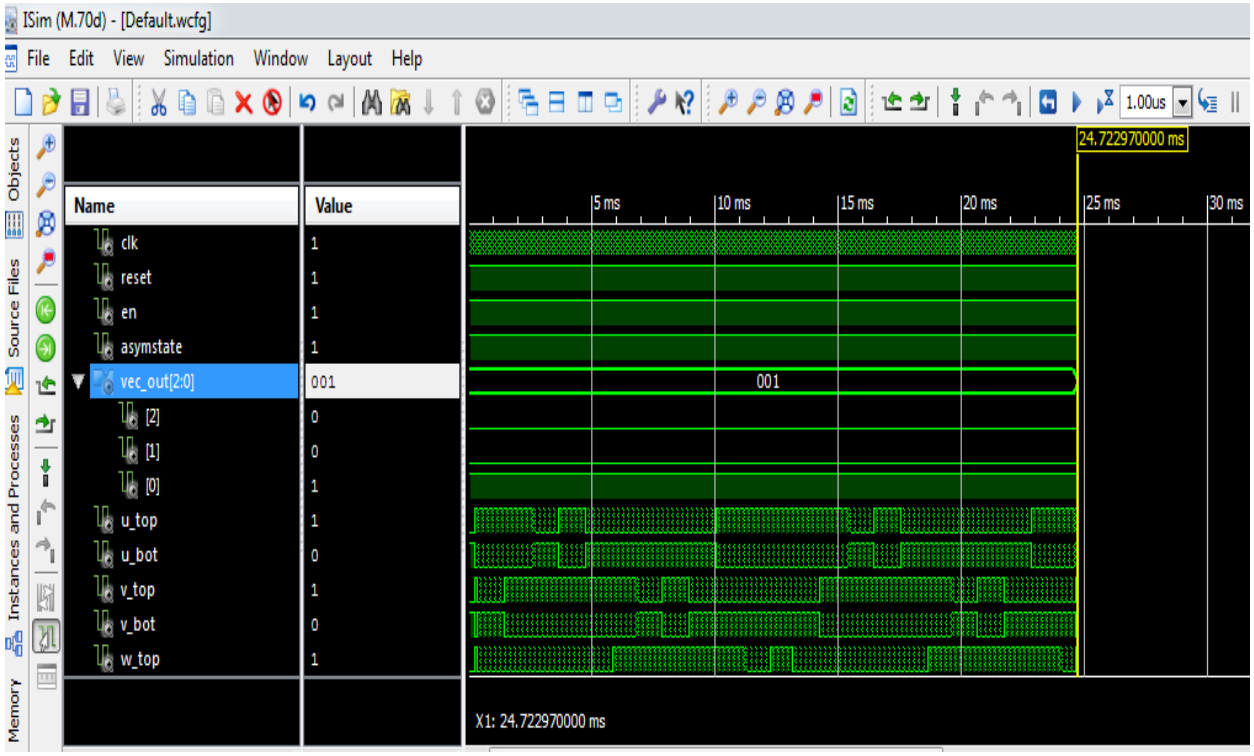


Fig 2: Block diagram for Efficient FPGA based Space vector pulse width modulation implementation for Servo control Application

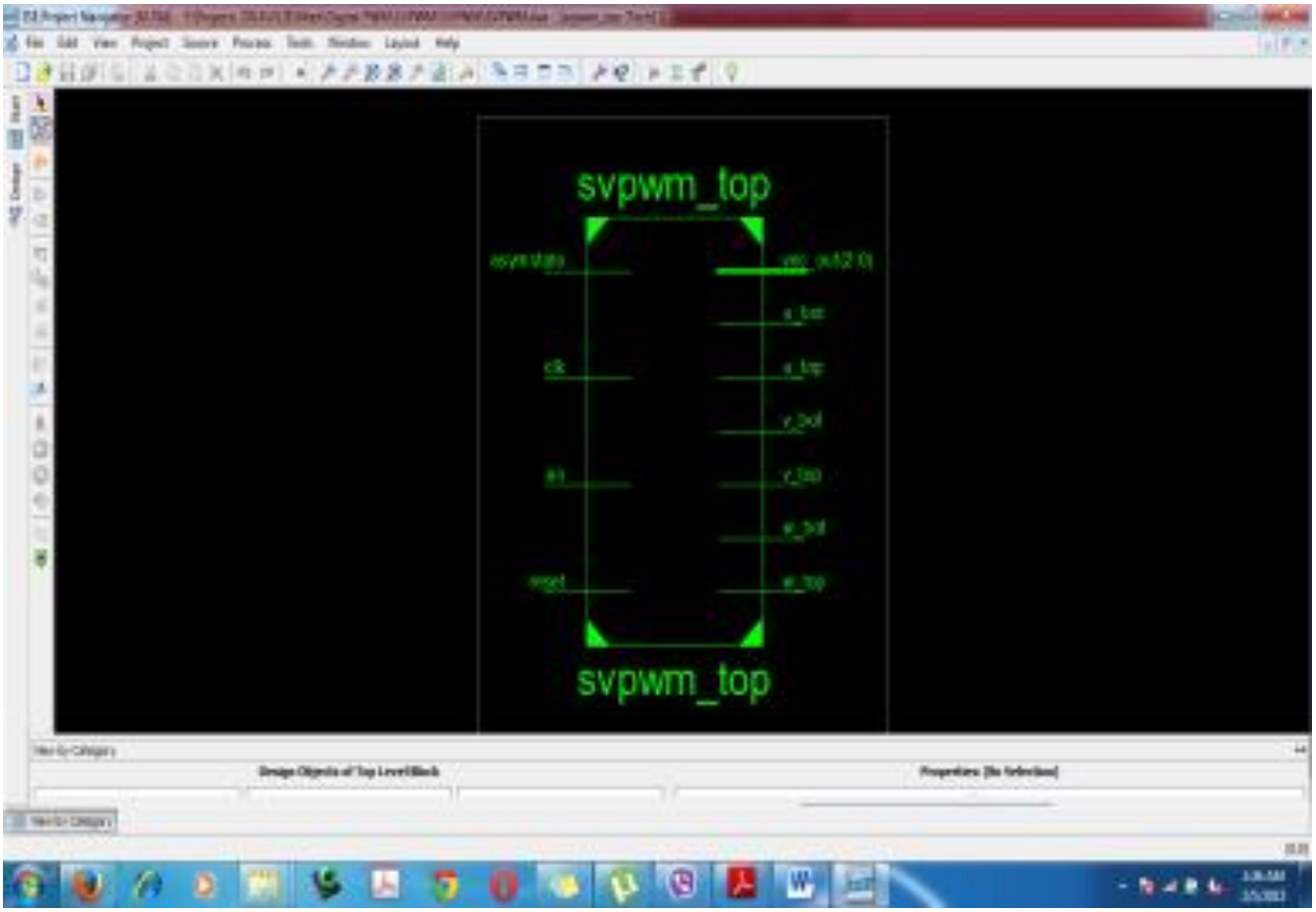
The FPGA based SVPWM generation involves a digital controller implementation to execute the algorithm and DQ reference generator gives reference vector signal to the controller. The controller in turn controls the PLL generator to generate pulse width modulated clock for three phases. The PLL generator is sourced by clock generator. The based SVPWM generation having following advantages

- SVPWM based control of power drives gives precision control.
- Low Harmonic Distortion compared to other PWM techniques.
- FPGA based SVPWM generation implies reduction of Hardware and can be implemented to generate dynamic control algorithm with less power consumption.

4. SIMULATION RESULTS



(a)



(b)

Fig 2 Simulation results (a) Simulation output (b) Space Vector Pulse Width Modulation

Above Figures shows the results of FPGA based Space Vector Pulse Width Modulation Simulation results as well as top module of Space Vector Pulse Width Modulation.

Timing Analysis Report

Data Sheet report:

All values displayed in nanoseconds (ns)

Setup/Hold to clock clk

Source	Max Setup to clk (edge)	Max Hold to clk (edge)	Internal Clock(s)	Phase
asymstate	0.283(R)	0.405(R)	clk_BUFGP	0.000
en	0.280(R)	0.545(R)	clk_BUFGP	0.000
reset	1.579(R)	0.545(R)	clk_BUFGP	0.000

Clock clk to Pad

Destination	clk (edge) to PAD	Internal Clock(s)	Phase
u_bot	6.216(R)	clk_BUFGP	0.000
u_top	6.216(R)	clk_BUFGP	0.000
v_bot	6.227(R)	clk_BUFGP	0.000
v_top	6.227(R)	clk_BUFGP	0.000
vec_out<0>	6.216(R)	clk_BUFGP	0.000
vec_out<1>	6.227(R)	clk_BUFGP	0.000
vec_out<2>	6.216(R)	clk_BUFGP	0.000
w_bot	6.216(R)	clk_BUFGP	0.000
w_top	6.216(R)	clk_BUFGP	0.000

Clock to Setup on destination clock clk

Source Clock	Src:Rise Dest:Rise	Src:Fall Dest:Rise	Src:Rise Dest:Fall	Src:Fall Dest:Fall
clk	9.097			

Analysis completed Thu Feb 05 01:42:49 2015

Trace Settings:

Trace Settings

Peak Memory Usage: 119 MB

5. CONCLUSION

FPGA based Space vector PWM implemented, which involves digital controller implementation. The digital controller executed the algorithm for reference vector signal to the controller. The PLL generator generated pulse width modulation clock for three phases. The SVPWM based method achieves a resolution of 1ns in the low-cost FPGA It is concluded that solution have good linearity and monotonicity properties.

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