A 2-STAGE DATA WORD PACKET COMMUNICATION DECODER USING RATE 1-BY-3 VITERBI DECODER AND PARITY GENERATOR

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Abstract

In the field of consumer electronics the high speed communication technology applications based on hardware and software control are playing a vital role in establishing the benchmarks for catering the operational requirements of the electronic hardware to fulfil the consumer requirements in wired and wireless communication. In the modern era of communication electronics decoding and encoding of any data(s) using high speed and low power features of FPGA devices [1] based on VLSI technology offers less area, hardware portability, data security, high speed network connectivity [2], data error removal capability, complex algorithm realization, etc. Viterbi decoder is a high rate decoder that is very commonly and effectively used method in modern communication hardware. It involves Trellis coded modulation (TCM) scheme for decoding the data. The viterbi decoder is an attempt to reduce the power, speed [1], and cost as compared to normal decoders for wired and wireless communication. The work in this paper proposes a improved data error identification probability design of Viterbi decoders for communication systems with a low power operational performance. The proposed design combines the error identification capability of the viterbi decoder with parity decoder to improve the probability of the overall system in identifying the error during the communication process. Among various functional blocks in the Viterbi decoder, both hardware complexity and decoding speed highly depends on the architecture of the Decoder. The operational blocks of viterbi decoder are combined with parity testing block to identify the error in the viterbi decoded data using parity bit. The present design proposes a multi-stage pipelined architecture of decoder. The former stage is the viterbi decoding stage and the later stage is the parity decoding stage for the identification of error in the communicated data. Any Odd number of errors occuring in the recovered data from the former decoding stage can be identified using the later decoding stage. A general solution to derive the communication using conventional viterbi decoder is also given in this paper. Implementation result of proposed design for a rate 1/3 convolutional code is compared with the conventional design. The design of proposed algorithm is simulated and synthesized successfully Xilinx ISE Tool [3] on Xilinx Spartan 3E FPGA.

Keywords: *ACS (Add-Compare-Select), Convolutional Code Rate, Error probability, FPGA, Low Power, Parity Encoder, Pipelining, Trace Back, Viterbi Decoder, Xilinx ISE.*

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1. INTRODUCTION

Typically, a TCM system employs a high-rate convolutional code that leads to a high complexity of the Viterbi decoder even for moderate constraint length of the convolutional code. A lot of work has already been proposed on Viterbi decoder. Use of rate-3/4 convolutional code is proposed for 4-D TCM system for deep space communications in [4]. Reduced-state sequence decoding (RSSD) method [5], M-algorithm [6] and T-algorithm [7, 8], Viterbi decoder based on over-scaling supply voltage [9], power efficiency in T-algorithm [10, 11] has been already proposed for speed and power based optimization of Viterbi decoder. General solutions for low-power VD design have already been well studied by existing work. T-algorithm is more commonly used than M-algorithm in practical applications. In the M-algorithm a sorting process is used in a feedback loop while in T-algorithm the optimal path matric search is performed. Searching for the optimal PM in the feedback loop still reduces the decoding speed. A Gate Diffusion Input circuits for asynchronous design is proposed in [12], Viterbi decoder based on modified register-exchange method [13], a scheme based on Verilog language for the implementation of high-speed and low power consumption bi-directional Viterbi decoder [14], various logic styles (CMOS, Pseudo NMOS and Dynamic logic) based design of circuits at ACS level [15], Gate Diffusion Input Logic (GDIL) based implementation [16], etc. are also proposed designs to improve speed of Viterbi decoder. A high-rate convolutional code suffers from a severe degradation of bit-error-rate (BER) performance due to inherent drifting error between the estimated the accurate path matric and the optimal path matric. The computational overhead and decoding latency of the data decoding system are to be taken into consideration along with the other performance criteria to meet the required performance of the decoding system. In this work, we analyzed the conventional Viterbi decoder algorithm and the proposed Viterbi decoder design algorithm for a rate 1/3 code. The proposed method is based on the performance of Viterbi Decoder in line with Parity Decoder to improve the data error identification probability. The block diagram of proposed encoder and decoder are shown in Fig-1 and Fig-2

respectively. The remainder of this paper is organized as follows. Section-2 gives the background information of Viterbi Decoder and its Operational Flow. Section-3 presents the proposed design architecture and its operational flow. Section-4 gives the simulation and synthesis results and conclusion is provided in Section-5.

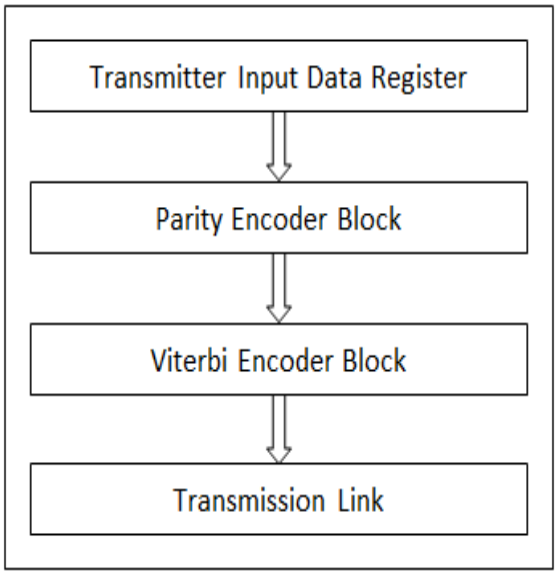

Fig -1: Block Diagram of Proposed Encoder

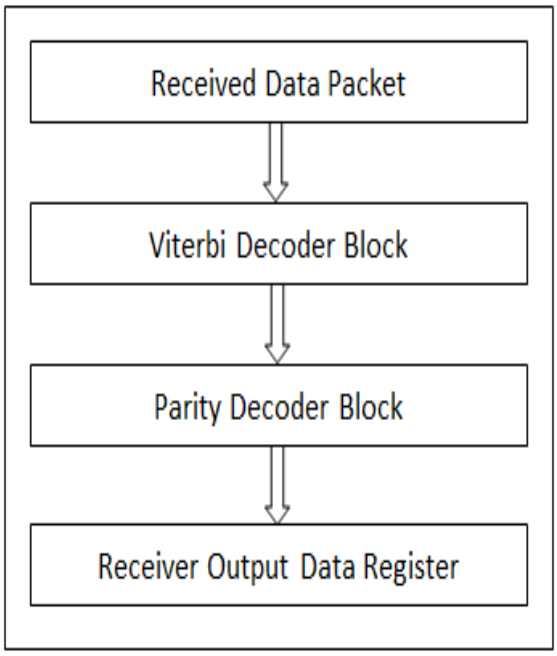

Fig -2: Block Diagram of Proposed Decoder

2. CONVENTIONAL VITERBI DECODER

In a convolutional encoder the output is a function of the current state of the encoder and the current input. The hardware circuit of a convolutional encoder is generally realized using one or more shift registers and logic gates. Among logic gates, XOR gate is most commonly used in circuit realization. An empirical approach is used to determine the interconnections of the registers and logic gates. The hardware interconnection and the number of memory elements determines the minimum Hamming distance which further determines the maximum number of error bits that can be corrected using the decoder. The conversion rate of a convolutional encoder is specified as the ratio of number of input bit(s) to the number of encoded output bit(s), i.e., for a decoder with 'm' number of input bits and 'n' number of corresponding encoded bits then it is called a rate "m/n" encoder. A simple block diagram of Viterbi Encoder is shown in Fig-3.

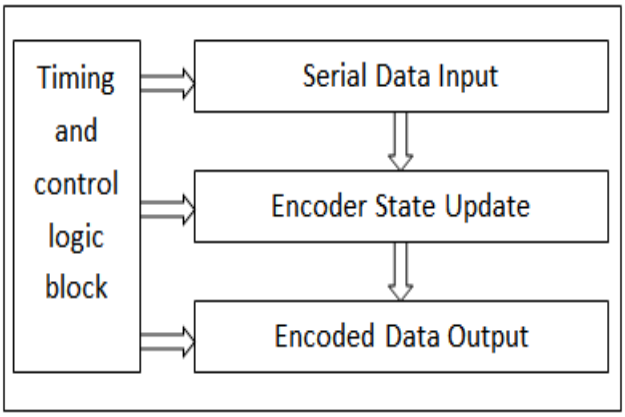

Fig -3: Simple Block Diagram of Viterbi Encoder

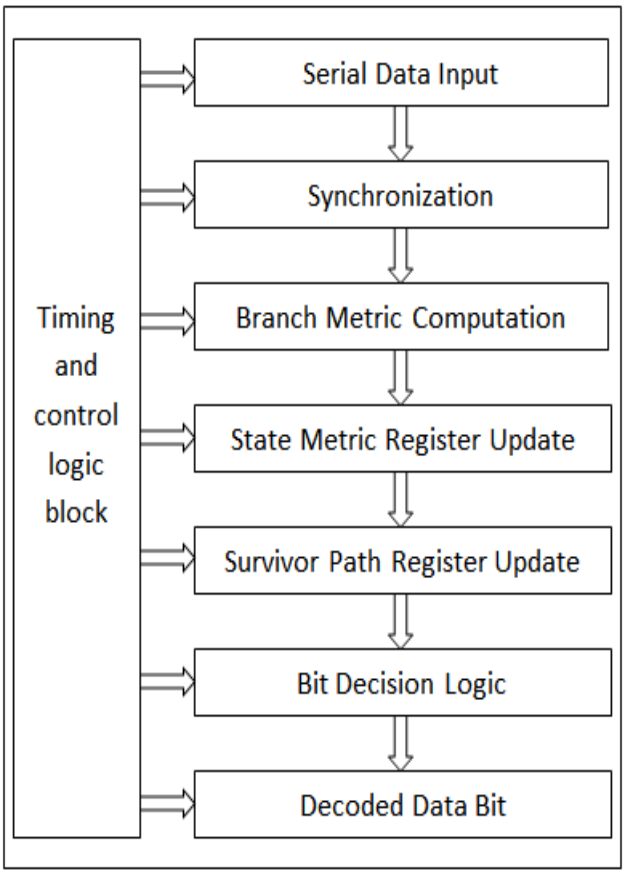

Fig -4: Simple Block Diagram of Viterbi Decoder

In a Viterbi decoder, the serially received bits are first synchronized by identifying the start and end of the data packet as well as the boundaries of the received symbols. The synchronized encoded symbol bits are then processed

for computing branch metric. A branch metric represents the Hamming distance between the estimated actual bit code symbol and its corresponding received code symbol. The branch metric accumulated along a path is called a "path metric" and a path matric at a state of computation from the initial computation state is called a "state metric". Branch metric and state metric values are updated in registers at every state of computation. When the trellis of a received symbol packet is complete, the trace back method is applied to retrieve the actual data bits from the computed data. When tracing the data, decision hardware is used to select the path with a smaller path metric value. When the trace back is complete, the data bits along the trace back path are selected as the decoded data bits. A simple block diagram of General Viterbi Decoder is shown in Fig-4.

3. PROPOSED VITERBI ENCODER AND DECODER

In the present work the Error detection and correction capability is used with the single bit error identification capability of parity encoder. From the data to be communicated, a parity bit is appended to every 7-bit to make parity encoded bytes of the information data. This is the first level of encoding of the information data. Two bytes of these parity encoded bytes are combined to make an encoded word. This word is appended two logic '0' bits, i.e., "00", as reset bits. This enables the trellis into the initial state. The first level encoded information thus consists of 18-bits. This is the first level encoded data packet. This first level encoded packet is further encoded using Viterbi encoder. This encoding is the second level encoding of the information data.

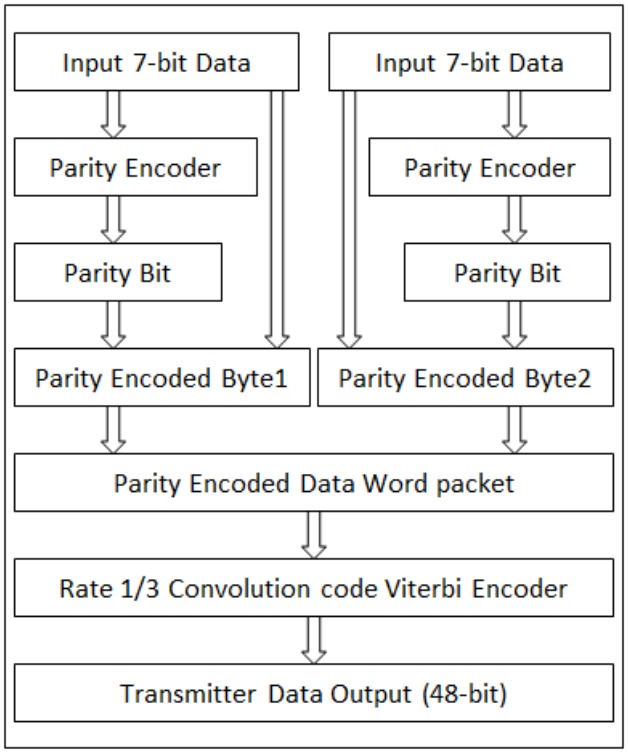

Fig -5: Block Flow Diagram of Proposed Encoder

The encoding steps are shown using block flow diagram in Fig-5. In the present work a rate 1/3 encoder is used for the synthesis and simulation of proposed design. Finally, the two-stage encoded bits are transmitted through the wired or wireless link.

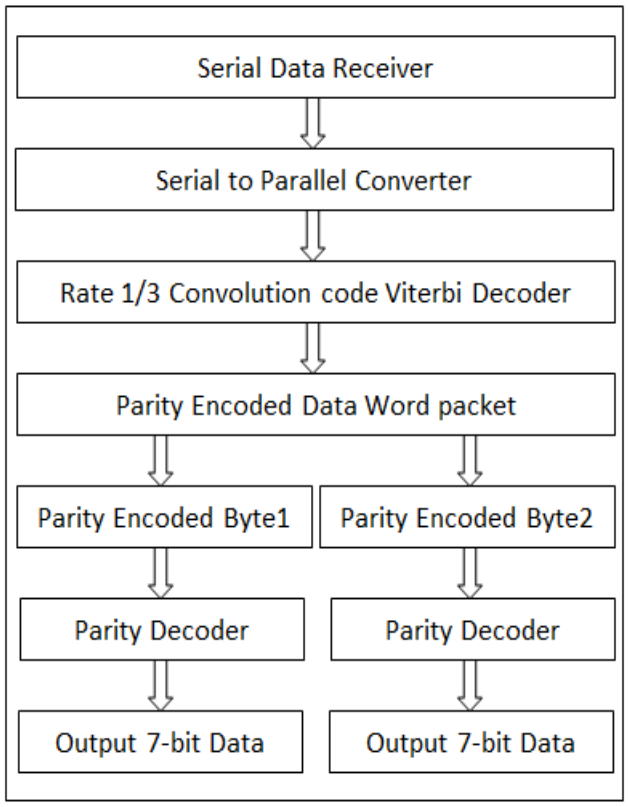

Fig -6: Block Flow Diagram of Proposed Decoder

In the proposed Decoder, an operation just reverse to that of encoder is performed by the hardware to recover the actual data. The operation of the proposed decoder is shown using block flow diagram in Fig-6. The parity encoded word is first recovered using Viterbi Decoder in the first stage of decoding. This decoding stage will overcome any error due to single bit change in the transmission path. But in some cases of multiple bit errors in the transmission path, data with error is recovered by this decoding stage. The received bits are further checked for bit error at byte level to authenticate the absence of the above mentioned multiple bit-error that lead to same result.

4. SIMULATION AND RESULT

The proposed design is simulated using Xilinx Tool on Xilinx Spartan-3E and Virtex-6 FPGA Devices. The waveform results of the functional Simulation of the proposed Encoder design is shown in Fig-7.

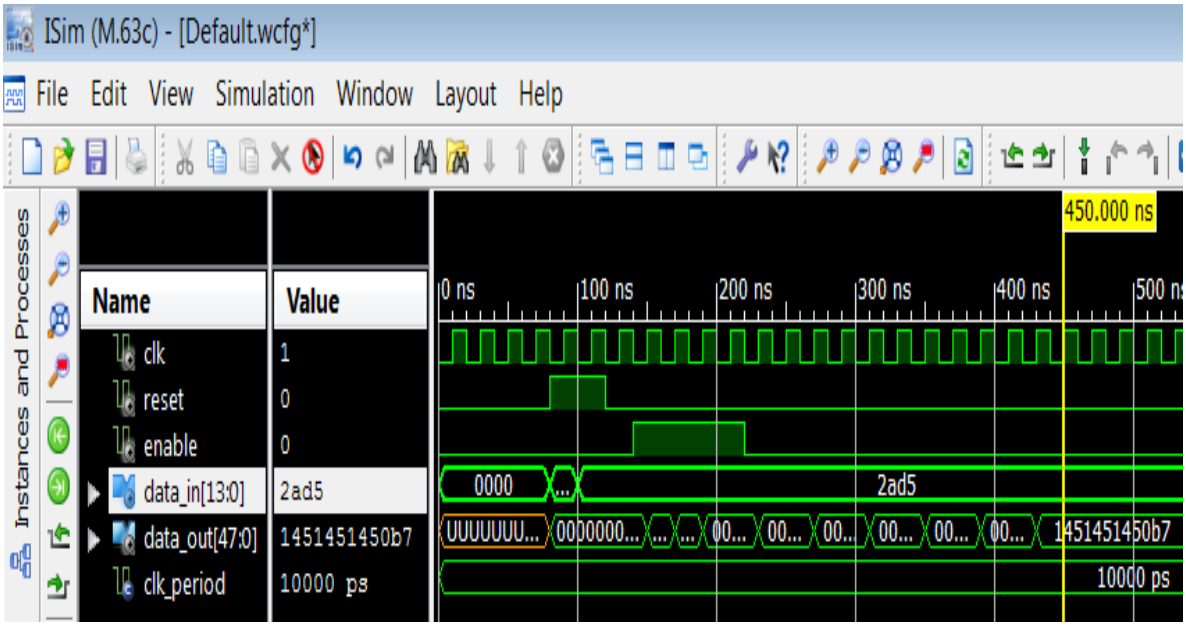

Fig -7: Simulation Waveform Diagram of Proposed Encoder

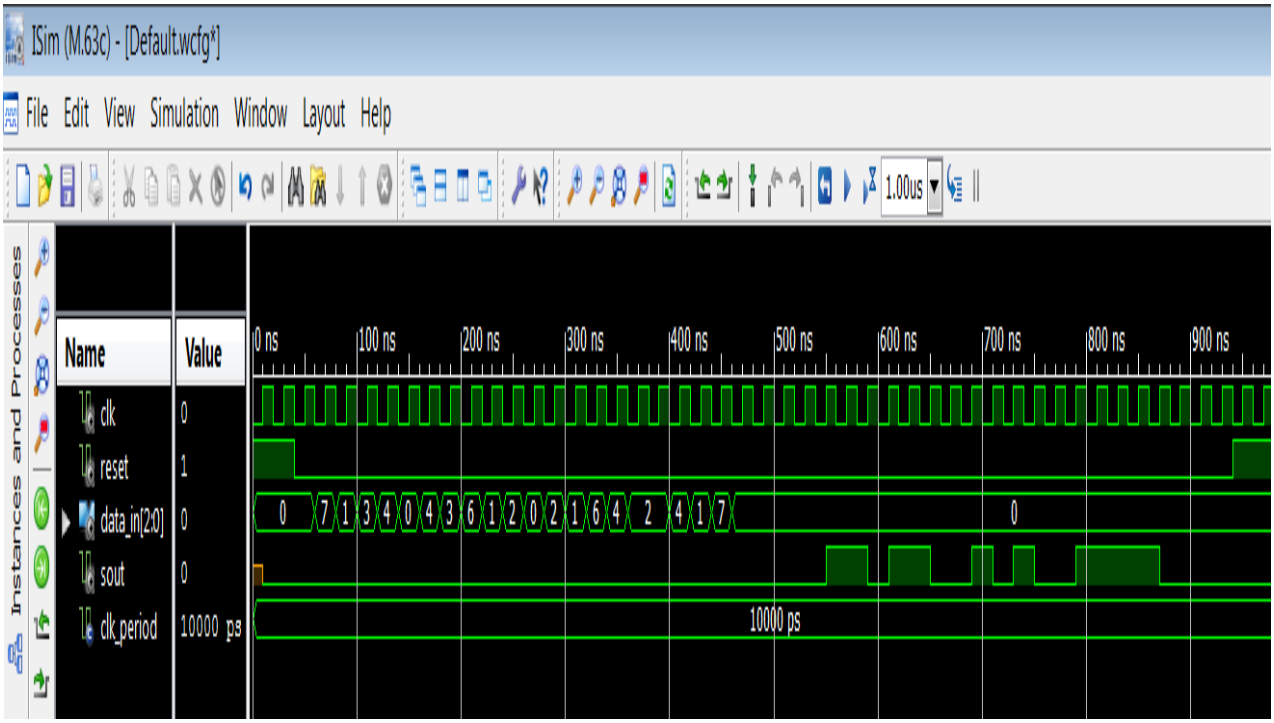

Fig -8: Simulation Waveform Diagram of Proposed Decoder without error in the transmitted encoder output

In the presented simulation results of the proposed the two 7-bit input data sets that are used to encode are:

Input 7-bit set-I – 1010101
Input 7-bit set-I – 1010101

After first stage parity encoding, the data bytes generated by the proposed encoder are respectively:

Input 7-bit set-I – 01010101
Input 7-bit set-I – 01010101

The Viterbi encoded output generated by the encoder with octal encoding is:

Encoder Output – 71340436120216422417

Error introduced Receiver input with octal encoding at octal coded symbol at 8th position is:

Receiver Input (without error) – 71340436120216422417
Receiver Input (with error) – 7134043'4'120216422417

The simulation output of proposed decoder without any error introduction in the encoded data bits is shown in Fig-8 and the simulation output of proposed decoder with 1-bit error correction is shown in Fig-9.

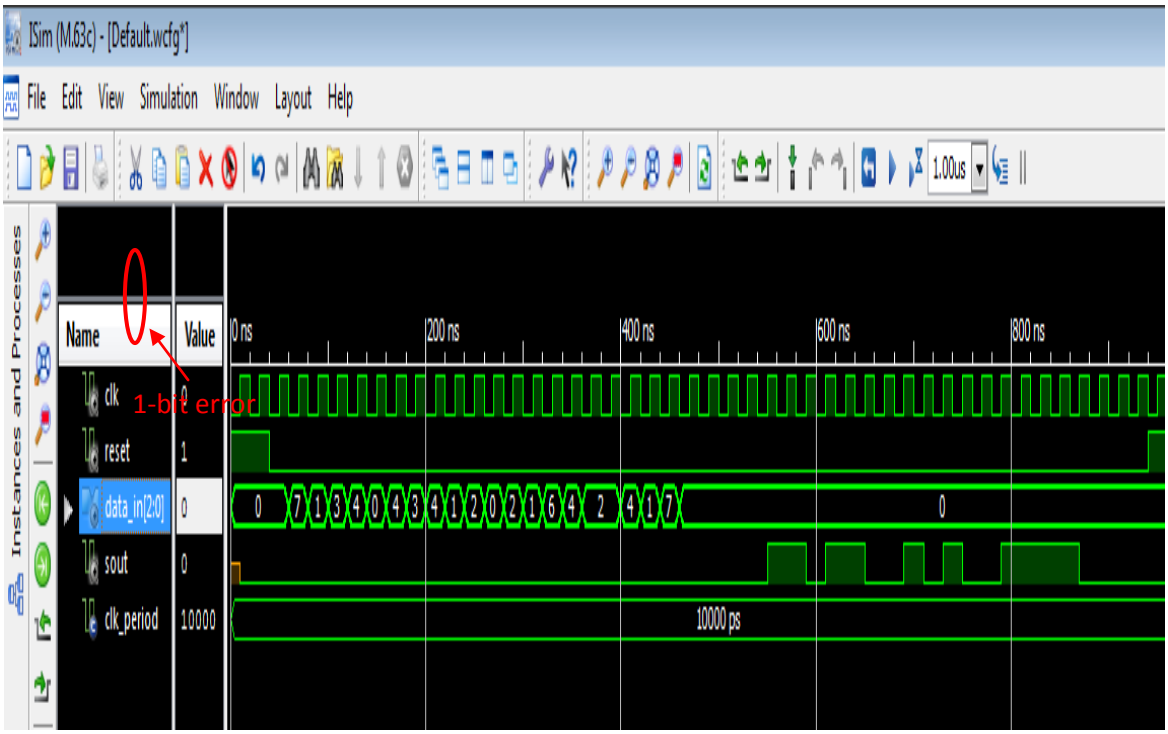

Fig -9: Simulation Waveform Diagram of Proposed Decoder with one-bit error corrected output

The comparison of the proposed design with the conventional design [17] is shown in Table-1 and the Hardware Utilization summary is presented in Table-2.

Table -1: Dynamic Power Consumption Comparison of Conventional Design with the proposed Design

	Proposed Design		Ref. [17] Conventional-T Viterbi Decoder	Ref. [17] Full Trellis Viterbi Decoder
Device	Virtex-6 XC6VLX75T-1FF484	Spartan-3E XC3S500E-4PQ208	TSMC 90-nm CMOS standard cell	TSMC 90-nm CMOS standard cell
Frequency (MHz)	500	500	232	505
Power (mW)	41	82	21.473	21.473
Multi-bit error	Odd Bits	Odd Bits	--	--

Table -2: Design Hardware Utilization

Virtex-6 XC6VLX75 T-1FF484	**Total**	**Encoder**		**Decoder**	
		Used	**%**	**Used**	**%**
Slices Reg	93120	241	0	364	0
LUTs	46560	462	0	457	0
LUT-FF Pair	517	186	35	164	24

a) Device Virtex-6 XC6VLX75T-1FF484

Spartan-3E XC3S500E-4PQ208	**Total**	**Encoder**		**Decoder**	
		Used	**%**	**Used**	**%**
Slices	4656	118	2	412	8
Flipflops	9312	105	1	362	3
LUTs	9312	205	2	610	6

b) Device Spartan-3E XC3S500E-4PQ208

5. CONCLUSION

A Viterbi Decoder is the most effective algorithm to identify single bit error during communication and also to recover the actual data from a single-bit error affected data. The proposed design is an attempt to improve the multiple bit error identification using a parity decoder. The proposed

design introduces only redundant bit overhead over the conventional method but effectively allows the proposed design to identify any odd number of bit changes in the data that is recovered from conventional design. The proposed method offers a simple hardware overhead over the conventional hardware circuit. The proposed concept can be effectively introduced with large data packets to reduce the overhead bit redundancy while maintaining the same improvement in the error identification.

ACKNOWLEDGEMENTS

The authors wish to convey special thanks to Mrs. Rita Jain (HOD, Department of Electronics and Communication Engineering, Laxmi Narain College of Technology, Bhopal, India) and Piyush Jain (Director Innovative Technology Design and Training Centre, Bhopal, India) for sharing ideas in line with the proposed work.

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