A 15 BIT THIRD ORDER POWER OPTIMIZED CONTINUOUS TIME SIGMA DELTA MODULATOR FOR AUDIO APPLICATIONS

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Abstract

Analog to Digital converters find a lot of usage in various receiver design architectures. Analog modules are found to be precise and quite resistant to various sources of noise and interference. Most of the highly accurate A/D converters involve the use of sigma-delta modulation which is associated with oversampling and noise shaping. The converters which make use of this modulation technique, find a high usage in applications which have the ability to tolerate offset and gain errors.The design of a 15 bit third order power optimized continuous time ∑-Δ modulator has been presented in this paper. This modulator operates with 1.8 V supply and has been implemented using cadence 180nm technology. In this paper, the individual blocks of the modulator have been designed. Instead of the conventional comparator, a clamped push pull type comparator has been used which can drive large capacitive loads.

Keywords: *A to D converter, Clamped push-pull comparator, Noise shaping, Offset error, Oversampling, Sigma Delta modulation*

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1. INTRODUCTION

The rapid growth of high speed wired and wireless communication systems has increased the need of highly powerful and efficient digital signal processing modules. They find a wider use in the field of communication, signal processing and several multimedia applications. This has developed the need for high resolution and power efficient analog and digital interfaces in audio applications. Hence, for such applications, oversampling technologies have become indispensible. As the scaling progresses, oversampled converters can reduce chip area and power consumption significantly unlike the conventional converters which are sampled at nyquist sampling rate. Sigma-Delta modulator increases the oversampling ratio and suppresses the aliased and out-of-band noise arising in many analog to digital converters. The major disadvantage of a one bit sigma delta modulator is that it shows reduced signal to noise ratio when a certain signal is given to it as an input. So, to avoid this problem, multi bit sigma delta modulator is used. In addition, use of higher order sigma delta modulators reduces the sampling rate and power consumption as the noise shaping filter order is increased which is an added advantage in the analog to digital converter design. The converters are broadly classified into two categories based on their sampling frequency. They are conventional Nyquist rate converters and Oversampling converters. The Oversampling converters have a sampling frequency greater than twice the bandwidth and are normally used for lower bandwidth operations such as audio and instrumentation. The resolution offered by them is significantly high when it undergoes proper noise shaping and the noise is pushed out of the signal band. As a consequence, the SNR improves.

The recent advances in VLSI technology has opened a wider scope for precise and optimized implementation of digital logic on a single silicon chip which is also known as system-on-chip design and this has played a significant role in pushing many types of signal processing operations to the digital domain. One of the applications of this phenomenon is the Sigma Delta analog to digital converter[1], in which the requirement of complex analog circuitry has been compensated by the use of certain dedicated signal processing techniques[2]. Different architectures of sigma delta analog to digital converters have been discussed in literature which has been implemented by using single order or multi order modulator stages. The two standard processes needed to convert analog signals to digital signals are sampling and quantization. In signal processing, sampling is the process by which a continuous signal is converted to a discrete signal. This conversion is performed at nyquist rate i.e. at $f_s=2f_m$ where f_s is the sampling rate and f_m is the bandwidth of the band limited function. This is followed by quantization where a larger set of input values is mapped to a smaller set. In other words, a quantizer normally converts continuous amplitude to discrete amplitude. The quantizer is a non linear device which introduces a quantization noise. The Signal to Quantization Noise ratio of Sigma Delta ADC for an 'n' bit quantizer with any test input is given by

$$SQNR= 6.02n + 1.76 \quad (1)$$

In order to reduce the effect of quantization noise, the signals are sampled as closely as possible. Practically, the signals are sampled at a rate greater than the nyquist rate i.e. fs>>2fm and the oversampling rate is given by $f_s/2f_m$. This value is found to be quite suitable for audio and wireless applications. Although oversampling increases the ADC cost and creates set up and hold time issues, it is preferred

because of its added advantage of higher ADC data rate and ability to capture high speed data. The SQNR is found to improve by a greatly after oversampling and is given by

$$SQNR = 6.02n + 10 \log (OSR) + 1.76 \quad (2)$$

The value of SQNR further improves with the increase in the order of the modulator which in turn helps in the achievement of a desirable cut-off value[3]. The effect of noise shaping is clearly indicated in the equation shown below. In the equation 'l' stands for the order of the filter

$$SQNR=6.02n + 10(2l+1) \log (OSR) + 1.76 \quad (3)$$

As can be seen from the equations, oversampling analog to digital converters based on sigma delta modulation offer high precision without the need of excessive component matching at the cost of speed. A simple sigma-delta ADC comprises of a summing amplifier, an integrator, a comparator and a 1 bit DAC. The output of the modulator is fed to a digital filter.

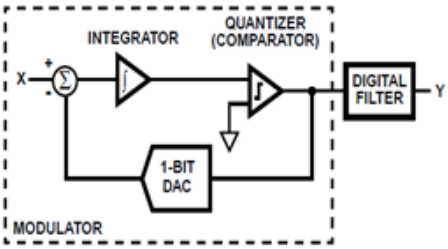

Fig -1: Block diagram of a Sigma Delta Modulator

The paper is organized into several sections as follows. Section 2 throws light on the available literature on Sigma Delta ADCs. Section 3 highlights the design approach and in section 4 the modulator design, implementation and results have been discussed. The conclusion has been given in section 5.

2. LITERATURE REVIEW ON SIGMA-DELTA ADCs

Several researches have been conducted on the Sigma-Delta ADCs till date. Some of the literature surveys done are summarized as follows:

2.1 ΣΔ ADC Design using Continuous Loop Filter

In the year 2003, F. Gerfers et al. presented the various design methodologies, implementation strategies of a power optimized third order low pass sigma delta ADC using a continuous time loop filter. The influence of a lower supply voltage on the functioning of the overall sigma delta modulator was analyzed. The ADC so designed was implemented in 0.5 μm CMOS technology using a supply voltage of 3.3 V. Analysis of the low power continuous time sigma delta ADC showed a DR of 80 dB and peak SNDR of 70 dB when in a bandwidth of 25 kHz. The power consumed was found to be 135μW from a 1.5V power supply.

2.2 Multi-bit ΣΔ ADC for Voice Coding

In the year 2006, L.Dorrer et al. proposed a 2nd order continuous time multi bit sigma delta ADC used for voice coding. The design was implemented in 65nm CMOS technology. The dynamic range was found to be 95 dB when made to operate over a bandwidth of 20Hz to 20KHz. Further, the need for anti-alias filtering is eliminated due to the feedback architecture used. The ADC used a 1.2 V supply and operated at 12MHz.

2.3 Low Power Continuous Time ΔΣ Modulators

In the year 2008, Shanthi Pavan et al. presented design specifications for low power Continuous Time modulators. The converter was designed using 180 nm CMOS process. The dynamic range achieved was found to be 93.5 dB. It operated at 1.8V power supply over a bandwidth of 24 KHz.

2.4 Low Latency ΣΔ ADC

In the year 2012, Shanthi Pavan et al. proposed a method of minimizing the order of noise shaping by a factor of 1. This method resulted in a continuous time analog to digital converter which had a higher sampling rate as compared to the previous existing designs. The design consumed a power of 47.6 mW. The bandwidth was obtained to be 16 MHz. It was implemented using a 180nm CMOS process.

3. DESIGN APPROACH

As shown in figure 1, the input signal from the previous stage is fed into the summing amplifier. The DAC output is fed back to the summer. The signal so obtained is integrated at a later stage. The integrator output is converted to a 1 bit digital output by the comparator. The output so obtained is fed as the input to the DAC. The output of the DAC is then subtracted from the incoming signal. The output from the sigma delta modulator is a digital data stream which consists of ones and zeros only. This data stream is then fed to a decimation filter to result in a binary output[1,4,5].

4. IMPLEMENTATION AND RESULTS

4.1 Conventional op-amp Design

This section presents a conventional two stage op-amp. Furthermore, a frequency compensation technique is used to ensure closed loop stability if op-amps are made to operate with negative feedback. A conventional op-amp comprises of three basic stages as shown below. It is often called a "two stage" op-amp, ignoring the buffer stage. The first stage comprises of a high gain differential amplifier. The most dominant pole of the system is present in the first stage.

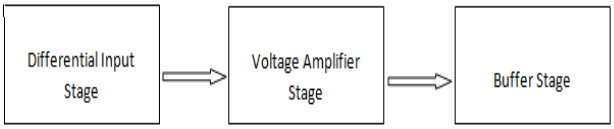

Fig -2: Block Diagram of Op-amp

Moreover, the differential amplifier is preferred in the first stage because of its ability to convert a differential input to a single ended output with a considerably high gain. The only drawback of the single stage is its reduced output swing. Hence, a common source amplifier is used in the second stage to improve the output swing by a considerable amount.

Table -1: Op-amp design Specifications

Parameter	Value
SUPPLY VOLTAGE	VDD=1.8v and VSS=-1.8v
CMRR	>=90 dB
GAIN	>=50 dB
PHASE MARGIN	>=60°
SLEW RATE	>=25 V/µsec
GBW	>=500 MHz
ICMR	-1.2 to 1.3v

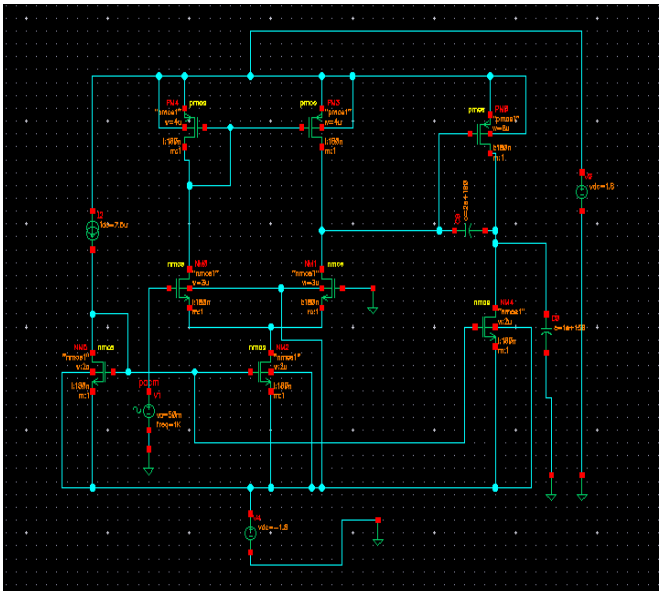

Fig -3: Op-amp design

The second stage contributes to very little input inferred noise due to the typically large gain of the first stage. Miller Compensation technique is used to facilitate pole splitting in order to maintain a 20 dB/dec roll-off. It also ensures stability when the op-amp is used with feedback. The buffer stage is considered when resistive loads are to be driven. If capacitive loads are considered then this stage is normally ignored. The fig. 3 shows the conventional Op-Amp design using cadence tools (180 nm tech) based on the specifications mentioned above.

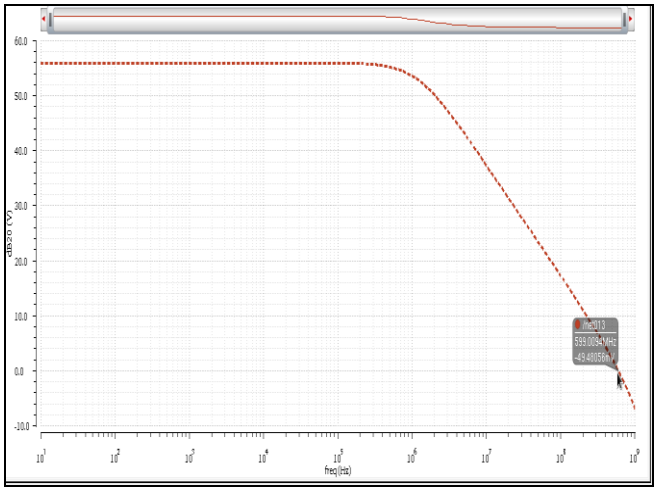

Fig -4: Frequency response plot of op-amp

4.2 Summing Amplifier

In summing amplifier, each input adds a particular voltage to the corresponding output multiplied by its individual constant gain factor. The feedback loop controls the voltage at the inverting input to match the potential at the non-inverting input. Both the non-inverting input and the inverting input are maintained at ground potential. This results in equal currents in both the resistors. The feedback resistor takes the sum of the currents supplied by the various inputs. The output voltage is given by

$$V_{out} = -R1.\left(\frac{V_{in(a)}}{R_a} + \frac{V_{in(b)}}{R_c} + \frac{V_{in(c)}}{R_c}\right)$$

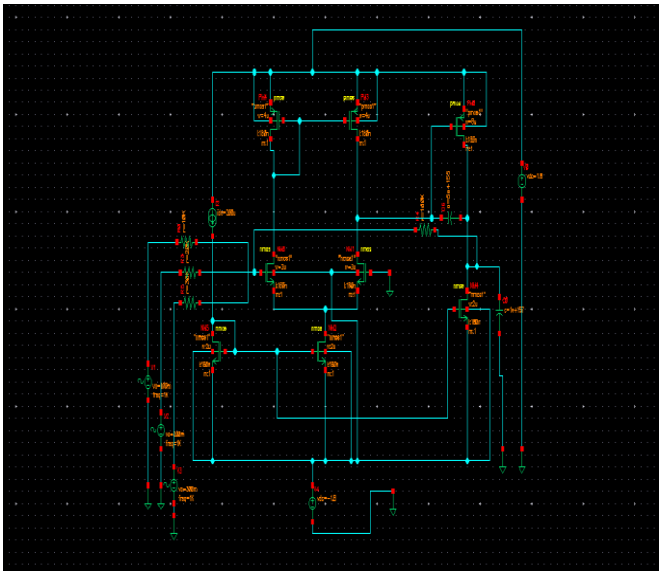

Fig -5: Schematic of a Summing Amplifier

As shown in fig 1. the output of the comparator is fed to the summing input after passing through a single bit DAC. This in turn forces the dc average value to be equal to the input voltage. Morever, a DAC can be constructed by using a summer and a set of resistors. Summing amplifiers make convenient level shifters also.

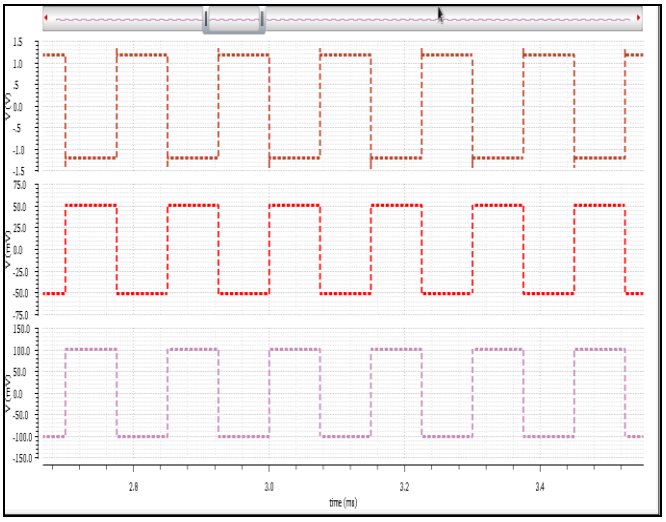

Fig -6: Output waveform of the summing amplifier

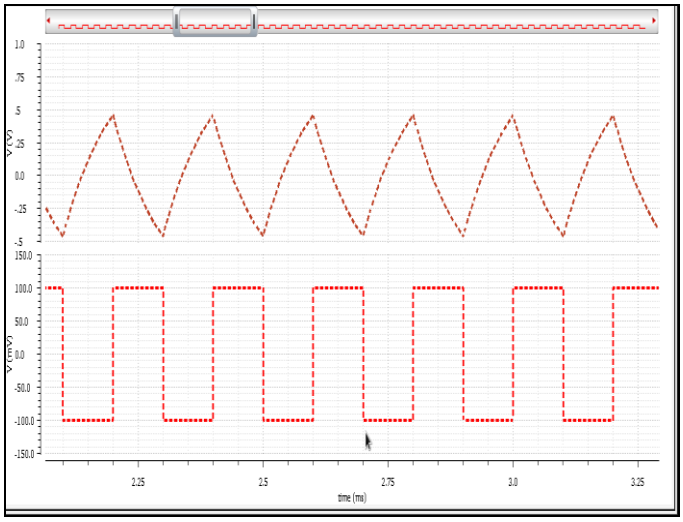

Fig -8: Output waveform of the Integrator

4.3 Integrator

The schematic of a practical integrator is as shown below. In the figure, the input voltage is given by V1. If V1=0, the integrator acts as an open loop amplifier. Here, in this case, the capacitor C1 acts as an open circuit to the input offset voltage. The input offset voltage is defined as the difference in input voltage needed to make the output voltage zero.

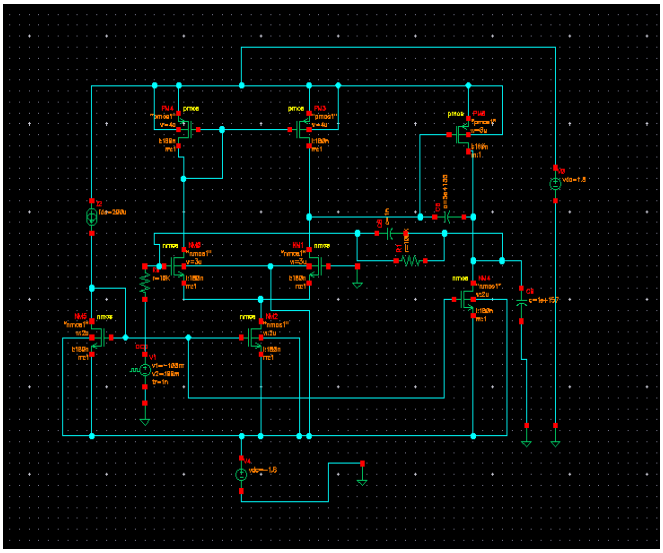

Fig -7: Schematic of an Integrator

The input offset voltage and the capacitor C1 produces an error voltage at the output of the integrator. To reduce this error voltage at the output, an additional resistor R2 is connected across the capacitor C1 in parallel. This additional resistor limits the low frequency gain and reduces variations at the output. Hence, the stability improves and low frequency roll-off problems can be corrected. Low frequency roll-off refers to the reduction in gain at low frequencies and stability refers to the attainment of constant gain when frequency of the input signal is varied over a certain range. The schematic of the practical integrator is as shown in the fig. 7.

4.4 Clamped Push-Pull Comparator

Normally, in the two stage open loop comparator stage, the propagation delay time is both due to transition of the first stage output and the second stage output. If we replace the current mirror load in the first stage with MOS diodes then the signal at the output of the first stage will be reduced in magnitude. Hence, gain reduces. This type of comparator is called "clamped" comparator.

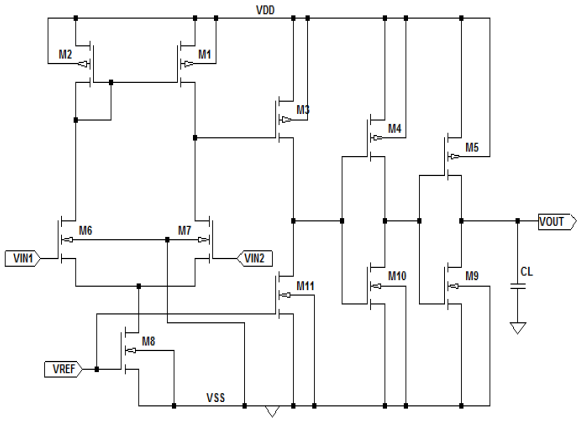

Fig -9: Schematic of a Clamped Push-Pull Comparator

Since, the comparator is push- pull type it has the ability to source and sink large values of current. But these type of comparators are slew rate limited if they drive large capacitive loads. In such a case, we can add several push-pull inverters to increase the driving capability. These inverters are nothing but high speed digital buffers. As seen in the fig below, the inverters M4-M10 and M5-M9 allow C_L to be large without sacrificing the speed. M4-M10 allows the current driving capability to be increased without loading M3-M11. The inverter M5-M9 allows the current sinking and sourcing to be further increased without loading M4-M10**.** The schematic of the clamped push-pull comparators designed to drive large capacitive loads is shown above.

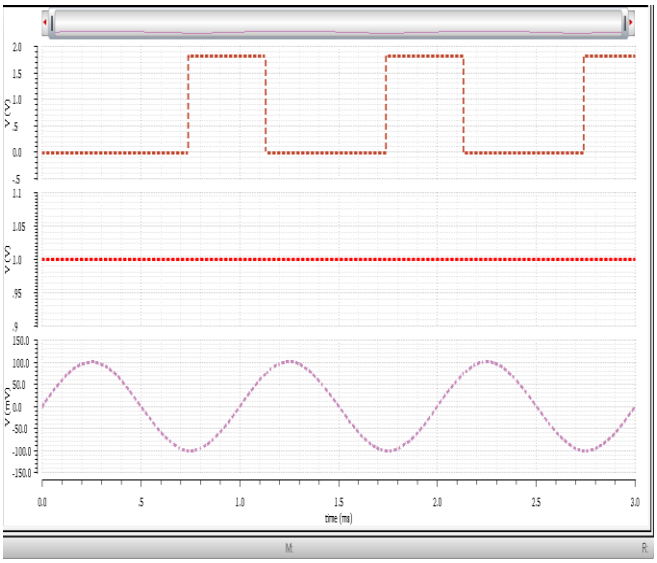

Fig -10: Output waveform of a Clamped Push-Pull Comparator

4.5 DAC

The most important component of the sigma delta modulator block is the 1 bit DAC. The output of the comparator is fed as an input to the DAC. It converts the output digital bit stream to an analog value depending on the reference voltage given. The figure shown below depicts a DAC which comprises of a basic multiplexer based design in which if logic 1 is given as an input, a voltage equal to +vref is fed back and if logic 0 is given as input, a voltage equal to –vref is fed back to the summing amplifier.

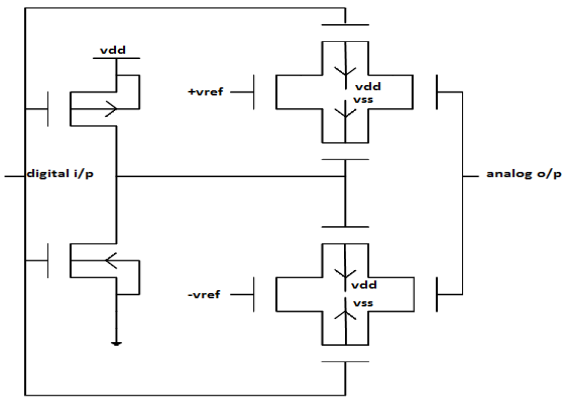

Fig -11: 1-bit DAC

5. CONCLUSION

This paper has undergone an extensive review of the existing research works on Sigma-Delta ADC. The design has been implemented using cadence 180 nm technology. The design operates at a power supply voltage of 1.8 V. The gain of the designed op-amp is found to be 57dB which is an improvement over the existing works. By using the sigma-delta toolbox the modulator coefficients have been obtained. For a third order system, the target bandwidth of 24 kHz has been obtained. The noise transfer function was found to be 1.5 and the SQNR was found to be 85.6 dB.

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BIOGRAPHY

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