FPGA BASED COMPUTER AIDED DIAGNOSIS OF CARDIAC MURMURS AND SOUNDS

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Abstract

The paper presents complete process and steps involved in FPGA based Computer Aided Diagnosis of cardiac abnormalities. Quality of the recorded heart beats is likely to be affected as the signal would be corrupted with noise. To overcome this problem Adaptive Line Enhancers (ALE) are used to eliminate the wide band noise and ALE, an adaptive noise cancellation technique is implemented with Least Mean Square (LMS) algorithm. The computation speed and noise rejection capability of DSPs do not serve the purpose. Since the FPGA is highly flexible, recursive algorithms are implemented in this device. The paper presents all the design steps involved in design of FPGA based phonocardiograph.

Keywords: *Phonocardiograph, Adaptive Line Enhancer, Least Mean Square, FPGA, Signal Acquisition*

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1. INTRODUCTION

Heart sound results from the activities related with the contraction and relaxation of atria and ventricles, valve movements, blood flow etc. There are at least two: the first when atrioventricular valves close at the inception of the systole and second when Aortic valves and Pulmonary valve close at the end of systole. Cardiac auscultation is the process of evaluating the magnitude, frequency, duration, number and quality of sounds [1]. Stethoscope is widely used by doctors as a preliminary diagnosis tool. However, Stethoscope is not reliable to diagnose cardiac abnormalities for instance, aortic insufficiency, aortic Stenosis, mitral insufficiency, mitral Stenosis etc. accurately. In order to overcome this, prominence is given for electronic devices for cardiac auscultation and one such device is phonocardiograph using which —visual representation and the recording of heart sounds—can be obtained, subsequently resulting in a comprehensive interpretation. Other features that enhance the utility of phonocardiograph are record and store, time and frequency analysis etc. The main challenge that we face in the design of this device is elimination of low frequency noise from power supply and background extraneous noise inherent in the vicinity and noise due to respiration noise, muscle tremors, stomach rumbling. They would impair the reception of heartbeats as the frequency range of the heart sounds and noise fall in the same range. To solve this problem of elimination of wideband noise, Adaptive Line Enhancer (ALE), an adaptive noise cancellation technique used for detection of faint signals in the presence of noise is used and it does not require any frame of reference eliminate the noise signal. The implementation of ALE is done by implementing LMS algorithm. Currently the digital signal processing applications such as adaptive filters are implemented in Digital Signal Processors [4]. The computation speed and noise rejection capability of DSPs do not serve the purpose. In addition, these DSPs are instruction based and 3 to 4 instructions are required for computation of mathematical expression. The sampled data of heart sounds must be captured through the input then forwarded to processing core for each operation and then the output. In contrast, FPGA is clock based and contains massive parallel structures made of uniform array of Configurable Logic Blocks (CLB), memory, DSP slices and every clock cycle has the ability to perform operation on incoming data. Since Phonocardiograph is real time device with very high system sample rate, I/O data rate, the device is implemented in FPGA (Spartan-3E) where algorithms can be designed with the help of block diagrams and state machines can be used instead of decision trees. The scope of this paper is to explain steps involved in design of FPGA based Phonocardiograph system.

2. COMPONENTS OF HEART SOUNDS

The significant constituents of heart sounds are first and second heart sounds (S1 and S2 respectively) [2]. S1 occurs during ventricular systole and is caused by the closure of the mitral and tricuspid valves. S2 occurs at beginning of ventricular diastole and is caused by the closure of the aortic and pulmonary valves. S3 is an additional sound which occurs just after S2 has reached relatively low energy state. S3 may be normal in people under 40 years and for athletes and emergence of this sound later in the life is abnormal. S4 occurs due to anomalous ventricular behavior and is usually observed in the pathological conditions. Heart murmurs are noises associated with the deviations in blood flow dynamics and improper closure of valves. Frequency of the normal heart sounds fall within a range of 20-250 Hz. As doctors say, any heart murmur is a blowing, whooshing or rasping sound heard during the heart beats. The sound is caused by irregular flow of blood through the heart valves and near the heart. For healthy hearts, the heart sounds (S1 and S2) are easy to

distinguish and heart murmurs on the other hand is caused by the turbulence of blood flowing through the cardiovascular system with possible heart diseases [3]. The heart has valves that close with each heartbeat, causing blood to flow in one direction. The valves are located between the chambers. The murmurs can happen due to several reasons such as valve not closing tightly and blood leaking backward (Regurgitation) or blood flowing through a narrowed or stiff heart valve (Stenosis). The murmurs are classified as Systolic murmurs and Diastolic murmurs based on the time during which they occur. Heart murmurs can have frequency in the high range of 700 Hz -1200 Hz.

3. HARDWARE IMPLEMENTATION

The important stages that are part of the design of Phonocardiograph are,

- Custom built transducer
- Signal conditioning
- Signal data acquisition and signal processing.

3.1 Custom Built Transducer

Heart's acoustic sound signals are converted to analog electrical signals using a custom sensor designed and developed to capture heart signals. The sensor system consists of a standard stethoscope chest piece to amplify acoustic signals and an MEMS microphone which convert the sound signals to electrical waveforms. The microphone is placed in the nearest vicinity of the chest piece. In order to enhance the signal quality and detection, an arrangement was made to solder a 3.5 mm cable to the base of the microphone and the other end of the cable was given as an input to the microphone.

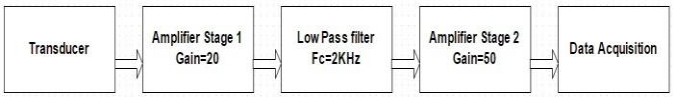

Fig.1 Signal Conditioning Block diagram

3.2 Signal Conditioning

Signal conditioning includes amplification, filtering and other activities required to achieve highest quality of the sensor output. The important stages are Custom built transducer, amplification and filtering units.

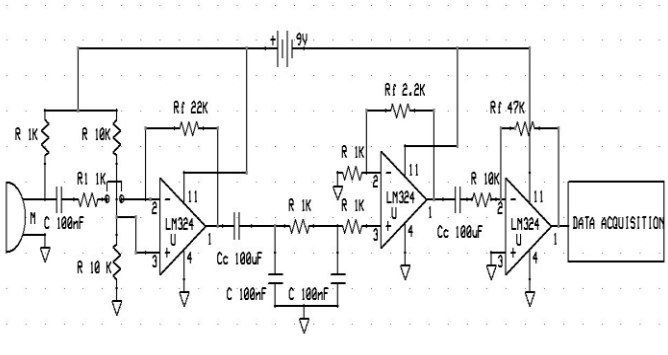

Fig.2. Signal Conditioning Circuit diagram

Fig.1 above shows the block diagram of signal conditioning unit and Fig.2 shows the circuit diagram of cascaded amplifier and filter constricted using OPAMP. The signal amplitude is amplified to make the signal suitable for filtering and further processing. High amplitude aids in better processing of a signal. The gain of the pre-amplifier is kept very low in the pre-amplification stage so as to keep the noise level to a minimum level. As shown in the above figure, the first amplifier stage was set with the gain of 10 so that it will increase the noise to a minimum level. The output of first stage is fed to a 4th order Butterworth low pass filter whose roll off frequency is 2000 Hz. The output of the filter is fed to second stage of amplifier whose gain is set to 100. Overall gain in the signal path is 1000. The reason of choosing Butterworth filter is, its pass band magnitude response is flat and stop band attenuation is steeper at 20db per decade. The output voltage after signal conditioning stage is in the range of 2.5- 3.5 volt.

4. SIGNAL ACQUISITION AND PROCESSING

Data acquisition is done using on board ADC present on Spartan-3E FPGA starter kit. The analog signal from signal conditioning circuit is fed into the Analog Capture Circuit of Spartan-3E starter kit, which includes a programmable pre-amplifier to scale the input signal for suitable voltage level and an Analog-to-Digital Converter to convert analog input signal to a 14 bit digital signal at a rate of 44000 samples per sec.

The acquired digital signal is internally connected to FPGA pins in Spartan-3E FPGA starter kit. The further processing of the signal is done inside FPGA, where the noises inherent in the vicinity are removed using Adaptive Filter technique. The adaptive filter is implemented in FPGA using LMS algorithm coded in Verilog. Also an Ethernet MAC Core is implemented in FPGA to send the processed digital signal to a MATLAB environment running in PC, through Ethernet cable, connected between PC and the Spartan-3E starter kit.

4.1 Adaptive Filter Theory

The Adaptive Line Enhancer (ALE) structure as shown in Fig. 3is enlarged to include Finite Impulse Response (FIR) with adaptive filter weights to obtain FIR-ALE structure as shown in Fig. 4. The FIR filter is also known as feed forward, non-recursive filter. The number of coefficients required increases with the increase in required SNR at the output.

The FIR filter is also called as tap delay line filter and is defined by the following difference equation.

$$y(n) = \sum_{0}^{N-1} w_k(n)x(n-k-d)\mathrm{d}) \qquad (1)$$

Where d is the prediction distance of the filter, $w_k(n)$n) represents the FIR filter coefficients. The delay de-correlates the noise components in the filter with respect to primary input while introducing a simple phase shift between sinusoidal components. The FIR ALE in this case is implemented using adaptive algorithm named LMS as shown in Fig .4.

ALE can be used as a potential means of eliminating wideband background noise overlapped with narrow band signal. In our case required narrow band signal is signal from heart whose frequency ranges between 20-250 Hz and broadband signal is [1]presence of noise contributed from several sources such as background noise, respiration noise, muscle tremors, stomach rumbling, non- optimal recording sites and weak sounds(Obese patients) etc. Many adaptive filter techniques normally require two inputs one is primary input and other is reference input whereas ALE implementation requires only one input. The reference input in this case is the delayed version of primary input. The narrow band components remain correlated with each other because of periodic nature of the input heart signals. The difference signal hence corresponds to uncorrelated noise signal based on which the filter weights of the FIR filter are adjusted.

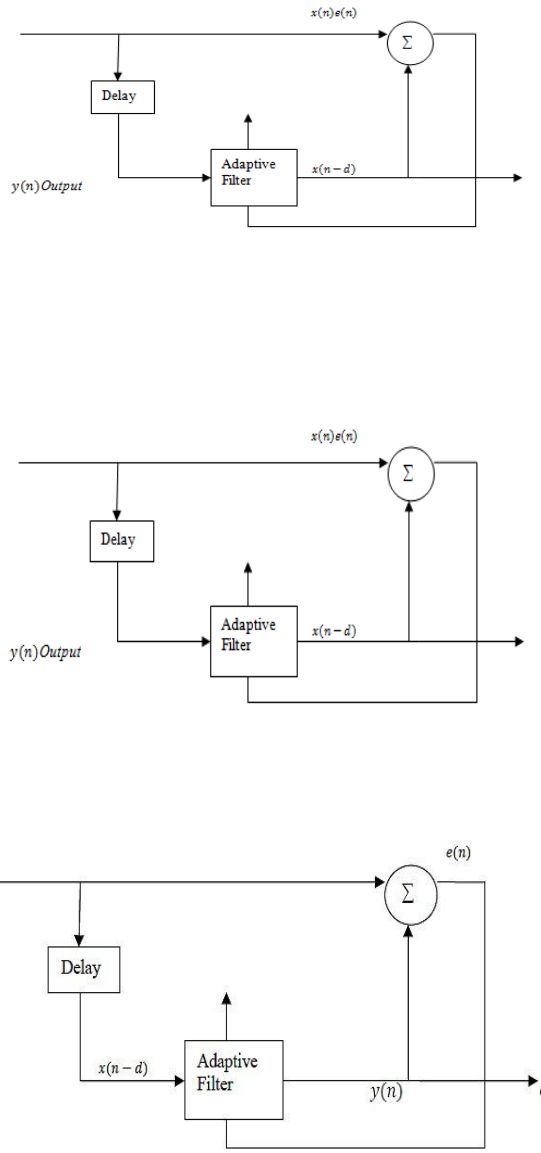

Fig.3. Adaptive Line Enhancer

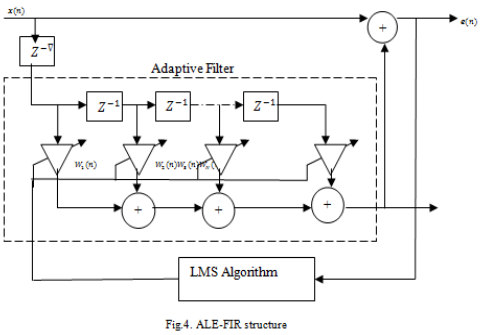

Fig.4. ALE-FIR structure

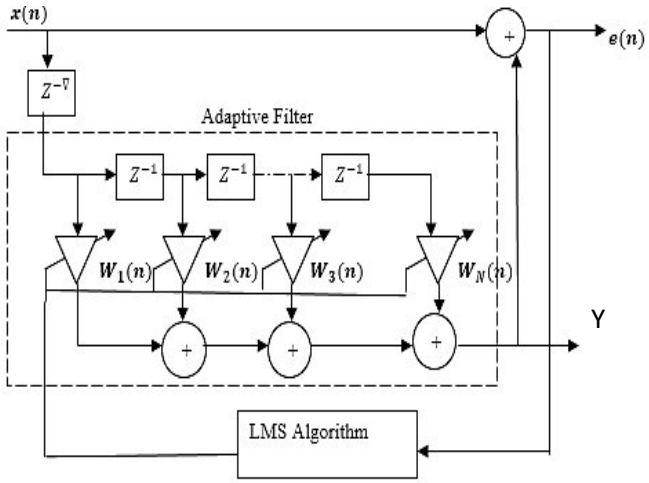

Fig.4. ALE-FIR structure

LMS adaptive filter output is given by

$$\boldsymbol{y}(n) = \sum_{i=0}^{N-1} \boldsymbol{w_i}(n)\boldsymbol{x}(n-i) = {W}^{T}(n)X(n) \quad (2)$$

$$\boldsymbol{X} = \left[\left(x_1(n), x_2(n-1) \dots \dots \dots . x_{N-1}(n-N+1)\right)\right]^T$$
$$\boldsymbol{W} = \left[\left(w_{1(n)}, w_2(n) \dots \dots \dots . w_{N-1}\right)\right]^T$$

$$\boldsymbol{X} = h\boldsymbol{s}(n) + \boldsymbol{noise}(n) \quad (3)$$

$$\boldsymbol{r}(n) = \boldsymbol{x}(n-d) \quad (4)$$

$$\boldsymbol{e}(n) = \boldsymbol{x}(n) - \boldsymbol{y}(n) \quad (5)$$

$$\boldsymbol{w_k}(n+1) = \boldsymbol{w_k}(n) + \mu\boldsymbol{e}(n)\boldsymbol{x}(n-k-d) \quad (6)$$

Where, X is the primary input signal which consists of heart signal component and wideband noise component [noise (n)]. The reference signal is the delayed version of the primary input signal by a delaying factor d. is the output of the adaptive filter which is the best estimate of the required response. $w_k(n)$ represents the adaptive filter weights and N represents the length of the adaptive filter.e(n) represents the error signal, μ represents the step size of the adaptive filter. The filter is considered to be moving average type.

The algorithm of LMS filter is implemented in FPGA as follows,

T1: $w_{i(n)}x(n-i+1)$

T2: Obtain the value of y_i(n)

T3: Calculate the value of $\sum_0^{N-1} y_i(n)$and $r(n) - \sum_0^{N-1} y_i(n)$

T4: Get the value of $y(n)$ and $e(n)$.

T5: Calculate $\mu e(n)x(n-k-d)$

T6: Calculate $w_k(n) + \mu e(n)x(n-k-d)$

T7: Get the value of $w_k(n+1)$

During T1, T2 and T3 the corrupted input primary signal is convoluted with filter coefficients to obtain the resultant signal y(n) which is compared with the reference signal (delayed version of the primary signal) to remove correlated signal which has required heart sound related information and based on the magnitude of the uncorrelated noise obtained after comparison as done in T3 e(n) is computed. Based on the value of the e(n) and μ, selected filter weights are adjusted in T5, T6 and T7. These steps are repeated until desired SNR is obtained at the output.

5. MATLAB GUI

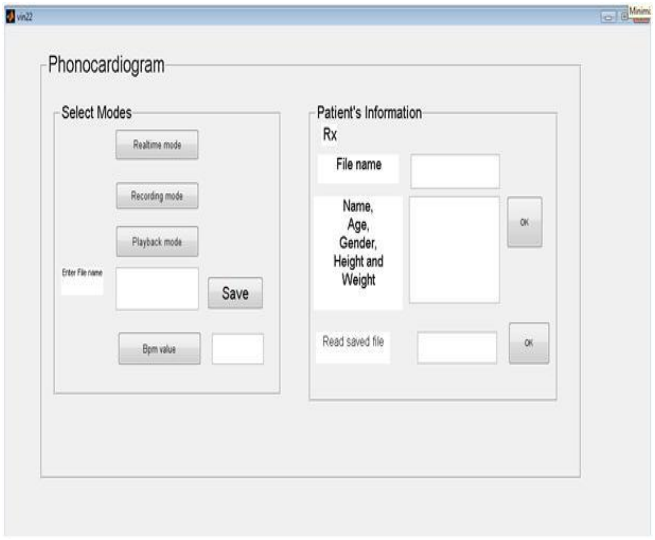

Fig.5. Phonocardiogram Graphical User Interface

Fig.5 shows the Graphical User Interface which is designed in MATLAB that will allow the doctors to create a profile for the patient and to operate the device in multiple modes. One mode is **REAL TIME AUSCULTATION** where the cardiac activity is visualized in MATLAB both in frequency as well as time domain. Second mode is **RECORD AND STORE** mode where the heart beat signals are first recorded for pre-specified interval and then visualized in time and frequency domain. The visualization is stored in the memory which can be used to track the progress of patient's health. The user interface includes fields to enter patients' information like their Name, Age, Height, Weight, Gender etc. The doctor can save this information as a text file in the computer memory and can be retrieved as needed.

6. RESULTS AND DISCUSSIONS

6.1 Time and Frequency Domain Representation of PCG Signal

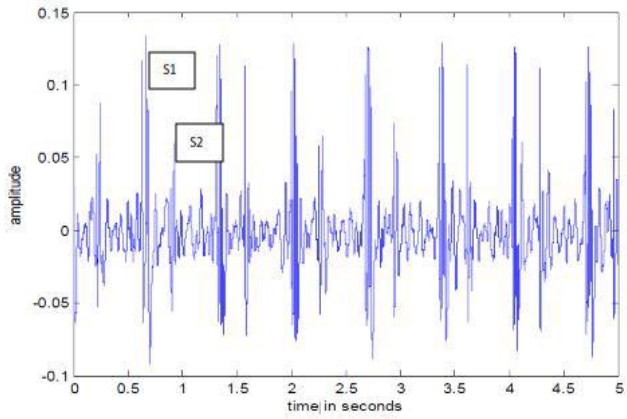

Fig 6 Time domain representation of the PCG signal

Fig .6 shows the heart beat signals obtained when a normal patient was examined. It can be observed that heart beat consists of two sounds S1 and S2. S1 has larger amplitude than S2 as evident from the above Fig. 4. If there are any cardiovascular disorders such as Systolic or Diastolic murmurs they can be visualized clearly through time domain waveforms. Systolic murmurs occur during systole and can be easily seen after S1 and before S2. Diastolic murmurs occur during diastole and can be easily seen after S2 and before S1.

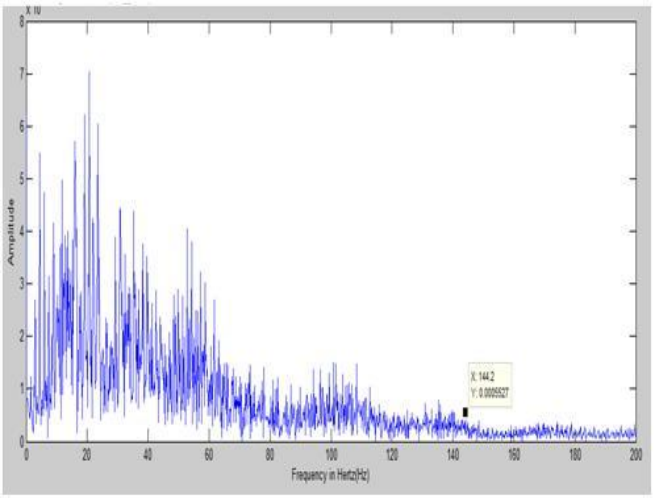

Fig.7. Frequency domain representation of the PCG signal

Fig.7. shows the frequency domain representation of the recorded signal. As evident from the above representation most of the frequency of interest for healthy heart is concentrated from 20Hz to 40Hz and it is clearly visible that high frequency disturbances and low frequency noise are removed to maximum extent. Since the murmurs have the distinctive frequency range of 700Hz – 1200Hz which can be clearly visualized from the frequency domain plot.

Appendix A

A.1. Abbreviations

ALE	Adaptive Line Enhancer
LMS	Least Mean Square
FPGA	Field Programmable Gate Arrays
PCG	Phonocardiograph
OPAMP	Operational Amplifier
DSP	Digital Signal Processor
MEMS	Microelectromechanical systems.
ADC	Analog to Digital Converter
FIR	Finite Impulse Response
CLB	Configurable Logic Blocks
MAC	Medium Access Control
FIFO	First In First Out
RAM	Random Access Memory
DRAM	Dynamic Random Access Memory

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BIOGRAPHIES

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