

# HARMONIC REDUCTION OF CASCADED MLI FED INDUCTION MOTOR DRIVE USING MODIFIED MODULATION STRATEGIES

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## Abstract

This paper proposes a modulating scheme for multilevel inverters, which may conjointly work in the over modulation range, using only the offset voltage injected in reference phase voltages. It doesn't involve any sector identification and considerably reduces the computation time when compared to the traditional space vector PWM technique. It is focused on the implementation of Cascaded H-bridge multilevel inverter fed induction motor by victimization the modulating technique of OVPWM with U-type carrier to the Five-level inverter. The PWM switching signals supported offset voltage injected in sine reference with U-type carrier been generated. a three phase Five-level cascaded inverter using IGBTs has been assembled and switched with the PWM signals generated. The multilevel inverter fed induction motor drive with SPWM and projected methods are performed and results are analyzed. The cascaded three-phase five level inverter fed induction motor simulated and therefore the performance of induction motor analyzed in varied aspects like, speed, torque etc.

**Keywords:** Multilevel concept, Cascade Multilevel inverter, Multi level carrier signals, Pulse width modulation, Total Harmonic Distortion

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## 1. INTRODUCTION

Modulation in multilevel inverters has recently been wide investigated; however the over voltage caused by multilevel modulation has not been mentioned totally. Many modulation ways, like space vector pulse width modulation (SVPWM), space vector control (SVC), duty cycle modulation (DCM) and a number of other sine-triangle comparison modulation variations are bestowed, for instance, within the literature given by wei.S et.al.[9] and Naumanen et.al.[13]. All the modulation ways, apart from the SVC, are supported pulse width modulation. The output voltage wave shape of the SVC resembles staircase that approximates the form of the reference wave. An example of a multilevel inverter victimization SVC is bestowed by Kouro.S et.al. [12]. Power electronic switches, particularly IGBTs became quicker in terms of turn-on and turn-off times that have led to the high dv/dt of the perimeters of the PWM voltage. As dv/dt becomes higher, an overvoltage can occur at even shorter cable lengths. This development has been totally reported by Persson et.al.[5] and Skibinski[7].

Wang et.al [8] in his investigation on sine triangle modulation technique declared that SPWM is the most typically used modulating technique suffers from bound draw-backs like low fundamental output voltage. The modified Reference Modulation techniques that provide improved performances as mentioned by M.H.Rashid [11] and are as trapezoidal, stair case, stepped, harmonic injected, space Vector PWM (SVPWM) and Offset voltage injected in reference(OVPWM). The above PWM techniques are applicable to three-phase inverters. But the last three techniques are commonly used for three-phase inverters.

Because of its flexibility of manipulation SVM has increasing applications in power converters and control. In the SPWM scheme for two-level inverters, every reference section voltage is compared with the triangular carrier and also the individual pole voltages are generated, freelance of every alternative as mentioned by Holtz.J [2].As per the literature given by Holmes [3], Kim. J et.al.[6], Carrara et.al.[4] and Baiju et.al.[10], to get the maximum attainable peak amplitude of the fundamental phase voltage, Voffset1, is added to the reference phase voltages, wherever the magnitude of Voffset1 is given by

$$V_{offset1} = \frac{-(V_{max} + V_{min})}{2} \quad (1)$$

In Equ. (1), Vmax is that the maximum magnitude of the three sampled reference phase voltages, whereas Vmin is that the minimum magnitude of the three sampled reference phase voltages, during a sampling interval. The addition of the common mode voltage, Voffset1, leads to the active inverter switching vectors being focused in a very sampling interval, creating the SPWM technique resembling the SVPWM technique as mentioned in Vander Broeck et.al. [1].

In multilevel case, PWM techniques with three completely different disposed triangular or U-type carriers were projected as follows:

- i. Alternate phase disposition (APOD) – each carrier wave shape is in out of phase with its neighbor carrier by 180°.
- ii. Phase opposition disposition (POD) – All carrier waveforms on top of zero reference are in phase and are 180° out of phase with those below zero.

- iii. Phase disposition (PD) - All carrier waveforms are in phase

## 2. MODIFIED MODULATING TECHNIQUES

Modulating techniques can be divided into two categories based on the reference signal and carrier signal. The conventional Sine wave reference is altered as trapezoidal wave, stepped wave, stair case wave, harmonic injected in reference sine wave, space vector wave and offset voltage injected in reference called as Trapezoidal PWM, Stepped PWM, Stair case PWM, Harmonic injected PWM, Space Vector PWM (SVPWM) and Offset voltage injected in reference PWM (OVPWM) respectively. These modified reference modulating techniques are implemented to five level Cascaded multilevel inverters at a switching frequency of 10 KHz. The comparative harmonic analysis can be made from Table1.

For OVPWM, Fig. 1 represents the reference and carrier signal comparisons to generate the PWM signals for the cascaded five level inverter. Fig.2 is evident for the THD spectrum of CC5LI with OVPWM or MSVPWM, in this modulation technique the fundamental voltage is 297.9 V and THD is 5.82% for the modulation indices 0.86 with switching frequency of 10 KHz and DC input of 100V at each H-bridge.

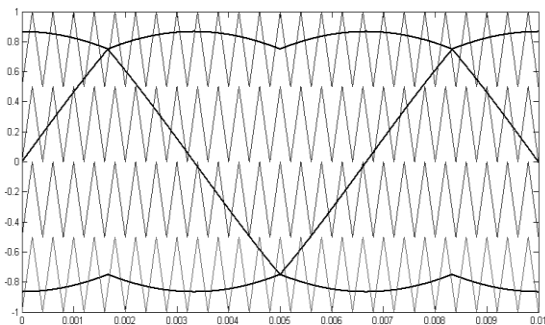


Fig 1 OVPWM with triangular carriers for 5-level inverters

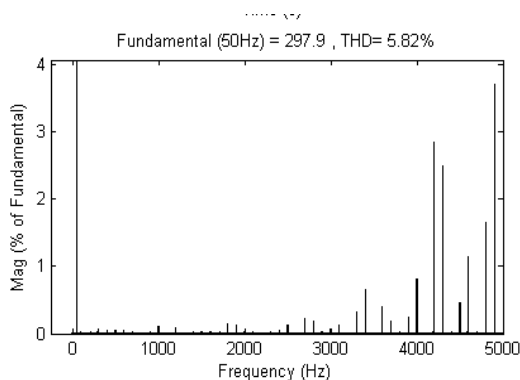


Fig 2 THD spectrum of CC5LI with MSVPWM

When observation comes to the comparison of last three modified reference modulating techniques i.e. The SVPWM, Third harmonic injected in reference PWM and Modified SVPWM or OVPWM, it can be observed that the shape of the reference wave looks similar.

Table 1 Comparison of THD and fundamental component for CC5LI with  $f_c$  of 10 KHz

Type of MRPWM ( $f_c$ of 10 KHz)	M=0.86		M=1	
	Fundamental Component	%THD	Fundamental Component	%THD
Sinusoidal PWM	297.9	6.53	346.4	6.08
Stair case PWM	322.6	7.36	375.1	10.77
Stepped PWM	295	8.03	344.2	9.19
Trapezoidal PWM	315.6	7.28	367	8.64
Third harmonic injected PWM	297.9	6.17	346.4	4.53
MSVPWM or OVPWM	297.9	5.82	346.4	4.14

But there is variation in performance as indicated in Table1. In addition to this, there is a large computations and complexity in determining the firing pulses for the SVPWM for three level inverter and this complexity increases as the number of levels increases. So, that conventional SVPWM cannot be opted. In case of third harmonic injected in reference PWM technique, there is an ambiguity in the amplitude of the third harmonic signal, because there is no fixed or particular value to be adopted. The various values in amplitude of third harmonic signal give variations in THD of the output. So, it is also cannot be opted.

The Modified SVPWM or OVPWM overcomes the above flaws, as it is not having computations and clarity in amplitude of the offset voltage to be injected i.e.  $(V_{min} + V_{max})/2$ . Because of above reasons, it is decided to select the Modified SVPWM. The name for this adopted as it is similar to the conventional SVPWM.

## 3. MODIFIED CARRIER MODULATION TECHNIQUES

The conventional triangular Carrier wave and proposed U-type carrier wave undergone for various shifting methods such as phase disposition (PD), Phase opposition with Disposition (POD), alternatively in opposition disposition (APOD)

### 3.1 OVPWM with Triangle and U-Type Carrier

As discussed in the earlier section, OVPWM signal generation does not involve checks for region identification, as in the SVPWM scheme. In this paper two types of carrier based techniques are proposed such as OVPWM reference with triangular carriers and OVPWM reference with U-type carriers. The above said two modulating strategies are under gone for triangular PD, POD and APOD with OVPWM

reference and U-type carriers PD, POD and APOD with OVPWM reference. The results are tabulated

### 3.1.1 Phase Disposition

In this method carriers are the same in frequency, amplitude and phases, but they are just different in DC offset to occupy contiguous bands as shown in Fig. 3. The carriers are in phase across all the bands. For this technique, significant harmonic energy is concentrated at the carrier frequency, but since it is co-phasal component, it does not appear in the line-to-line voltage.

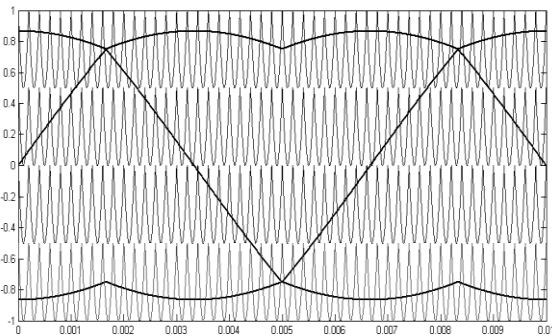


Fig 3 Generation of gate pulses with PD U-type carriers

Fig. 4 is the line-line output voltage and harmonic spectrum of cascaded five-level inverter with the modulating technique represented in Fig 3. For this the U-type carriers are used. The harmonic spectrum of cascaded five-level inverter with R-load shows that the total harmonic distortion is 3.68% with 346.3 V

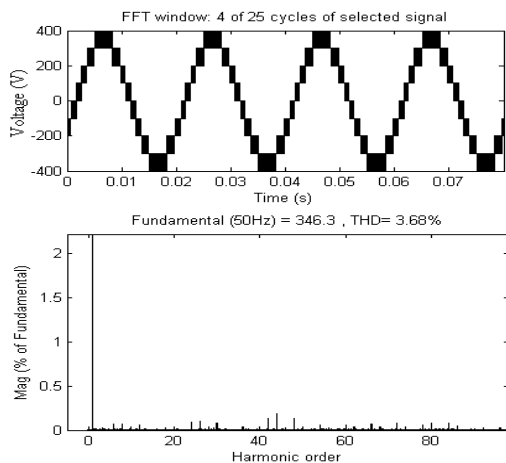


Fig 4 Output line-line voltage and harmonic spectrum u-type carriers

### 3.1.2 Phase Opposition Disposition (POD)

Carrier signals used in this method are the same in frequency and amplitude but they are different in phase. The carriers above the reference zero point are out of phase with those below that by  $180^\circ$  as shown in Fig.5

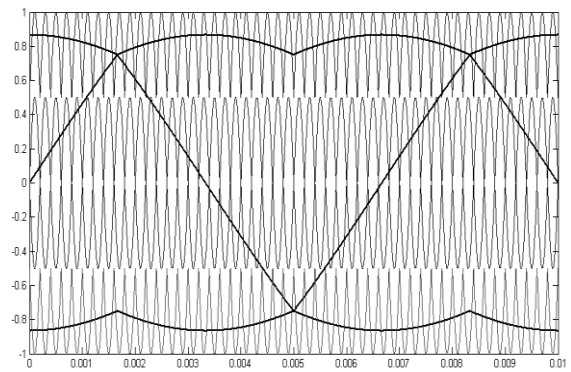


Fig 5 Generation of gate pulses with POD U-type carriers

### 3.1.3 Alternative Phase Opposition Disposition (APOD)

In this method carriers have the same frequency and the same amplitude but they are different in their DC offset and phases as shown in Fig. 6. In this method carriers are phase shifted by  $180^\circ$ , so this method uses two degrees of freedom of carriers namely their DC-offset and phases.

An another analysis brought out based on the results obtained in table 2, i.e. In the Modified Carrier Modulation technique Position Disposition (PD) have less THD with Sine wave reference as well as OVPWM. Hence by considering PD carrier based technique and SPWM, OVPWM with triangular carrier and U-type carrier are tested with 10KHz

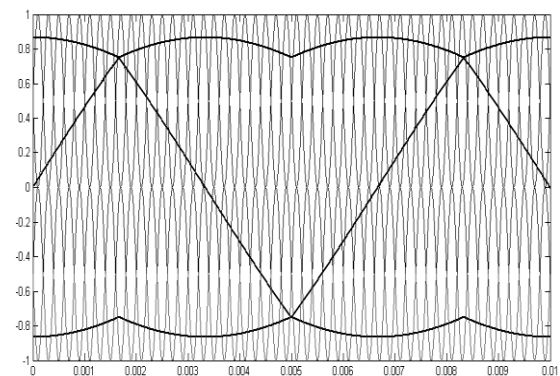


Fig 6 Generation of gate pulses with APOD U-type carriers

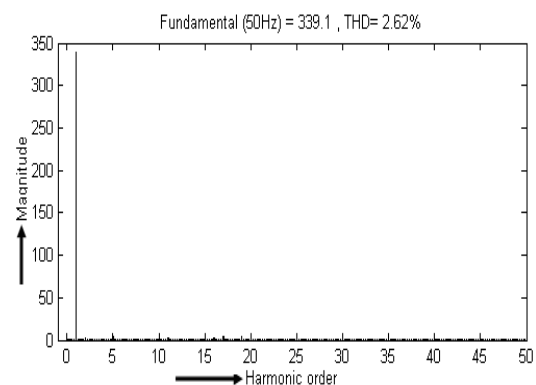


Fig 7 Spectrum of OVPWM with PD U-type carrier for CC5LI for 10 KHz

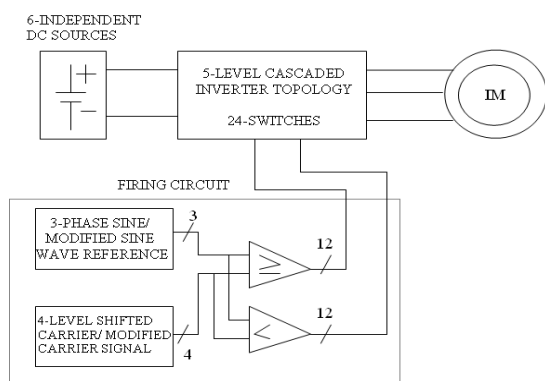
**Table 2** The %THD comparison of voltage for with MCPWM at  $f_c = 10\text{KHz}$

PWM technique M=0.86	Cascaded 5 Level Inverter	
	Fundamental component(V)	THD (%)
OVPWM with triangular carriers	339.2	5.77
OVPWM with U-type carriers	339.1	2.62

In this section, an analysis is brought out using Simulink; Modified Reference Modulating Techniques and Modified Carrier Modulating techniques are employed for the Cascaded 5-level 3-phase topology. The results are tabulated for fundamental component and %THD in Table 2. Hence, it is concluded that the OVPWM with U-type Carrier Modulating technique performance is best among all. So, it is recommended for the further research to fed asynchronous AC motors.

#### 4. OVPWM WITH U-TYPE CARRIER MODULATING TECHNIQUE FOR CASCADED H-BRIDGE MLI FED 3-Φ INDUCTION MOTOR

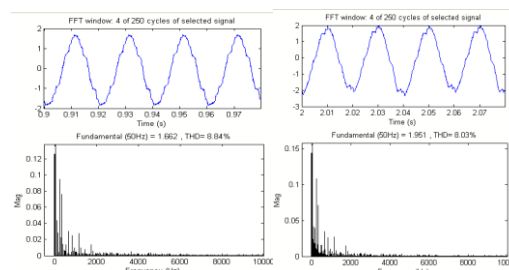
The complete block diagram of cascaded five-level inverter fed induction motor drive is shown in Fig.8, in this three phase cascaded five-level inverter topology consists of six H-bridges (i.e. two H-bridges per phase) with six individual DC sources. Two comparators are used in the firing circuit, one for three phase reference signal or modified reference signal and the other is for four level shifted carriers or modified carriers. By using of this combination total 24 pulses are generated to trigger 24 semiconductor switches i.e. IGBTs.



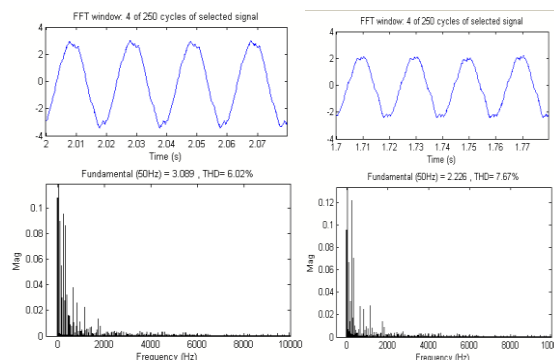
**Fig 8** Block diagram of cascaded five level inverter fed induction motor drive

Fig 9 shows the stator current drawn from the cascaded H-bridge five level inverter for the loads ranging from no-load to 27N-m applied at 1.5 sec. Fig 9 (a) represents the no-load current characteristics such as fundamental component and its harmonic content. At starting, current transients occurs in the range of 10A-12A and it settles to a steady state value with in a small interval of time 0.3sec as 1.6A with %THD of 8.84. Harmonic spectrum obtained for four cycles from 0.9sec to 0.98sec as indicated in the fig 9(a).

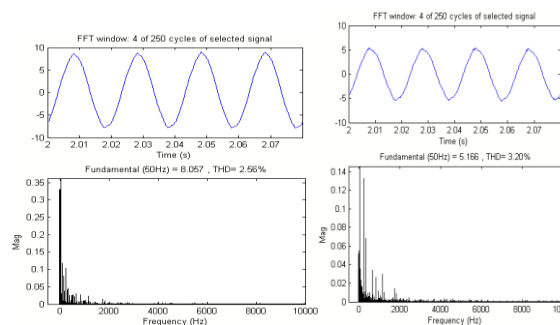
Fig 9(b) to 10(f) represents stator current characteristics for a load of 5 N-m,7 N-m,12 N-m,20 N-m and 27 N-m. From the figures, it can be observed that the raise in load current and fall in %THD as follows 1.951A with 8.03% for a load of 5N-m , 2.226A with 7.67% for a load of 7N-m, 3.089A with 6.02% for a load of 12N-m, 5.166A with 3.20% for a load of 20N-m and it is 8.05A with 2.56% for a load of 27N-m. From the results it is also observed that the stator current attaining sinusoidal form as the load increases from 5N-m to rated value of 27N-m, and it reduces the harmonic current.



**Fig. 9 (a)** no load **Fig. 9 (b)** 5 N-m



**Fig. 9(c)** 7 N-m **Fig. 9 (d)** 12 N-m



**Fig. 9(e)** 20 N-m **Fig. 9(f)** 27 N-m

**Fig 9** Stator current THD of CC5LI fed IM with various loads at t=1.5 sec

Fig 10 (a) to (e) shows the speed characteristics for the various loads of 5N-m, 12N-m, 20N-m, 25N-m and 27 N-m applied at 1.5 sec. It is observed that the motor has attained its no-load speed of 157rad/sec which is equivalent to the 1500 rpm in the less time of 0.3 sec. There is a variation in speeds to 153 rad/sec at 1.6 sec for a load of 5 N-m, 143 rad/sec at 1.7 sec for a load of 12N-m, 127rad/sec at 2.2 sec for a load of 20N-m and 110rad/sec at 2.75 sec for a load of 25N-m.

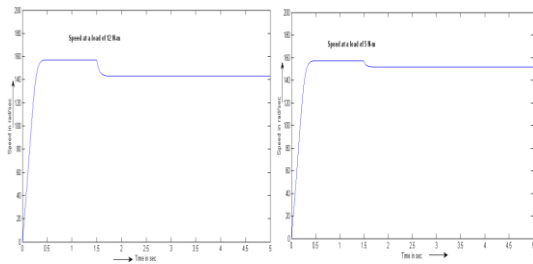


Fig. 10 (a) At a load of 5 N-m Fig. 10 (b) At a load of 12 N-m

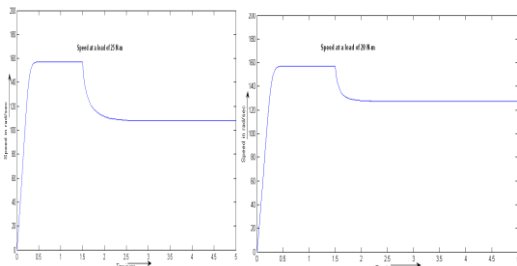


Fig.10 (c) at a load of 20 N-m Fig 10 (d) at a load of 25 N-m

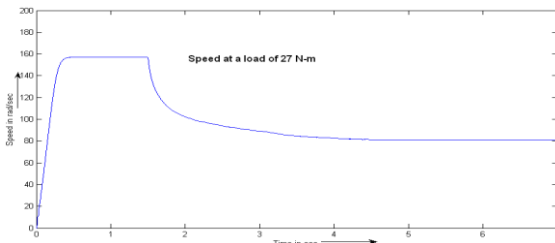


Fig10 (e) at a load of 27 N-m

Fig 10 Speed characteristics of CC5LI fed IM for various loads

Especially Fig 10 (e) at a load of 27 N-m has attained a steady speed of 80 rad/sec at 4 sec, which shows the poor performance beyond the rated torque of 25 N-m

Table 3 Performance of 3-Φ IM at various loads

Load (N-m)	Input voltage		Input current		Speed (rad/sec)
	V	%THD	I	%THD	
0	339.6	2.66	1.662	8.84	157
5	339.6	2.66	1.951	8.03	155
7	339.6	2.66	2.226	7.67	149
9	339.6	2.66	2.535	6.54	147
12	339.6	2.66	3.089	6.02	143
20	339.6	2.66	5.166	3.20	127
25	339.6	2.66	7.077	2.17	110
27	339.6	2.66	8.059	2.56	80

### 5. CONCLUSIONS

In this section the simulation results of cascaded five-level inverter fed induction motor with proposed modulating technique are analyzed with respect to line-line voltage waveform, current waveform, the THD spectrum of line-line voltage and torque speed characteristics of induction motor. The simulation results of induction motor speed with

cascaded five level inverter based modified SVPWM with no-load and with various step loads like 5 N-m, 7N-m, 9N-m, 12 N-m,20N-m,25 N-m and 27N-m are obtained as tabulated in Table 3.From all these observations it can be concluded that the speed will reach the steady state without oscillations in the case of cascaded five-level inverter. The %THD of Line-Line output voltage of cascaded five-level inverter is 2.66% with the U-type carrier PD with OVPWM.

Future scope of this research can be stated as, based on the simulated analysis, the OVPWM with U-type carrier modulation technique implementation with the digital controllers can be applied in industrial areas of medium and high power applications to avail the better performance in output, it is also recommended for the machines with higher rating suits well because of their good power factor.

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