ANALYSIS OF DC CAPACITOR VOLTAGE BALANCE METHOD FOR H-BRIDGE INVERTER BASED POWER LINE CONDITIONER

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Abstract

Among the various multilevel inverters, cascaded multi level inverters are widely known for their many advantages like modularized circuit, requirement of less number of components as compared to other multilevel inverters and possibility of switching redundancy for inner voltage levels. For power conditioning applications a cascaded multi level inverter with capacitors can be used instead of dc sources. But the voltage balancing of dc capacitors is a critical problem. This paper presents an algorithm by which the capacitor voltages can be balanced significantly. The charging and discharging process of capacitor is dependent on the width of the output pulses.

A mathematical model of H- bridge inverter based power conditioner is developed. Simulation has been carried out using MATLAB/ SIMULINK and the results are presented.

Keywords— *Cascaded H- Bridge Inverter, DC capacitor voltage balance, voltage balancing control technique, point of common coupling (PCC), power line conditioner (PLC), Active Power Filter(APF), Static Compensator (STATCOM)*

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1. INTRODUCTION

Because of the ever increasing demand of power the non-linear loads are being used widely. But the presence of these loads pollutes the power system as they draw large amounts of harmonic currents making it less suitable. Also there is always a need to control the power more efficiently and safely. In order to meet the demand and to achieve controllability modern power electronic equipment came into picture which has been revolutionalized over the past few decades.

But there are some problems associated with the power electronic equipment. Unlike the conventional loads, they control the flow of power by chopping, flattening, or shaping the system voltages or currents. These waveform distortions cause problems for neighbouring loads and tend to have a detrimental effect on the quality of power provided to the end users. One solution that has great potential is the power line conditioner (PLC). This device can correct the network distortion caused by the power electronic loads by injecting equal but opposite distortion at selected PCCs. Thus the distortions can be compensated successfully to some extent. It appears to be an attractive method for reducing voltage and current distortion, power quality problems like voltage spikes, transients and flicker. Thus this device enhances the quality of the power that is being fed to the end user. Also it achieves good voltage profile by regulating the voltage.
PLCs use an inverter and DC source. The dc source is alternately connected or disconnected rapidly to absorb or supply power as per requirement. For power conditioning applications the dc source of an inverter consists of a capacitor that resists the voltage changes. Usually multilevel inverters are preferred as they reduce the voltage stress, output waveform is free of harmonics and the output power can be improved. Among the various topologies of multilevel inverters, the cascaded multi level inverter is the best option as it improves the voltage profile and compensates the reactive power and the harmonics caused by the non-linear loads. But the voltage balancing control of the capacitor is quite cumbersome.

This paper presents an algorithm for balancing the charging and discharging processes of the capacitors in order to maintain the equal voltages at the capacitors of two units of inverter. This process is based taking the output pulses of the inverter into consideration. This paper provides a detailed theoretical analysis. This method can be implemented to many industrial applications. A mathematical model is developed based on the output pulses of the H- bridge inverter utilizing the voltage switching functions is developed as a means to investigate the control technique and to offer insight to the problem. The regulation of the output pulses of the H- bridge inverter to redistribute the active power is reported.

2. PRINCIPLE OF H-BRIDGE INVERTER BASED POWER LINE CONDITIONER

The Fig.1 shows the schematic diagram of a three phase cascaded H- bridge inverter based power line conditioner. The nonlinear load draws non-sinusoidal current which distorts the sinusoidal current produced by the source , thus results in introduction of harmonics into the system and makes it less efficient. The power line conditioner injects some amount of current at PCC which is equal but opposite to the harmonic content drawn by the load. Fig.1 shows that each phase of this equipment consists of two H-bridge inverter units. $u_{dc_{a1}}$, $u_{dc_{a21}}$ are capacitor voltages of the two H-bridge units of phase A respectively. H- bridge inverter consists of four IGBT switches $T_{a11,}$ $T_{a12,}$ $T_{a13,}$ T_{a14} for phase A as shown in Fig. 1.

The H-bridge inverter gives four switching states for different combinations of switches .The following table shows the switching states for the first unit of the H- bridge of phase A.

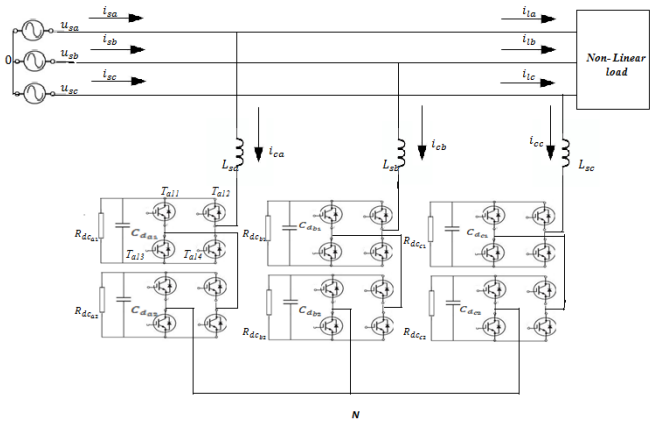


Fig1. Block diagram of H- bridge inverter based PLC

Table 1 Switching states of H- bridge inverter

T_{a11}	T_{a12}	T_{a13}	T_{a14}	S_{a1}
ON	OFF	OFF	ON	1
OFF	ON	ON	OFF	-1
ON	ON	OFF	OFF	0
OFF	OFF	ON	ON	0

Thus each H-bridge inverter unit results in three voltage levels. The same pattern holds good for the other H-bridge units of other phases too which can be represented as S_{a2} for second unit of phase A, S_{b1}, S_{b2}, S_{c1}, S_{c2} for first and second units of phases B and C respectively.

From Table.1 the following relation between the current and voltage between dc and ac parts can be obtained.

$$u_{a1} = S_{a1}.u_{dc_{a1}} \text{----------Eq.1}$$

$$i_{dc_{a1}} = S_{a1}.i_{ca} \text{----------Eq.2}$$

u_{a1} is the output voltage of the first H- bridge, $i_{dc_{a1}}$ is the current through the flying capacitor of first H- bridge. The mathematical model of power line conditioner with H- bridge inverter can be represented in stator co-ordinates as follows:

$$Z\dot{X} = AX + Be \text{----------Eq.3}$$

Where A =

$$\begin{bmatrix} -R_{sa} & 0 & 0 & \frac{2}{3}S_{a1} & \frac{2}{3}S_{a2} & -\frac{1}{3}S_{b1} & -\frac{1}{3}S_{b2} & -\frac{1}{3}S_{c1} & -\frac{1}{3}S_{c2} \\ 0 & -R_{sb} & 0 & -\frac{1}{3}S_{a1} & -\frac{1}{3}S_{a2} & \frac{2}{3}S_{b1} & \frac{2}{3}S_{b2} & -\frac{1}{3}S_{c1} & -\frac{1}{3}S_{c2} \\ 0 & 0 & -R_{sc} & -\frac{1}{3}S_{a1} & -\frac{1}{3}S_{a2} & -\frac{1}{3}S_{b1} & -\frac{1}{3}S_{b2} & \frac{2}{3}S_{c1} & \frac{2}{3}S_{c2} \\ S_{a1} & 0 & 0 & -\frac{1}{R_{dc_{a1}}} & 0 & 0 & 0 & 0 & 0 \\ S_{a2} & 0 & 0 & 0 & -\frac{1}{R_{dc_{a2}}} & 0 & 0 & 0 & 0 \\ 0 & S_{b1} & 0 & 0 & 0 & -\frac{1}{R_{dc_{b1}}} & 0 & 0 & 0 \\ 0 & S_{b2} & 0 & 0 & 0 & 0 & -\frac{1}{R_{dc_{b2}}} & 0 & 0 \\ 0 & 0 & S_{c1} & 0 & 0 & 0 & 0 & -\frac{1}{R_{dc_{c1}}} & 0 \\ 0 & 0 & S_{c2} & 0 & 0 & 0 & 0 & 0 & -\frac{1}{R_{dc_{c2}}} \end{bmatrix}$$

$$Z = diag[L_{sa} \quad L_{sb} \quad L_{sc} \quad C_{d_{a1}} \quad C_{d_{a2}} \quad C_{d_{b1}} \quad C_{d_{b2}} \quad C_{d_{c1}} \quad C_{d_{c2}}]$$

$$X = [i_{ca} \quad i_{cb} \quad i_{cc} \quad u_{dc_{a1}} \quad u_{dc_{a2}} \quad u_{dc_{b1}} \quad u_{dc_{b2}} \quad u_{dc_{c1}} \quad u_{dc_{c2}}]^T$$

$$B = diag[1 \quad 1 \quad 1 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0]$$

$$e = [u_{sa} \quad u_{sb} \quad u_{sc} \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0]^T$$

3. ANALYSIS OF VOLTAGE BALANCE METHOD

If various parameters and the conducting times of the units of H-bridge inverter are same, the actual power of each unit will be same. But because of the dispersion of the dc capacitor parameters, unequal conducing, losses of DC capacitor, switching losses of the devices, the active power of the units of H- bridge inverter will be unequal. This results in unequal voltages of the DC capacitors of two units of H- bridge. To redistribute the total active power equally between the two units and to make the DC capacitor voltages equal to the reference value, an additional control loop must be added.

$$i_{ca}(t) = \sqrt{2}\, I \cos\ \omega t \text{----------Eq.4}$$

Using Eq.1, Eq.2 and Eq.3, the following equation can be obtained.

$$C_{d_{a1}} \frac{du_{dc_{a1}}}{dt} + \frac{u_{dc_{a1}}}{R_{dc_{a1}}} = S_{a1}.\sqrt{2}\, I \cos\ \omega t \text{----------Eq.5}$$

From Eq.5, it can be seen that the voltage of DC capacitor of first bridge of H- bridge of phase A is dependent on the parameter values of $C_{d_{a1}}$ and $R_{dc_{a1}}$, switching state and output current of phase A. Out of the above mentioned factors only the switching states of the inverter is variable. The parameter values of $C_{d_{a1}}$ and $R_{dc_{a1}}$ are fixed. Also the value of the output current cannot be controlled. These conditions are applicable to all the H-bridge inverter units of all the three phases.

$$P_{a1} = \int_{\frac{\pi}{2}-\varphi_{a1}-\frac{W_{a1}}{2}}^{\frac{\pi}{2}-\varphi_{a1}+\frac{W_{a1}}{2}} u_{dc}\ .\sqrt{2}\, I \cos\ \omega t\, d\omega t$$
$$= 2\sqrt{2}\, u_{dc} I\, Sin\varphi_{a1}.\sin\frac{W_{a1}}{2} \text{----------Eq.6}$$

$$\sin\frac{W_{a1}}{2} \approx \frac{W_{a1}}{2} \text{----------Eq. 7}$$

$$P_{a1} = 2\sqrt{2}\, u_{dc} I\, Sin\varphi_{a1}.\sin\frac{W_{a1}}{2} = \sqrt{2}\, u_{dc} I\, Sin\varphi_{a1} W_{a1} \text{------}$$
$$\text{----------Eq.8}$$

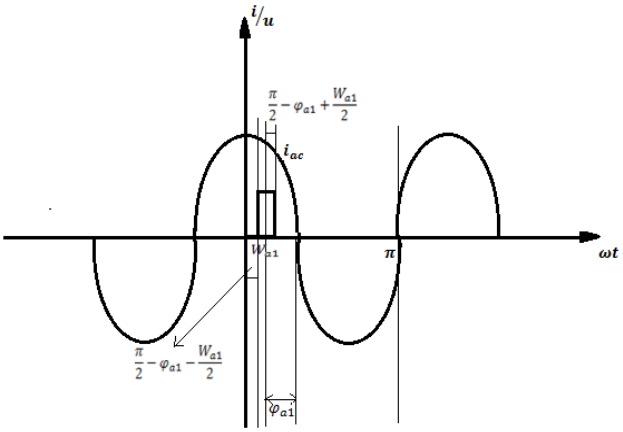


Fig.2 Output current and Output pulse of the inverter

Fig.2 explains the relationship between output current and output pulse of the H-bridge inverter. The output pulse can be used as a supplement for output voltage of the inverter.

The active power absorbed by the first unit of H-bridge inverter can be expressed as

$$P_{a1} = \int_{\frac{\pi}{2}-\varphi_{a1}-\frac{W_{a1}}{2}}^{\frac{\pi}{2}-\varphi_{a1}+\frac{W_{a1}}{2}} u_{dc}\ .\sqrt{2}\, I \cos\ \omega t\, d\omega t$$
$$= 2\sqrt{2}\, u_{dc} I\, Sin\varphi_{a1}.\sin\frac{W_{a1}}{2} \text{----------Eq.9}$$

Where $W_{a1}$is the width of the output pulse, φ_{a1} is phase angle of the output pulse.

When the switching frequency is high, the width of the output pulse is very small,

$$\sin\frac{W_{a1}}{2} \approx \frac{W_{a1}}{2} \text{---------- Eq.10}$$

Eq.9 on simplification can be written as

$$P_{a1} = 2\sqrt{2}\, u_{dc} I\, Sin\varphi_{a1}.\sin\frac{W_{a1}}{2}$$
$$= \sqrt{2}\, u_{dc} I\, Sin\varphi_{a1} W_{a1} \text{----------Eq.11}$$

Thus from Eq.6 it is evident that the active power absorbed by the inverter can be regulated either by varying phase angle φ_{a1} or the width of the output pulse W_{a1}or both. In this paper, regulating the width of the output pulses is only considered.

Considering switch period to be T_s and T as the fundamental period, the width of one switch period can be expressed as

$$\frac{2\pi T_s}{T} \text{----------Eq.12}$$

The equivalent output voltage of the first H-bridge unit in switch period in average model is expressed as

$$\frac{W_{a1}}{2\pi}.\frac{T}{T_s}.u_{dc} \text{---------- Eq. 13}$$

4. CAPACITOR VOLTAGE BALANCING TECHNIQUE

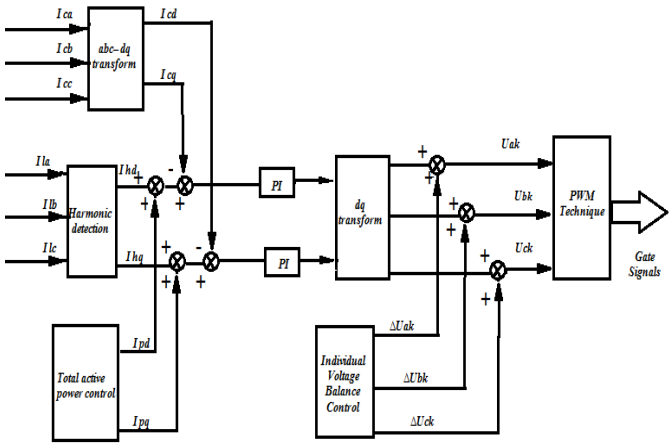


Fig. 3: Control block Diagram of the whole system

Fig. 3 shows the control block diagram of the whole system. It consists of harmonic current extraction, current tracking control and capacitor voltage control blocks. Harmonic currents are detected using Instantaneous Reactive Power theory. The output current waveform can be controlled by using PI controller. This dc capacitor voltage algorithm can be divided into two parts.

(i) Overall active power control in the method in which the sum of the capacitor voltages of each phase are made equal to the reference value.

(ii) Individual voltage balance control is the method in which the capacitor voltage of each H- bridge unit is made equal.

4.1 Overall Active Power Control

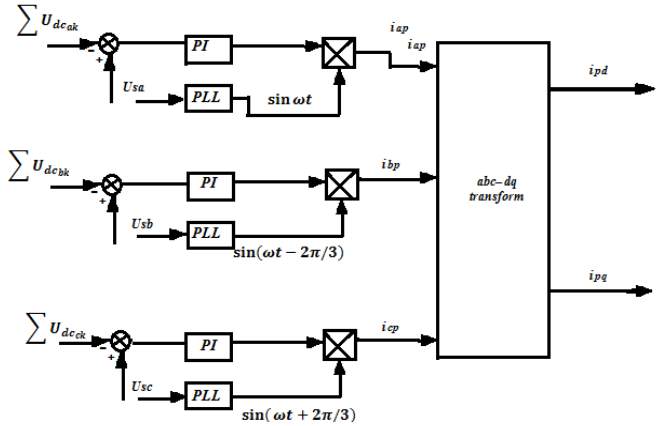


Fig.4: Block Diagram of Overall Active Power Control

This principle is similar to that of a two – level APF. The harmonic currents are detected and compared to that of a reference value. The PLL block provides a 120degree phase shift for all the three phases. The PI controller is used to vary the output current waveform based on the error generated. Thus the corresponding currents those are equal and opposite to the harmonic currents are generated and transformed to two phases as per requirement.

4.2 Individual Voltage Balance Control

When the width of the output pulse is changed from W_{a1} to ΔW_{a1}, the active power transferred from power grid to DC side of H- bridge is expressed as

$$\Delta P_{a1}^{*} = \int_{\frac{\pi}{2}-\varphi_a+\frac{W_a}{2}-\frac{\Delta W_a}{2}}^{\frac{\pi}{2}-\varphi_a+\frac{W_a}{2}+\frac{\Delta W_a}{2}} u_{dc}\,.\sqrt{2}\,I\cos\ \omega t\,d\omega t - 2\int_{\frac{\pi}{2}-\varphi_a+\frac{W_a}{2}-\frac{\Delta W_a}{2}}^{\frac{\pi}{2}-\varphi_a+\frac{W_a}{2}+\frac{\Delta W_a}{2}} \sqrt{2}\ u_{dc}\ I\cos\ \omega t\,d\omega t$$

$$= \sqrt{2}\ u_{dc}\ I\ Sin\ \varphi_a\ (W_{a1}+\Delta W_{a1}) - \sqrt{2}\,u_{dc} I\ Sin\varphi_a W_a$$

$$= \sqrt{2}\,u_{dc} I\ Sin\varphi_a \Delta W_a$$ ----------Eq. 14

When the switching frequency is high, DC voltage variation of each H- bridge inverter unit is very small. So loss of the equivalent resistance connected in parallel with the capacitor is approximately equal before and after the regulation.

When the dc voltage of the unit changes from $u_{dc_{a1}}$ to $u_{dc_{a2}}$, the active power is absorbed after regulation.

$$\Delta P_{dc_{a1}} = \frac{1}{2}C\left(u_{dc1_{a1}}^2 - u_{dc2_{a1}}^2\right)$$

$$= \frac{1}{2}C\left(u_{dc1_{a1}} + u_{dc2_{a1}}\right)\left(u_{dc1_{a1}} - u_{dc2_{a1}}\right)$$

$$\approx C.u_{dc}\Delta u_{dc1_{a1}}$$ ----------Eq.15

By solving Eq.14 and Eq. 15 the relationship between $\Delta\ u_{dc}$ and ΔW_{a1} can be determined as follows:

$$C.\Delta u_{dc1_{a1}} = 2\sqrt{2}\ I\ Sin\varphi_{a1}\Delta W_{a1}$$ ----------Eq.16

$2\sqrt{2}\ I\ Sin\varphi_{a1}$ represents output current value in the switching cycle. Replacing the constant quantity by K and $2\sqrt{2}\ I\ Sin\varphi_{a1}$ by output current value i_{ca} , the width of the output pulse is changed by the factor

$$\Delta W_{a1} = \frac{K.\Delta u_{dc1_{a1}}}{i}$$ ----------Eq.17

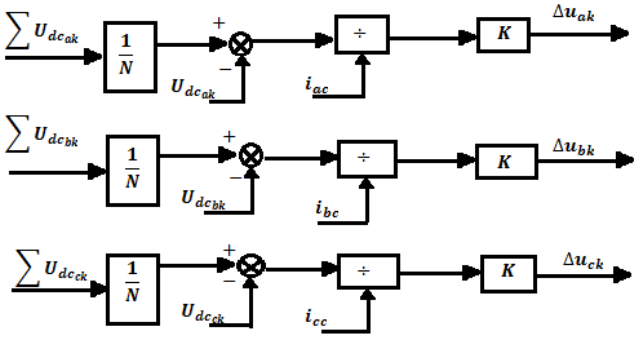


Fig.5: Control block of Individual Voltage Control Method

As long as Eq.17 is satisfied that is change in the value of the output width of the pulse is proportional to the required absorbing active power of each unit, then the final output of

the inverter remains unchanged and the dc capacitor voltages of the two H-bridge inverter units will be equal.

5. SIMULATION RESULTS

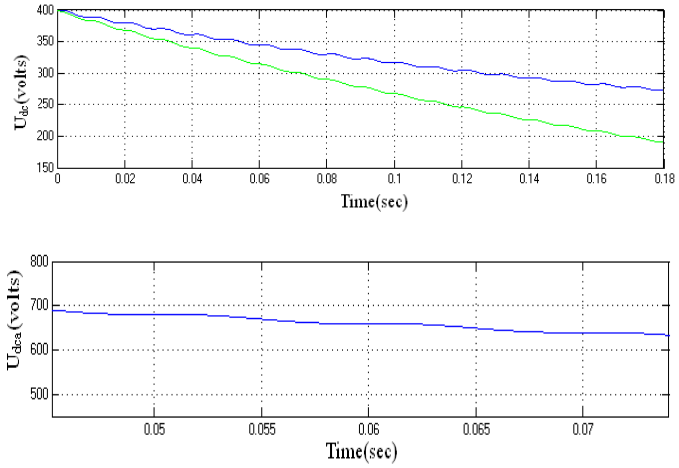


Fig.6 DC voltage waves when no voltage loops are added

When DC voltage control loop is not added, the two capacitor voltages are differ from each other and the sum of them is not equal to the set value, as shown in Fig.6.

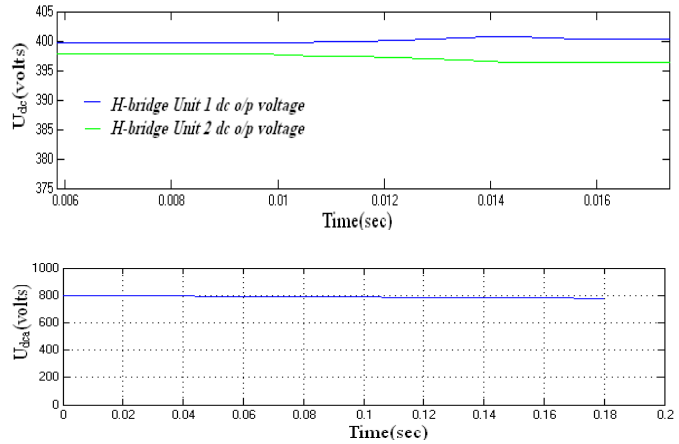
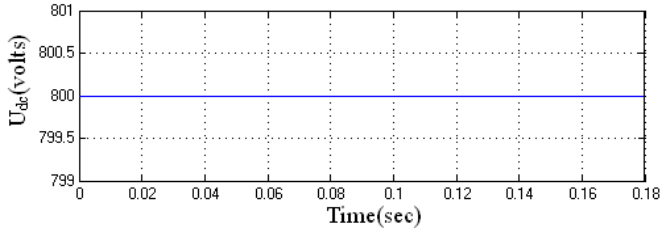


Fig.7 DC voltage waveforms when only the overall active power control loop is added

When the overall active power control loop is added while the individual voltage balance control loop is not added, the sum of the two capacitor voltages are equal to the set value but they are differ from each other as shown in Fig.7.



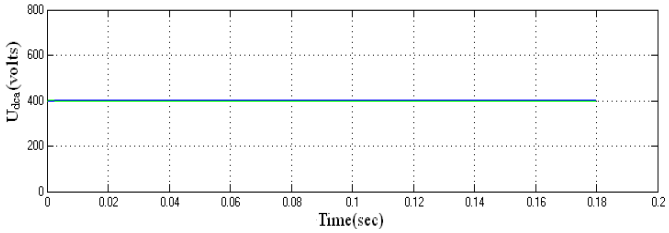


Fig.8 DC voltage waveforms when DC voltage control loops are added

When both the overall active power control loop and the individual voltage balance control loop are added to the whole control system, the two capacitor voltages are equal to the set value and they are balanced.

It can be seen that the two DC capacitor voltages fluctuate at the point of 400V and are simultaneously balanced in steady states. The proposed control method is effective and has good steady state characteristics.

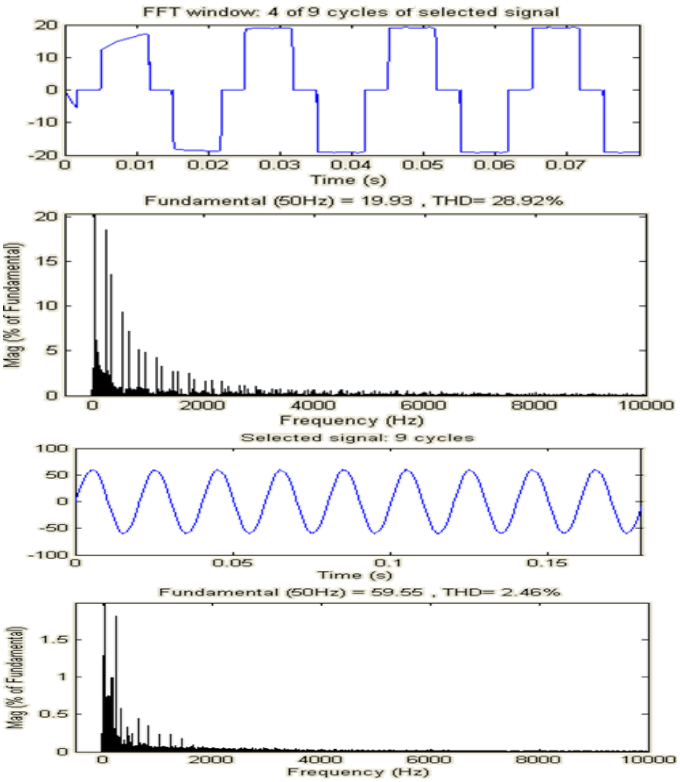


Fig.9 Steady waveforms of load current and system supply current and THD spectrum

The THD (total harmonic distortion) of load current is calculated to be 28.92%. The THD of supply current is 2.46%. The simulation results proved that the proposed power quality conditioner has good steady filtering capability.

Parameters of the circuit:
Switching frequency is 10 kHz,
DC capacitance is 3300uF
DC voltage of each H-bridge unit is 400V

Equivalent resistances, $R_{dc_{a1}} = 150\Omega$ and $R_{dc_{a2}} = 350\Omega$. The values are same for all the three phases.

6. CONCLUSIONS

This paper presents a detailed theoretical analysis of dc voltage balance method of H- bridge inverter. The active power absorbed by each unit of H- bridge inverter is controlled by varying the width of the output pulses of the inverter. Thereby the dc voltage s of both the units of each phase are made equal. Simulation results prove that THD of supply current has been reduced to 2.46%. This control technique can be applied to STATCOMs, APFs, energy storage systems and asymmetrical multilevel inverters.

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