COMPARISON OF PARALLEL SUMMATION AND WEAK INVERSION BASED LOGARITHMIC AMPLIFIER

Amrutha Paul[1], N.Kayalvizhi[2]

[1]*ECE Department, Amrita VishwaVidyapeetham, Coimbatore, India*
[2]*ECE Department, Amrita VishwaVidyapeetham, Coimbatore, India*

Abstract

Logarithmic amplifier is used for reducing the dynamic range of the input signal. Logarithmic amplifier is implemented using two different techniques. One of the methods is a parallel summation based method and the other one is a weak inversion based method. In parallel summation based method the transistors are maintained in saturation whereas in weak inversion based method the transistors are maintained in weak inversion. Both methods are simulated in 50nm CMOS technology using HSPICE. Considering power, area and dynamic range weak inversion method is more efficient compared to parallel summation method.

Keywords: *Logarithmic amplifier, Parallel SummationLogarithmic amplifier;WeakInversion;Saturation;MOSFET;*

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1. INTRODUCTION

A Logarithmic amplifier will convert a nonlinear transducer characteristics into linear characteristics.[1]-[2].A good example of a nonlinear sensor is a thermistor. The exponential Resistance-Temperature characteristics of a thermistor can be linearized with the help of a Logarithmic network. The theory behind this is that when the resistance of a thermistor varies exponentially with change in temperature. This causes the voltage across the thermistor probe to vary exponentially with temperature. So by applying this to a Logarithmic network, the variation of resistance of the thermistor will be linear with the temperature[3]. Logarithmic amplifiers can be realized using different methods. Opamp based Logarithmic amplifiers[4]uses diodes or bipolar transistors in their feedback path to get logarithmic relationship between input voltage and output voltage by exploiting their exponential dependence between current and voltage. Most of the methods have their own advantages and disadvantages. We can use weak inversion MOSFET's to realize a Logarithmic relationship between input voltage or current and output voltage or current respectively. This method is less power consuming as MOSFET's are scaled down and also the power supply is also scaled down.

Logarithmic amplifiers are used in radio receivers [5],radar signal receivers for reducing the dynamic range of the input signal due to compressive nature of the log function.

This paper aims at the comparative study of two important Logarithmic amplifier techniques which can be used to linearize a nonlinear transducer characteristic. This paper is organized into sections as follows. In Section II, Logarithmic amplifiers are discussed in detail; the theory behind parallel summation Logarithmic amplifier and weak inversion Logarithmic amplifiers are also explained. In Section III, some important design considerations are discussed and in Section IV the results and analysis is discussed. Finally the paper is concluded in Section V.

2. LOGARITHMIC AMPLIFIERS

Logarithmic amplifiers are usually constructed with diode or bipolar transistors in the feedback path of an inverting opamp. However its operation is limited to low frequencies. Logarithmic amplifiers are used to linearize a nonlinear input signal or to reduce the range of a signal with large dynamic range. Usually a MOSFET based ASIC design has many advantages like low power consumption, small area, etc. A basic Logarithmic amplifier module consists of a clipping amplifier and a voltage to current converter. So if we cascade this stage repeatedly then we will obtain a more linearized output voltage which will be proportional to the sensed temperature. This output voltage will be given to a dual slope digital converter[6]. The dual slope digital converter is a complex module which provides a digital output corresponding to the temperature sensed. Logarithmic amplifier can be realized using various methods. Here a comparative study of two important methods is done.

1. Parallel Summation based Logarithmic amplifier[6]
2. Weak Inversion based Logarithmic amplifier

Both of these methods are discussed in this paper and their transfer functions are plotted.

2.1 Parallel Summation based Logarithmic Amplifiers

Parallel Summation method uses MOSFET in saturation. In this region of operation. MOSFET uses square law of Current whereas in Weak Inversion, a MOSFET uses exponential relationship between drain current and gate to source voltage. Usually we use saturated MOSFETs for realization of different circuits. But this will result in high power consumption due to a large supply voltage. So in order to reduce the power consumption weak inversion biased MOSFET's are a good alternative.

Parallel summation method uses MOSFET's linear region to get a linear response. This method is achieved by cascading n number of gain stages. So by increasing the number of gain stages we can increase the dynamic range upto which the response of a signal can be linearized. Parallel summation based method is realized with a single block consisting of a gain stage A and a unity gain stage repeated n times to get a linear characteristics between output and the input.

The Figure1 shows the Parallel Summation based method Parallel summation method is one of the good methods for implementing the Logarithmic amplifier using MOSFET'S biased in saturation. We can reduce the power consumption of the saturated MOS transistors by using the MOS transistors in weak inversion.

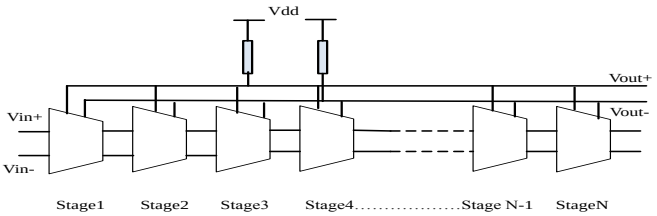

Fig 1. Parallel Summation Method

MOS transistors in saturation region will satisfy the following equations

$$V_{DS} \geq V_{GS} - V_{TH} \quad (1)$$

$$I_D = K_n' \frac{W}{L}(V_{GS} - V_{TH})^2 \quad (2)$$

$$K_n' = \mu_n C_{OX} \quad (3)$$

$$V_{GS} \geq V_{TH} \quad (4)$$

These equations satisfies the condition for saturation even though a subthreshold current flows through the MOSFET, when $V_{GS} \geq V_{TH}$.

2.2 Weak Inversion based Logarithmic Amplifier

The core of the proposed design is an extended translinear principle proposed by Hart[7].Weak inversion based method uses MOS biased in weak inversion. Weak inversion biasing is a new concept introduced in the field of MOSFET's where usual biasing is carried out in saturation region. Weak inversion is realized by making MOSFET's V_{GS} very much less than the threshold voltage V_{TH}. The threshold voltage is obtained by plotting I_D vs V_{GS} characteristics and then extrapolating the curve to x-axis. The intersection of the curve to the x-axis is the threshold voltage. Also we have to ensure that V_{DS} 4 V_T. When these conditions are met, a sub-micrometer current will flow through the channel.

This particular situation can be analyzed by the majority carriers being depleted away from the surface of the substrate. Thus a region of fixed charges will be created. The density of minority carriers also increases over time. Thus there is a current called subthreshold current which was neglected for years since it was at the submicrometer level. MOS transistors are usually used with strongly inverted channel where drain current is at micrometer level whereas in weak inversion we will use MOS transistors with lightly inverted channel with a subthreshold current flow, due to diffusion of the charge carriers. The most important application of MOS in weak inversion is the reduction in power consumption due to the scaling of the supply voltage.

As the voltages are scaled down with that of the transistor size, the subthreshold conduction has become an important. The reason for this is that the supply voltage was scaled down continuously for power reduction. But as a result leakage has been increased very much. The amount of subthreshold conduction is determined by the threshold voltage. The threshold voltage also has to be scaled down with the scaling of supply voltage. This tells us the need of the biasing of transistors in weak inversion. In MOSFET's the weak inversion characteristics is exponential in nature. So to build a Logarithmic amplifier using MOSFET to linearize the nonlinear characteristics is quiet easy. After taking Logarithmic of the exponential characteristics we will get a linearized curve.

MOSFET's biased in weak inversion region will satisfy the equations

$$I_D = I_S \frac{W}{L} e^{\left(\frac{V_{GS}-V_T}{nV_{TH}}\right)} \{1 - e^{(V_{DS}/V_T)}\} \quad (5)$$

$$V_{DS} = V_{GS} - V_{TH}$$
$$V_{DS} \geq 3V_T \quad (7)$$
$$V_{GS} \leq V_{TH}$$

I_S is the subthreshold leakage current

Here I_D is exponentially related to V_{GS} and V_{DS} ,where V_{DS} is directly proportional to the gate source voltage, V_{GS} . Also I_D depends on temperature directly in weak inversion. So at weak inversion also, which is a region fully avoided has some importance when linearization of the output of transducers is important. To be specific in case of a trasducer for e.g. a thermistor, which has an exponential resistance temperature characteristics, can be linearized by using a Logarithmic amplifier. The temperature dependence can be easily compensated by applying translinear principle[10].

A translinear circuit carries out its function using the translinear principle. The translinear principle states that in a closed loop containing an even number of translinear elements

with the same number of them arranged in clockwise and in anti-clockwise direction , the product of the currents through the clockwise translinear elements will be equal to the product of the currents through the anti-clockwise translinear elements. The transconductance of the collector current of a MOS transistor is linearly related to the collector current of the device. Traditionally translinear circuits have been realized using bipolar transistors. MOS transistor can also be used as translinear element when operated in the subthreshold region.

3. DESIGN AND IMPLEMENTATION

Parallel Summation based circuit and Translinear based Weak Inversion circuit is implemented in HSPICE tool in 50µm CMOS technology. Parallel Summation based circuit is given in Figure3 and Weak inversion based circuit is given in Figure4. The aspect ratios of the transistors for both the parallel summation based as well as weak inversion based method is given in table2.

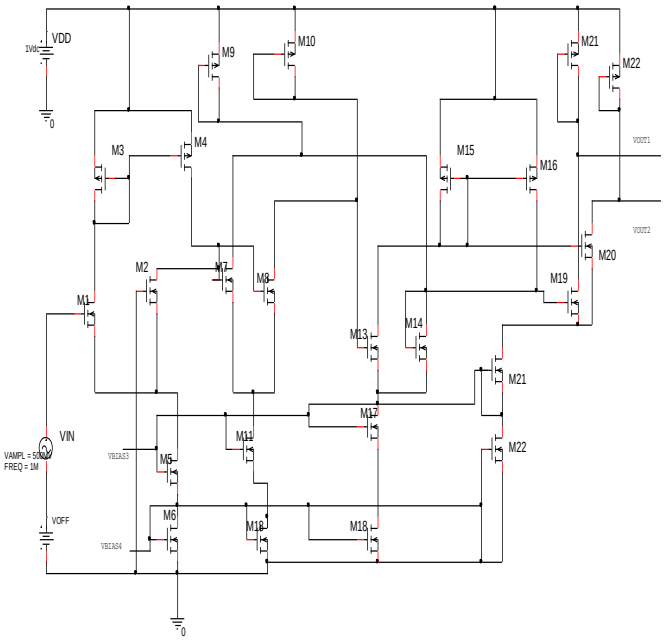

Fig2 Parallel Summation Method

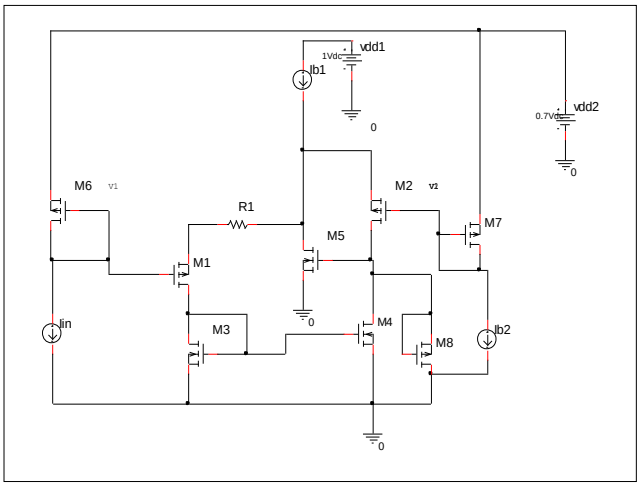

Fig 3 Weak Inversion Method

Simulation of both the circuits are done and the output transfer characteristics are plotted for both the circuits. Also transient analysis is done using HSPICE

Table 1 Transistors and their aspect ratios

Methods	Transistors	W/LRatios	
		PMOS µm	NMOS µm
Parallel Summation Based	M9,M10,M21,M22	100/2	_
	M1,M2,M3,M4,M5,M6,M7 ,M8,M9,M10,M11,M12,M1 3,M14,M15,M16,M17,M18 ,M19,M20	_	50/2
Weak Inversion Based	M1	186/1	_
	M2,M3,M4	_	186/1
	M6,M7	1.268/1 00	_
	M8	_	50/2

4. RESULTS AND DISCUSSION

Comparison of both the methods is done and the graphical analysis of the two methods are done using HSPICE simulator. The comparison results are placed in Table3. Slew rate of the circuit is measured with and without a current amplifier at the output of the weakinversion based log amplifier. It is found that slew rate increases after cascading a current amplifier. Slew rate before cascading was 0.5v/µs and after the cascading of the current amplifier was 2.079v/µs.Also a plot of output current vs input current was plotted with different bias currents as in Figure 6.

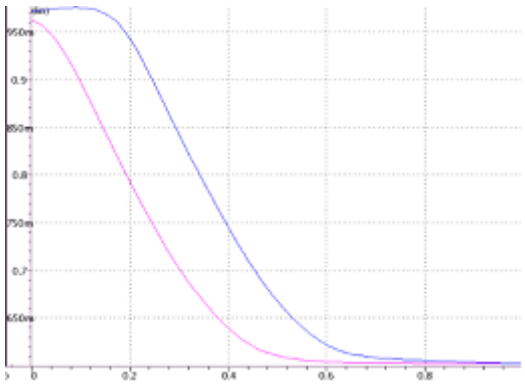

Fig 4 Parallel Summation Transfer Characteristics

We can see from Figure6 that when the bias currents are increased the graph becomes more linear . The bias current is varied from 1nA to 5nA. Table2and Table3 has the tabulation for Figure4 and Figure5. In Table2 Vout1 is the output of stage1 and Vout2 is the output of stage2. In Table3 tabulation for output current vs input current is given. Input current is varied from 0µA to 100µA.

Table 2 Parallel Summation based method

V_{IN} (V)	V_{OUT1} (V)	V_{OUT2} (V)
10E-3	1.39	1.3946
100E-3	1.38	1.4220
200E-3	1.28	1.4235
300E-3	1.19	1.3453
400E-3	1.13	1.2451
500E-3	1.11	1.1683
600E-3	1.10	1.1249
700E-3	1.10	1.1131
800E-3	1.10	1.1103
900E-3	1.10	1.1183
1000E-3	1.10	1.1065

In Figure5 we can see that the output current vs input current graph is almost a straight line which concludes that the output vs input relation is more linear. Also upto 100µA range the output is linear.

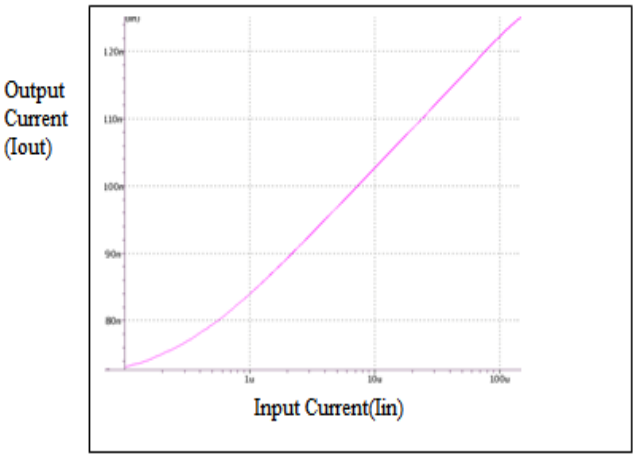

Fig 5 Weak Inversion Transfer Characteristic

Table 3 Weak Inversion based method

I_{IN} (V)	I_{OUT} (V)	I_{IN} (V)	I_{OUT} (V)
100E-9	73.0409E-9	6E-6	98.3925E-9
200E-9	75.0338E-9	7E-6	99.6842E-9
300E-9	76.7042E-9	8E-6	100.8035E-9
400E-9	78.1372E-9	9E-6	101.7909E-9
500E-9	79.3888E-9	10E-6	102.6744E-9
600E-9	80.4978E-9	20E-6	108.4995E-9
700E-9	81.4919E-9	30E-6	111.9358E-9
800E-9	82.3919E-9	40E-6	114.3959E-9
900E-9	83.2134E-9	50E-6	116.3163E-9
1E-6	83.9685E-9	60E-6	117.8893E-9
2E-6	89.3036E-9	70E-6	119.2163E-9
3E-6	92.6138E-9	80E-6	120.3568E-9
4E-6	95.0022E-9	90E-6	121.3479E-9
5E-6	96.8661E-9	100E-6	122.2138E-9

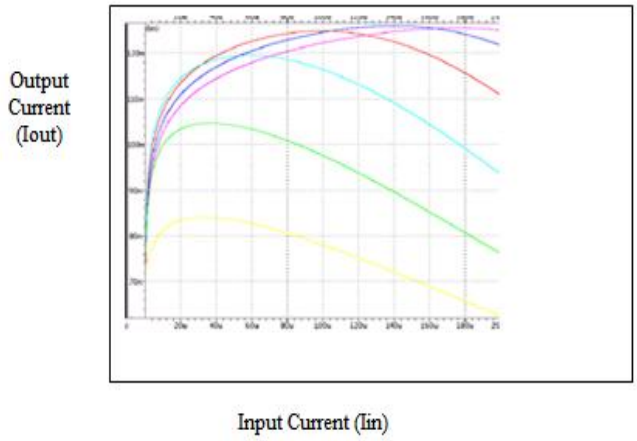

Fig 6 Iout vs Iin for different biasing currents

AC analysis of the weak inversion circuit is also done with and without a current amplifier at the output. Gain was increased while taking the output with the current amplifier. The gain vs frequency plot before cascading a current amplifier is given in Figure7 and after cascading is given in Figure8.

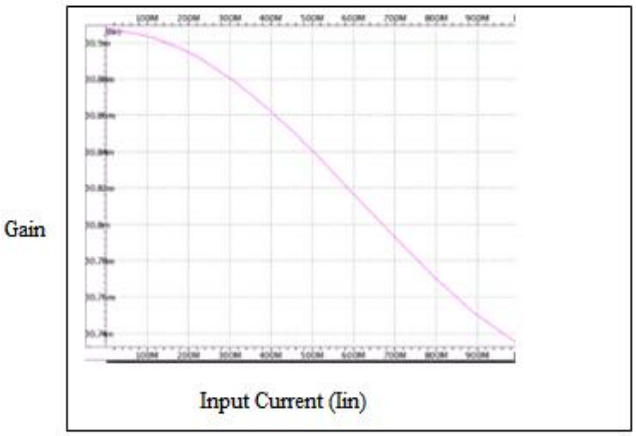

Fig 7 Gain vs frequency plot before cascading

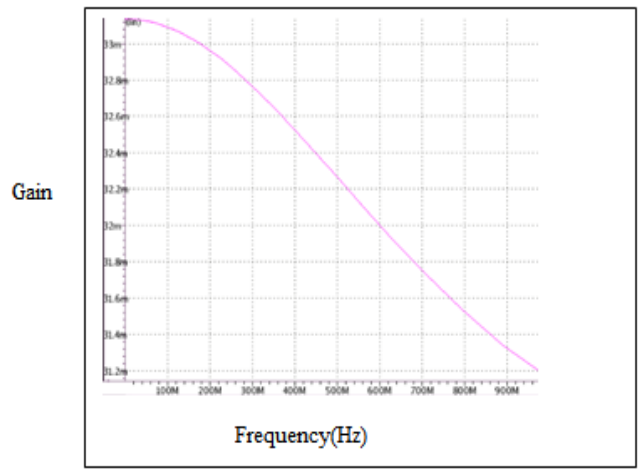

Fig 8 Gain vs frequency plot after cascading

5. CONCLUSIONS

In this paper, a comparison between two Logarithmic amplifier methods is done. It was found that the Logarithmic amplifier in Weak Inversion region has achieved more linearization than the parallel summation Logarithmic amplifier technique which uses MOSFET biased in saturation. By using weak inversion based method the dynamic range of a Logarithmic amplifier can be improved. Also power reduction is achieved using this technique.

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